



AKD4584

Evaluation board Rev.A for AK4584

GENERAL DESCRIPTION

AKD4584 is an evaluation board for the 24bit 96kHz CODEC, AK4584. The AKD4584 can evaluate A/D converter D/A converter separately in addition to loopback mode (A/D → D/A). The AKD4584 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4584 --- Evaluation board for AK4584
 (Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this.)

FUNCTION

- DIT/DIR with optical input/output
- BNC connector for an external clock input
- 10pin Header for serial control mode

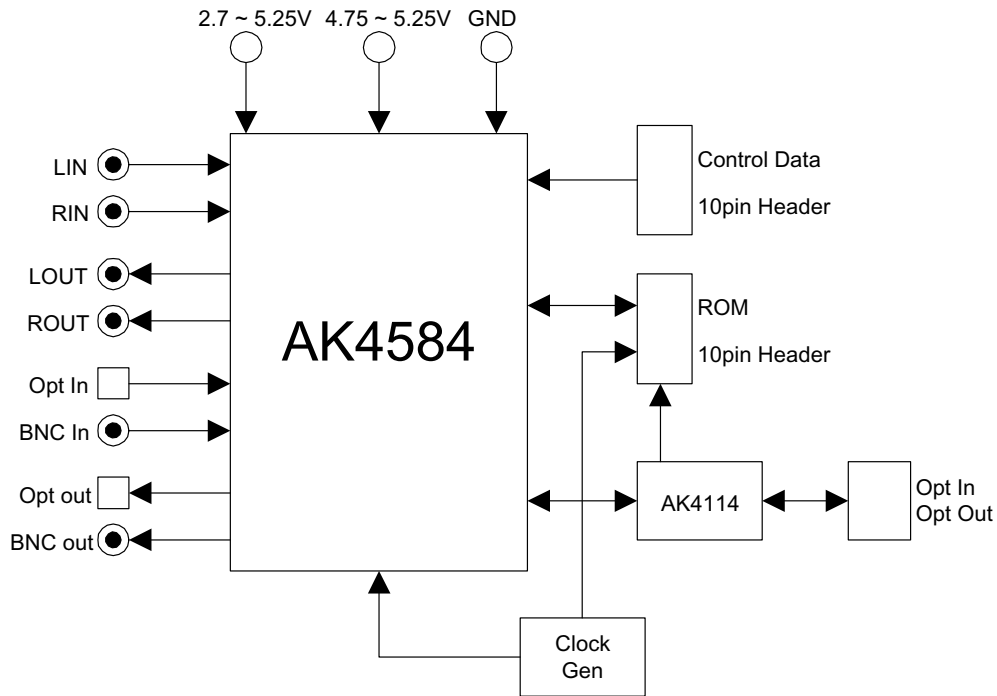


Figure 1. AKD4584 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

1. Evaluation Board Manual

■ Analog Input / Output circuits

(1) Input circuits

The analog input of AK4584 inputs from J1 (RIN), J3 (LIN).

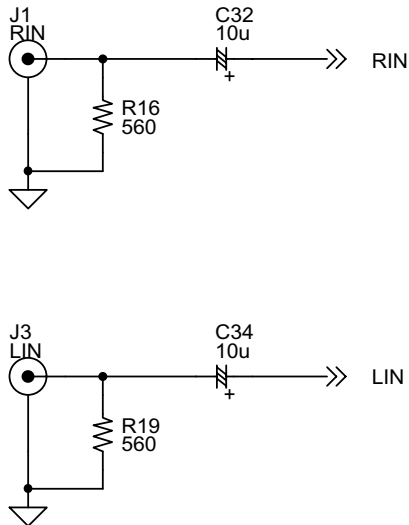


Figure 2. LIN/RIN Input circuits

(2) Output circuits

The analog output of AK4584's DAC outputs from J2 (ROUT), J4 (LOUT).

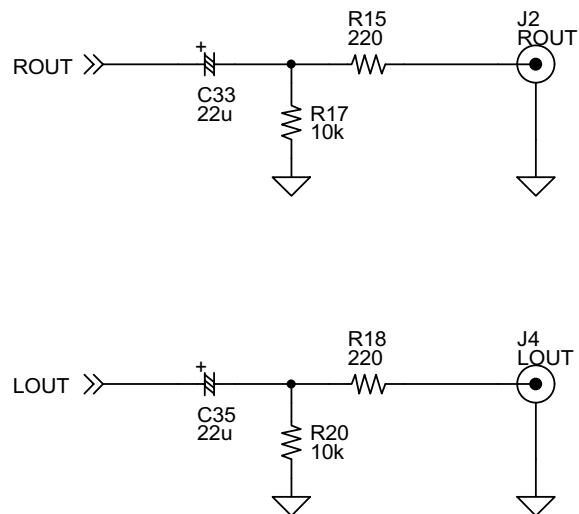


Figure 3. LOUT/ROUT Output circuits

* AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Digital Input / Output circuits & Set-up jumper pin

(1) Digital input circuits

The digital input of AK4584 inputs from J7 (RX) or PORT5 (DIR).

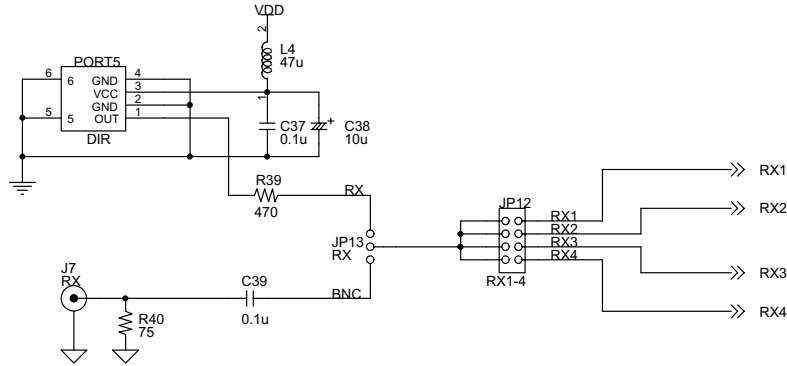
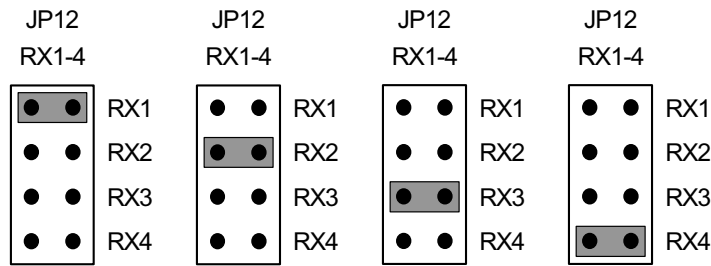
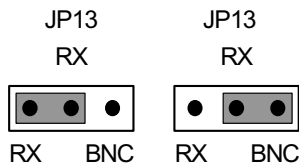


Figure 4. Digital input circuit

1. Digital signal is input to RX1-4 pins respectively.



2. Digital signal is input to RX1-4 pins via J7 (RX) and PORT5 (DIR).



* AKM assumes no responsibility for the trouble when using the above circuit examples.

(2) Digital output circuits

The digital output of AK4584 inputs from J6 (TX) or PORT4 (DIT).

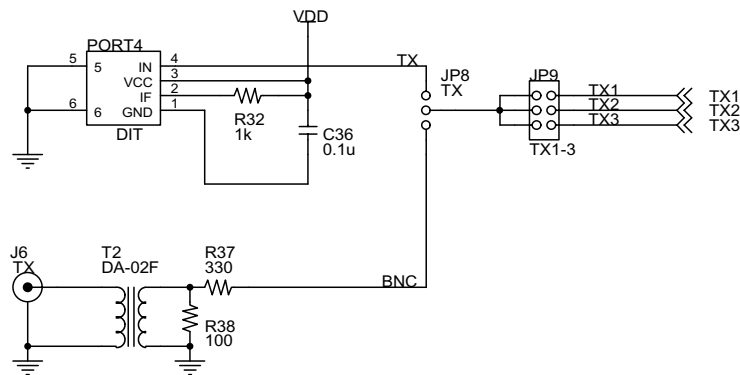
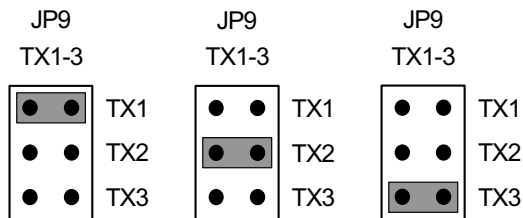
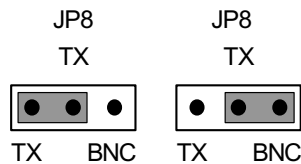


Figure 5. Digital output circuit

1. Digital signal is output to TX1-3 pins respectively.



2. Digital signal is output to TX1-3 pins via J6 (TX) and PORT4 (DIT).



* AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Operation sequence

1) Set up the power supply lines.

[AVDD]	(red)	= 4.75 ~ 5.25V	: for AVDD, DVDD, PVDD of AK4584 (typ. 5.0V)
[TVDD]	(orange)	= 2.7 ~ 5.25V	: for TVDD of AK4584 (typ. 3.0V)
[VCC]	(red)	= 5.0V	: for logic (typ. 5.0V)
[VDD]	(red)	= 5.0V	: for logic (typ. 5.0V)
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

The AK4584 should be reset once bringing SW1 "L" upon power-up.

■ Evaluation mode

(1) Slave mode

In case of AK4584 evaluation using AK4114, it is necessary to correspond to AK4584's and AK4114's audio interface format. About AK4584's audio interface format, refer to AK4584's datasheet. About AK4114's audio interface format, see Table2.

(1-1) A/D evaluation using DIT function of AK4584

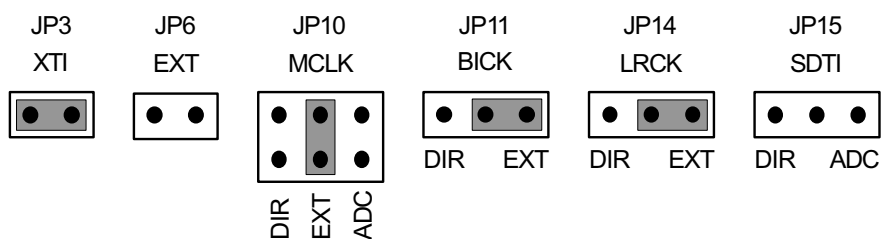
(1-2) A/D evaluation using DIT function of AK4114

(1-3) D/A evaluation using DIR function of AK4114

(1-4) All interfacing signal (MCLK, BICK, LRCK) are fed from the external circuit

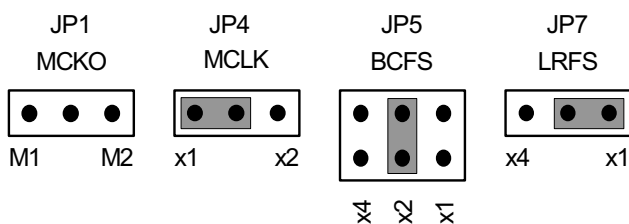
(1-1) A/D evaluation using DIT function of AK4584

Using J5 (EXT), PORT4 (DIT) and J6 (TX). Nothing should be connected to J7 (RX), PORT1 (DIR), PORT5 (DIR) and PORT6 (ROM). Remove the X'tal (X1). The bi-phase data is output from TX3. JP6 (EXT) should be open.

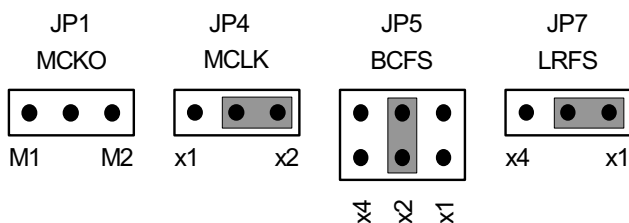


• Clock setting

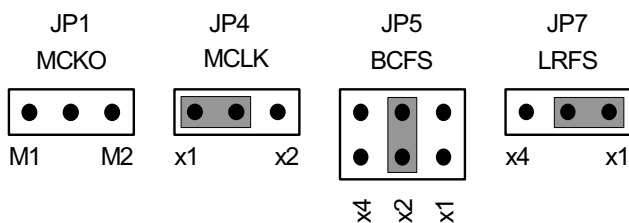
(1-1-1) Normal Speed (MCLK=256fs=11.2896MHz@fs=44.1kHz)



(1-1-2) Normal Speed (MCLK=512fs=22.5792MHz@fs=44.1kHz)



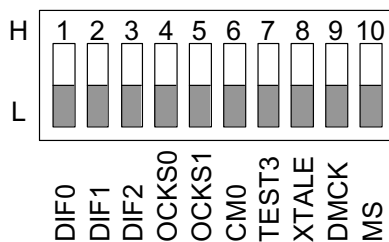
(1-1-3) Double Speed (MCLK=256fs=22.5792MHz@fs=88.2kHz)



• SW2 (MODE) setting (See Table 1)

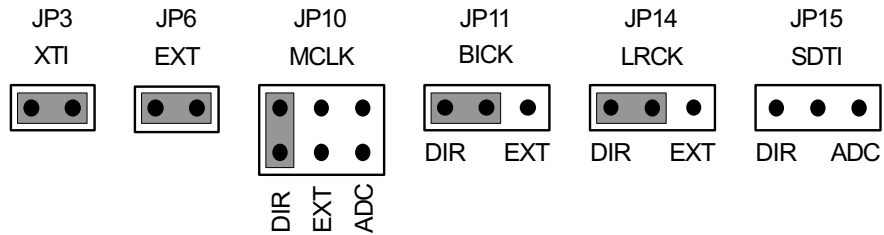
Normal speed and double speed are same setting.

- (1) When XTALE is "H", MCLK can output from MCKO1/2 pins though AK4584 is powered down.
- (2) When DMCK is "H", MCKO1 output is disabled.



(1-2) A/D evaluation using DIT function of AK4114

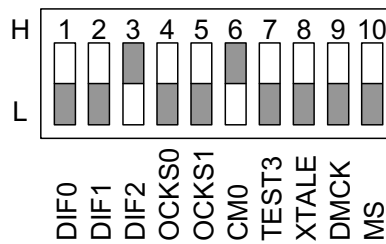
Using X'tal (X2) and PORT2 (DIT). Nothing should be connected to J5 (EXT), J7 (RX), PORT1 (DIR), PORT5 (DIR) and PORT6 (ROM). Remove the X'tal (X1). JP6 (EXT) should be short. In normal speed and double speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.



• SW2 (MODE) setting (See Table 1)

Normal speed and double speed are same setting.

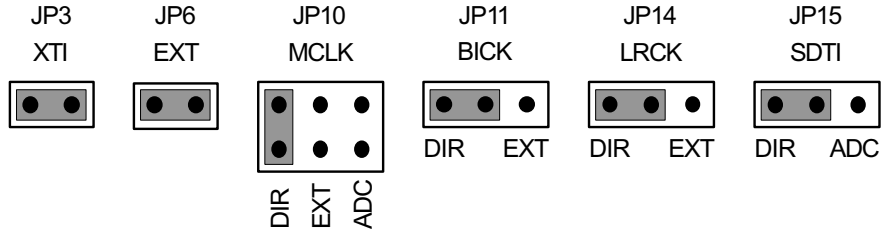
- (1) Set the audio interface format of AK4114 using DIF2-0.
- (2) Set the master clock output of AK4114 using OCKS1-0.
- (3) Set the PLL mode or X'tal mode of AK4114 using CM0.
- (4) When XTAL is "H", MCLK can output from MCKO1/2 pins though AK4584 is powered down.
- (5) When DMCK is "H", MCKO1 output is disabled.



Above figure is 24bit MSB justified, MCKO output of AK4114 is 256fs, AK4114 is X'tal mode. Using DIT of AK4114, AK4114 is set X'tal mode.

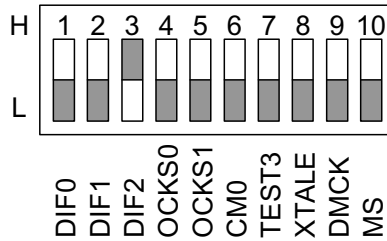
(1-3) D/A evaluation using DIR function of AK4114

Using PORT1 (DIR). Nothing should be connected to J7 (RX), PORT5 (DIR) and PORT6 (ROM). Remove the X'tal (X1). JP6 (EXT) should be short. In normal speed, double speed mode and quad speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.



• SW2 (MODE) setting (See Table 1)

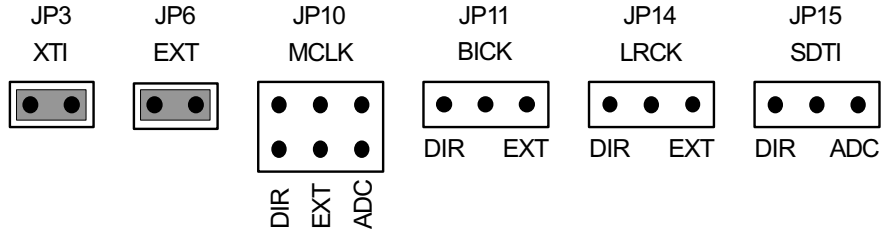
- (1) Set the audio interface format of AK4114 using DIF2-0.
- (2) Set the master clock output of AK4114 using OCKS1-0.
- (3) Set the PLL mode or X'tal mode of AK4114 using CM0.
- (4) When XTALE is "H", MCLK can output from MCKO1/2 pins though AK4584 is powered down.
- (5) When DMCK is "H", MCKO1 output is disabled.



Above figure is 24bit MSB justified, MCKO output of AK4114 is 256fs, AK4114 is PLL mode. In quad speed mode of AK4114, set OCKS1="H" and OCKS0="H". The MCKO output of AK4114 is output 128fs.

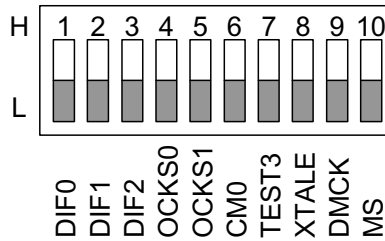
(1-4) All interfacing signal (MCLK, BICK, LRCK) are fed from the external circuit

Using PORT6 (ROM). Nothing should be connected to J7 (RX), PORT1 (DIR) and PORT5 (DIR). Remove the X'tal (X1). JP6 (EXT) should be short. In normal speed, double speed mode and quad speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.



• SW2 (MODE) setting (See Table 1)

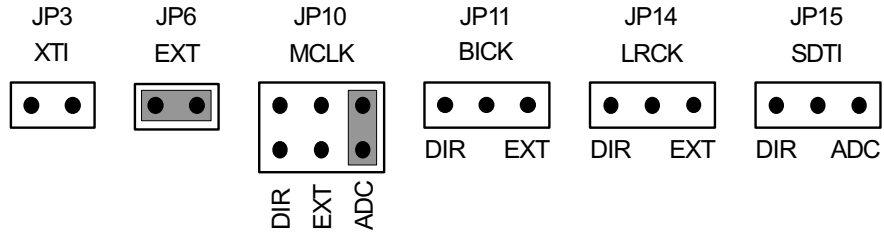
- (1) When XTALE is “H”, MCLK can output from MCKO1/2 pins though AK4584 is powered down.
- (2) When DMCK is “H”, MCKO1 output is disabled.



(2) Master Mode

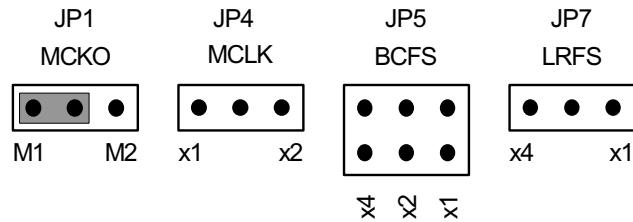
(2-1) A/D evaluation using DIT function of AK4584

Using X'tal (X1), PORT4 (DIT) and J6 (TX). Nothing should be connected to J7 (RX), PORT1 (DIR), PORT5 (DIR) and PORT6 (ROM). The bi-phase data is output from TX3. JP6 (EXT) should be short. In normal speed, double speed mode and quad speed mode, JP3 (XTI), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.

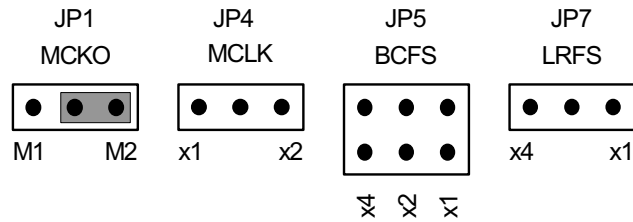


• Clock Setting

(2-1-1) Select MCKO1



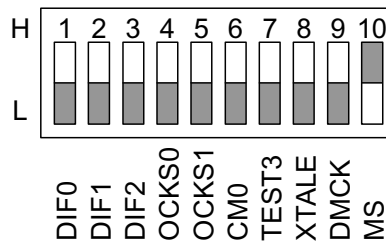
(2-1-2) Select MCKO2



• SW2 (MODE) setting (See Table 1)

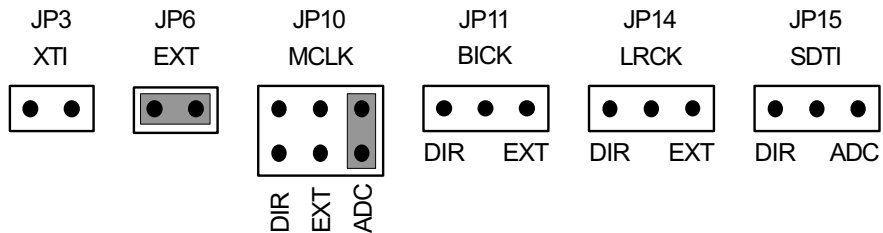
Normal speed and double speed are same setting.

- (1) When XTALE is “H”, MCLK can output from MCKO1/2 pins though AK4584 is powered down.
- (2) When DMCK is “H”, MCKO1 output is disabled.



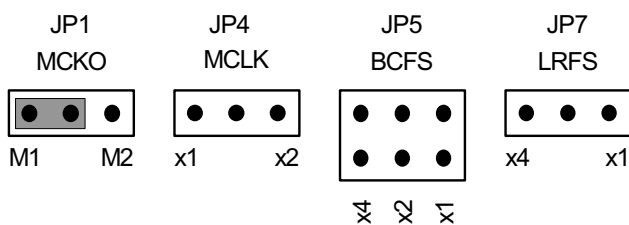
(2-2) D/A evaluation using DIR function of AK4584

Using PORT5 (DIR) or J7 (RX). Nothing should be connected to PORT1 (DIR) and PORT6 (ROM). JP6 (EXT) should be short. In normal speed and double speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.

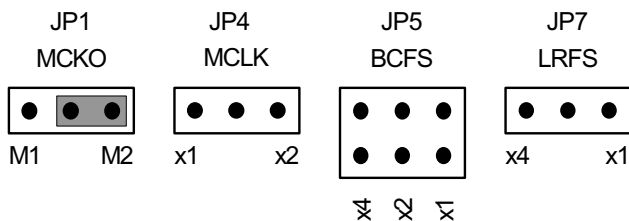


• Clock setting

(2-2-1) Select MCKO1



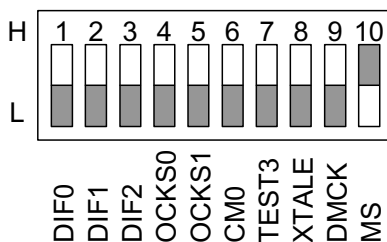
(2-2-2) Select MCKO2



• SW2 (MODE) setting (See Table 1)

Normal speed, double speed and quad speed mode are same setting.

- (1) When XTALE is “H”, MCLK can output from MCKO1/2 pins though AK4584 is powered down.
- (2) When DMCK is “H”, MCKO1 output is disabled.



■ DIP Switch set up

[SW2] (MODE): Setting evaluation mode for AK4584 and AK4114
ON is “H”, OFF is “L”.

No.	Name	ON (“H”)	OFF (“L”)
1	DIF0	AK4114 Audio Format Setting See Table 2	
2	DIF1		
3	DIF2		
4	OCKS0	AK4114 Master Clock Output Setting See Table 3	
5	OCKS1		
6	CM0	AK4114 X’tal Mode	AK4114 PLL Mode
7	TEST3	Normally OFF	
8	XTALE	MCKO1/2 Enable	MCKO1/2 Disable
9	DMCK	MCKO1 Disable	MCKO1 Enable
10	M/S	Master Mode	Slave Mode

Table 1. Setting mode for AK4584 and AK4114

Mode	DIF2	DIF1	DIF0	AK4114 DAUX	AK4114 SDTO
0	0	0	0	24bit, MSB justified	16bit, LSB justified
1	0	0	1	24bit, MSB justified	18bit, LSB justified
2	0	1	0	24bit, MSB justified	20bit, LSB justified
3	0	1	1	24bit, MSB justified	24bit, LSB justified
4	1	0	0	24bit, MSB justified	24bit, MSB justified
5	1	0	1	24bit, I ² S	24bit, I ² S

Table 2. Setting AK4114 audio interface format

Mode	OCKS1	OCKS0	MCKO1	X’tal	fs
0	0	0	256fs	256fs	~ 96kHz
1	0	1	256fs	256fs	~ 96kHz
2	1	0	512fs	512fs	~ 48kHz
3	1	1	128fs	128fs	~ 192kHz

Table 3. Setting AK4114 master clock output

■ Other jumper pins set up

- JP1 (GND) : Analog ground and Digital ground
OPEN : Separated. <Default>
SHORT : Common. (The connector “DGND” can be open.)

■ The function of the toggle SW

Upper-side is “H” and lower-side is “L”.

[SW1] (PDN): Power down of AK4584. Keep “H” during normal operation.

[SW3] (DIR): Power down of AK4114. Keep “H” during normal operation.

■ Indication for LED

[LED1] (INT0): Output INT0 pin of AK4584.

[LED2] (INT1): Output INT1 pin of AK4584.

[LED3] (ERF): Output INT0 pin of AK4114.

[LED4] (DZF): Output DZF pin of AK4584.

■ Serial Control

The AK4584 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (CTRL) with PC by 10 wire flat cable packed with the AKD4584.

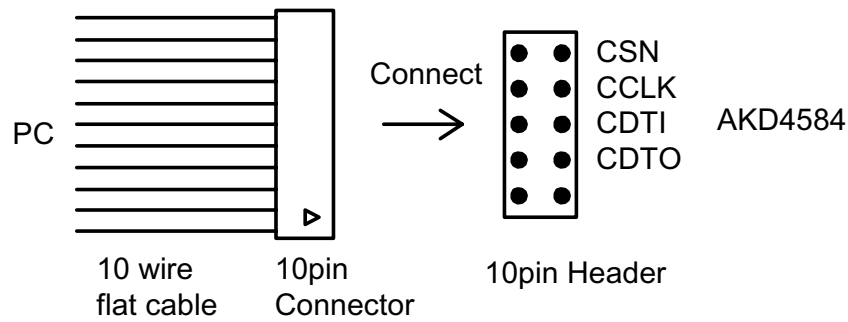


Figure 6. Connect of 10 wire flat cable

2. Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4584 according to previous term.
2. Connect IBM-AT compatible PC with AKD4584 by 10-line type flat cable (packed with AKD4584). Take care of the direction of 10pin header. (This control software does not operate on Windows NT/2000, therefore please operate it on Windows 95/98.)
3. Insert the floppy-disk labeled “AKD4584 Control Program ver 1.0” into the floppy-disk drive.
4. Access the floppy-disk drive and double-click the icon of “akd4584-1.exe” and “akd4584-2” to set up the control program.
5. Then please evaluate according to the follows.

■ Explanation of each buttons

1. [Port Setup] : Set up the printer port.
2. [Write default] : Initialize the register of AK4584.
3. [All Read] : Read the all register of AK4584.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function2] : Dialog to evaluate IPGA and OATT.
6. [Write] : Dialog to write data by mouse operation.
7. [Read] : Read each register data by mouse operation.

■ Explanation of each dialog

1. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input register address in 2 figures of hexadecimal.
Data Box: Input register data in 2 figures of hexadecimal.

If you want to write the input data to AK4584, click “OK” button. If not, click “Cancel” button.

2. [Function2 Dialog] : Dialog to evaluate IPGA and OATT

This dialog corresponds to only addr=04H, 05H, 06H, 07H.

Address Box: Input register address in 2 figures of hexadecimal.
Start Data Box: Input start data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4584 by this interval.
Step Box: Data changes by this step.

Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.

[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.

[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4584, click “OK” button. If not, click “Cancel” button.

3. [Write Dialog] : Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the “Write” button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4584, click “OK” button. If not, click “Cancel” button.

■ Operation flow

Keep the following flow surely.

1. Set up the control program according to explanation above.
2. Click “Port Setup” button.
3. Click “Write default” button.
4. Then set up the dialog and input data.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Attention on the operation

If you set up Function1 or Function2 dialog, input data to all boxes. Attention dialog is indicated if you input data or address that is not specified in the datasheet or you click “OK” button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click “Cancel” button or check the check box.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit: Audio Precision, System Two Cascade
- MCLK : 256fs
- BCLK : 64fs
- fs : 44.1kHz, 96kHz
- Bit : 24bit
- Power Supply : AVDD=DVDD=TVDD=PVDD=5.0V
- Interface : DIR/DIT
- Temperature : Room

[Measurement Results]

Parameter	Result	Unit
ADC Analog Input Characteristics		
S/(N+D)		
(fs=44.1kHz, -0.5dB Input)	92.0	dB
(fs=96kHz, -0.5dB Input)	88.3	dB
D-Range		
(fs=44.1kHz, -60dB Input, A-weighted)	100.6	dB
(fs=96kHz, -60dB Input)	96.1	dB
S/N		
(fs=44.1kHz, A-weighted)	101.0	dB
(fs=96kHz)	96.1	dB
Interchannel Isolation	110.5	dB
DAC Analog Output Characteristics		
S/(N+D)		
(fs=44.1kHz, 0dB Output)	95.3	dB
(fs=96kHz, -0.5dB Output)	95.1	dB
D-Range		
(fs=44.1kHz, -60dB Output, A-weighted)	105.5	dB
(fs=96kHz, -60dB Output)	100.4	dB
S/N		
(fs=44.1kHz, A-weighted)	105.9	dB
(fs=96kHz)	100.5	dB
Interchannel Isolation	115.5	dB

[ADC Plot : fs=44.1kHz]

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AK4584 ADC THD+N vs. Input Level
VDD=5.0V, fs=44.1kHz, fin=1kHz

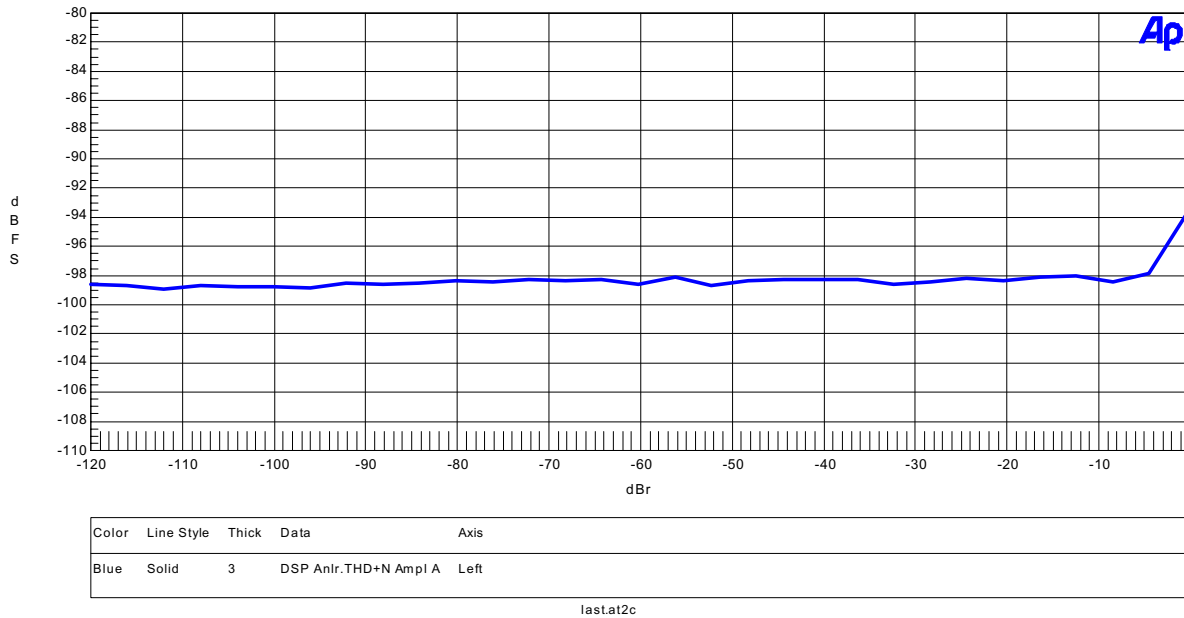


Figure 1. THD+N vs. Input Level

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AK4584 ADC THD+N vs. Input Frequency
VDD=5.0V, fs=44.1kHz, Input=-0.5dBr

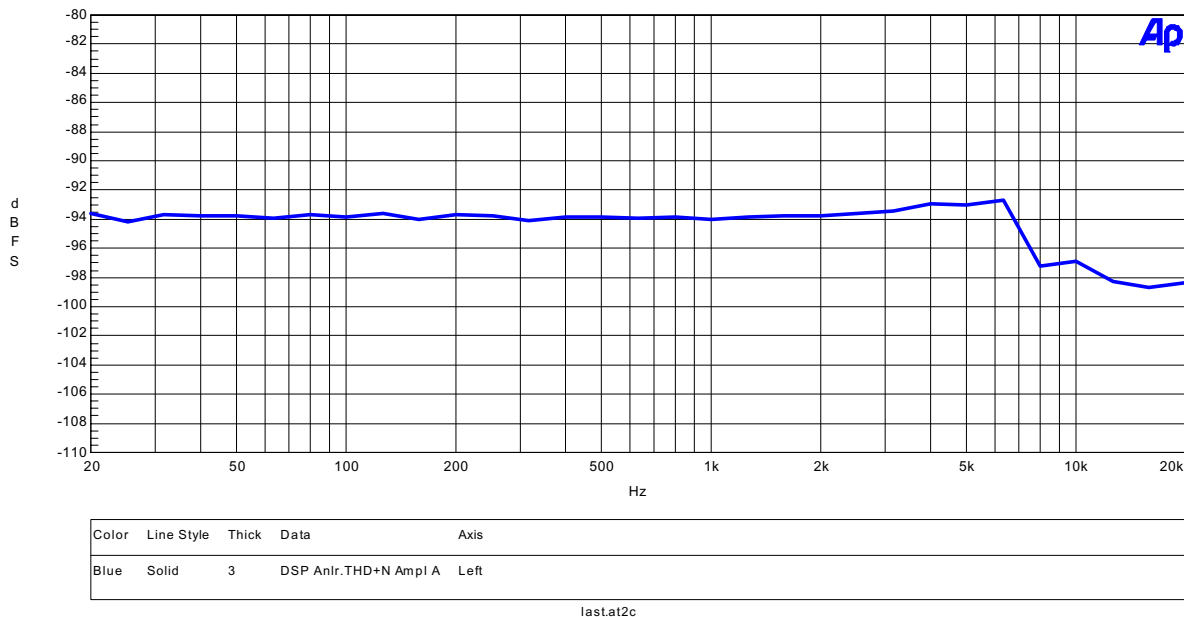


Figure 2. THD+N vs. Input Frequency

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AK4584 ADC Linearity
VDD=5.0V, fs=44.1kHz, fin=1kHz

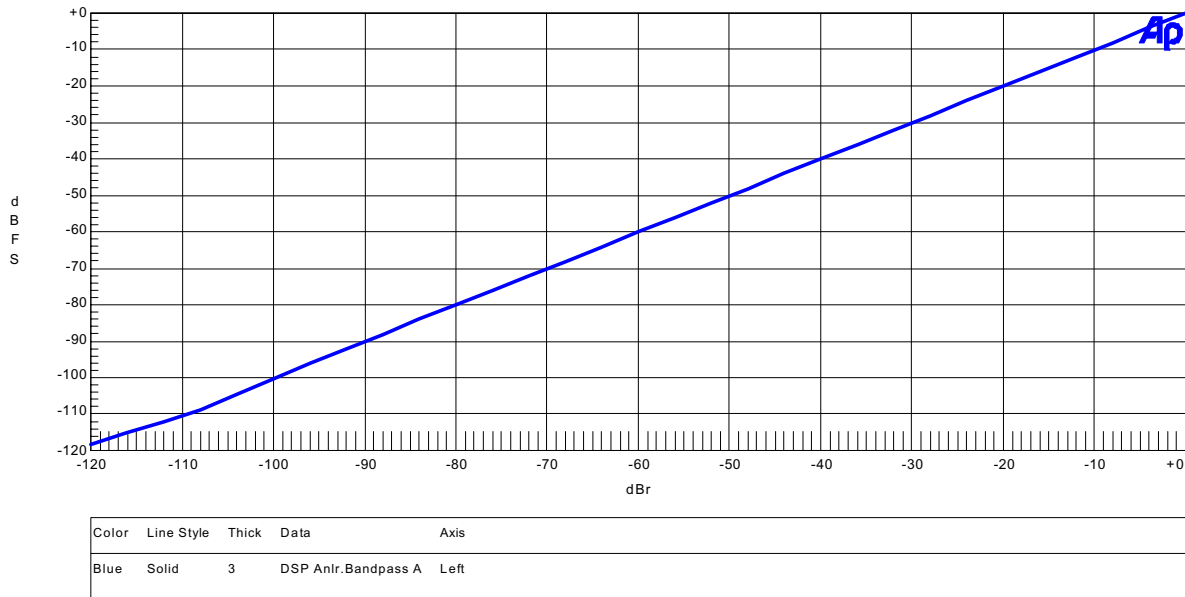


Figure 3. Linearity

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AK4584 ADC Frequency Response
VDD=5.0V, fs=44.1kHz, Input=-0.5dBr

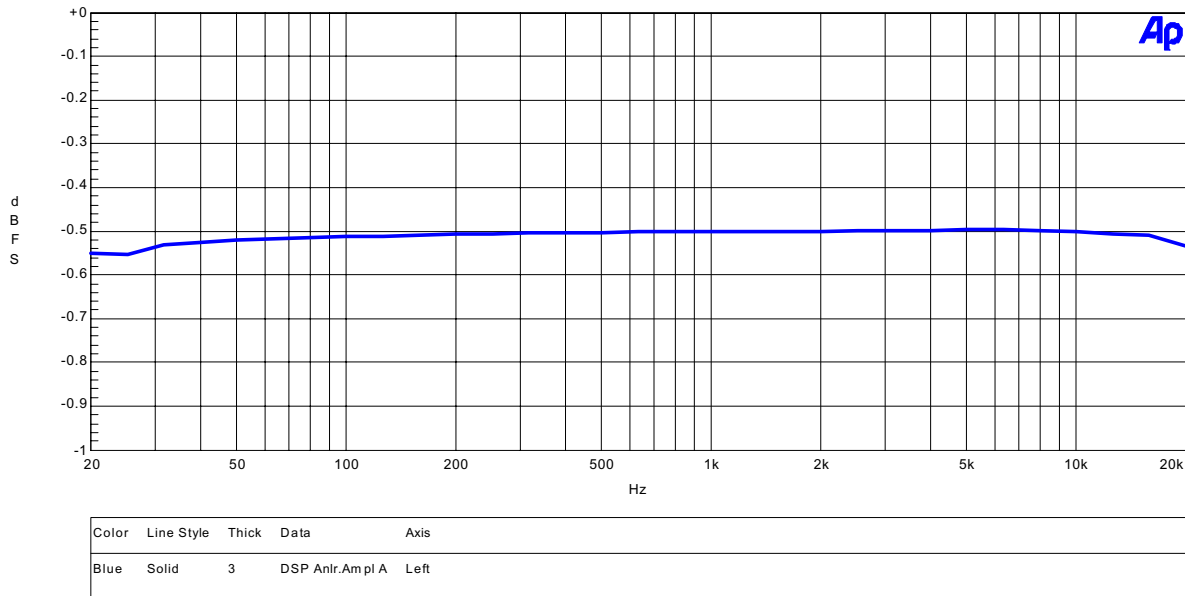


Figure 4. Frequency Response

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AK4584 ADC Crosstalk
VDD=5.0V, fs=44.1kHz, Input=-0.5dB

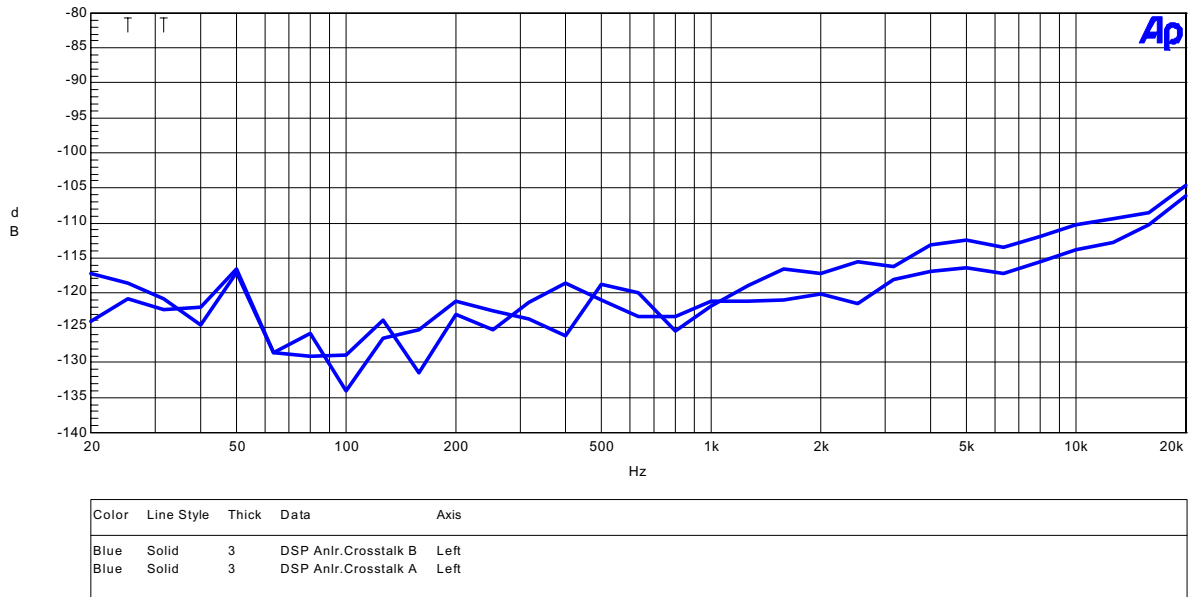


Figure 5. Crosstalk

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AK4584 ADC FFT Plot
VDD=5.0V, fs=44.1kHz, fin=1kHz, Input=-0.5dB

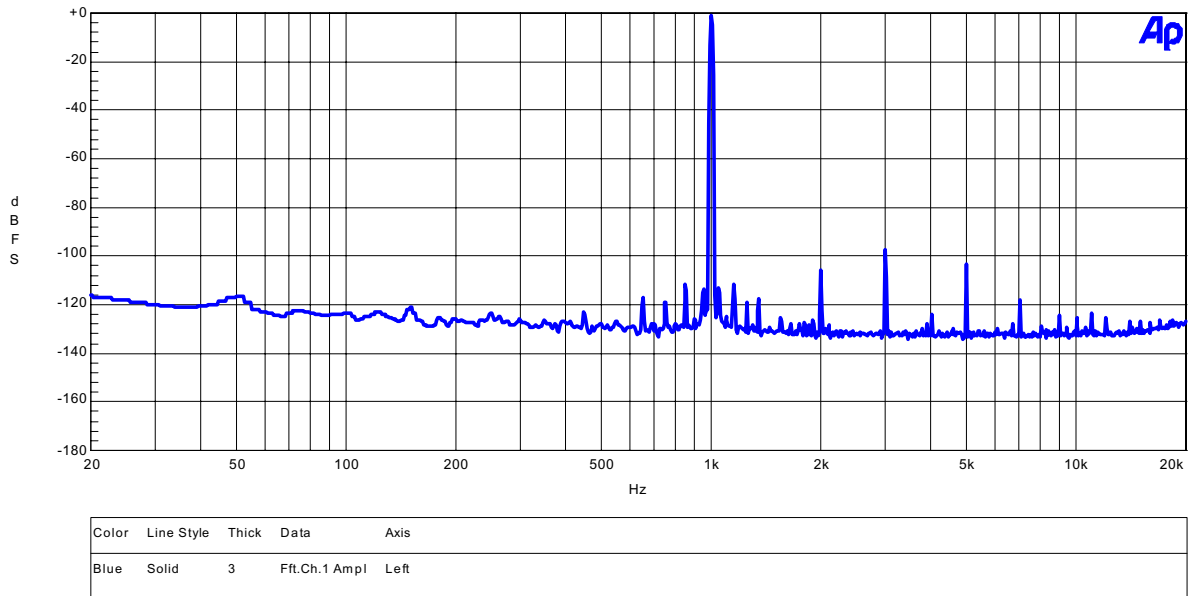


Figure 6. FFT Plot

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AK4584 ADC FFT Plot
VDD=5.0V, fs=44.1kHz, fin=1kHz, Input=-60dB

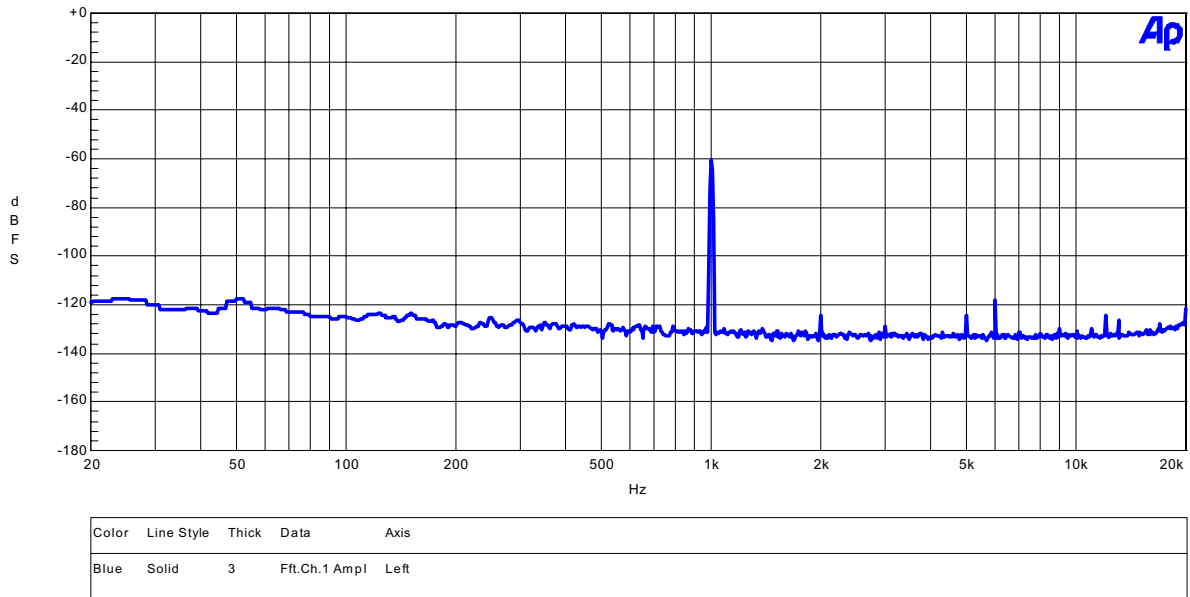


Figure 7. FFT Plot

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AK4584 ADC FFT Plot
VDD=5.0V, fs=44.1kHz, fin=None

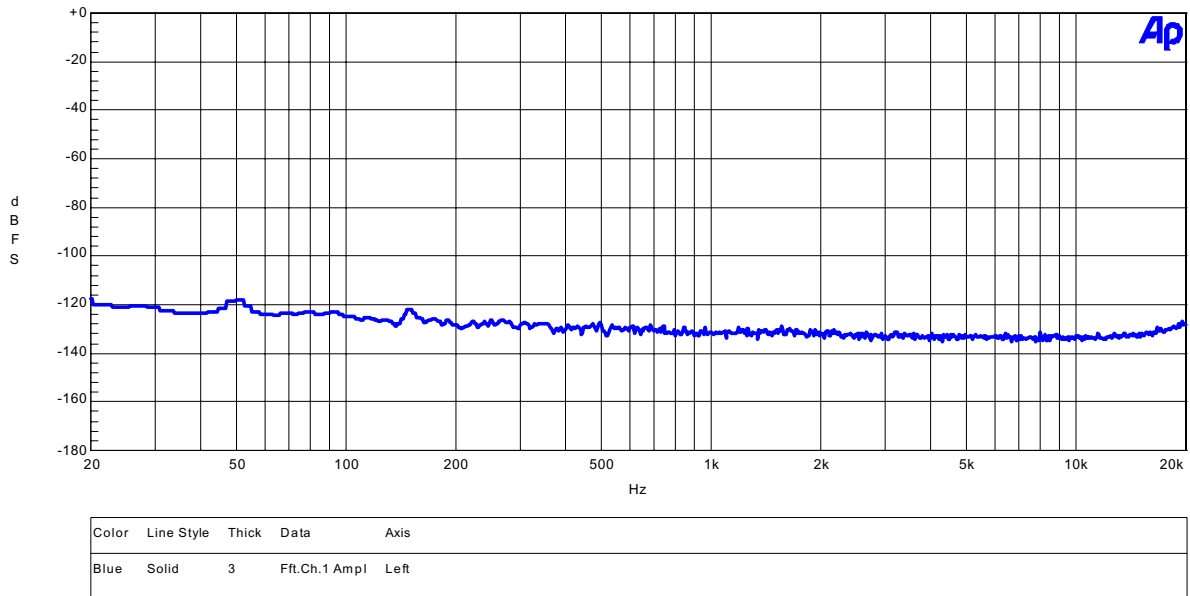
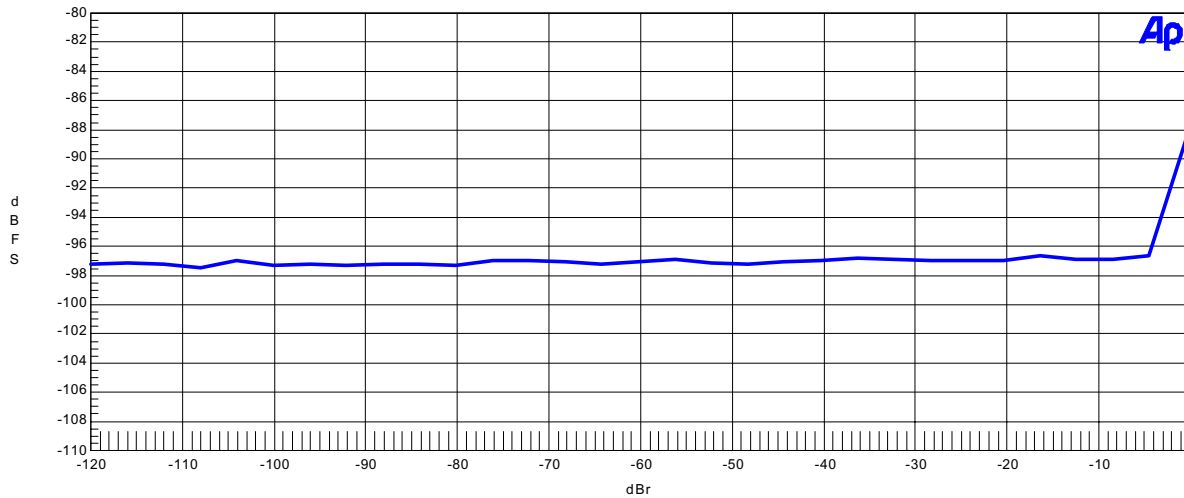


Figure 8. FFT Plot

[ADC Plot : fs=96kHz]

AKM

AK4584 ADC THD+N vs. Input Level
VDD=5.0V, fs=96kHz, fin=1kHz



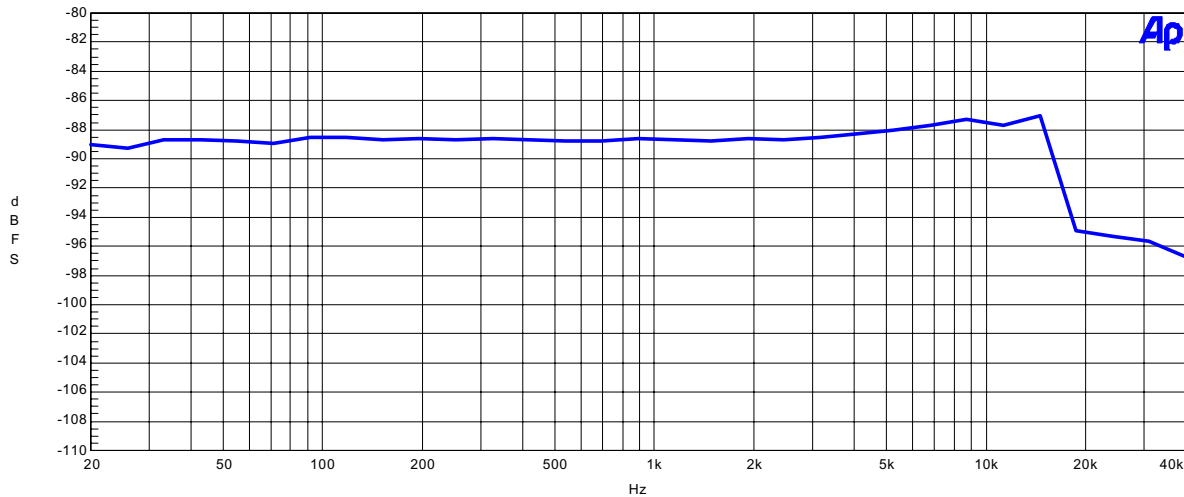
Color	Line Style	Thick	Data	Axis
Blue	Solid	3	DSP Anlr.TH+D+N Ampl A	Left

last.at2c

Figure 9. THD+N vs. Input Level

AKM

AK4584 ADC THD+N vs. Input Frequency
VDD=5.0V, fs=96kHz, Input=-0.5dBr



Color	Line Style	Thick	Data	Axis
Blue	Solid	3	DSP Anlr.TH+D+N Ampl A	Left

last.at2c

Figure 10. THD+N vs. Input Frequency

AKM

AK4584 ADC Linearity
 VDD=5.0V, fs=96kHz, fin=1kHz

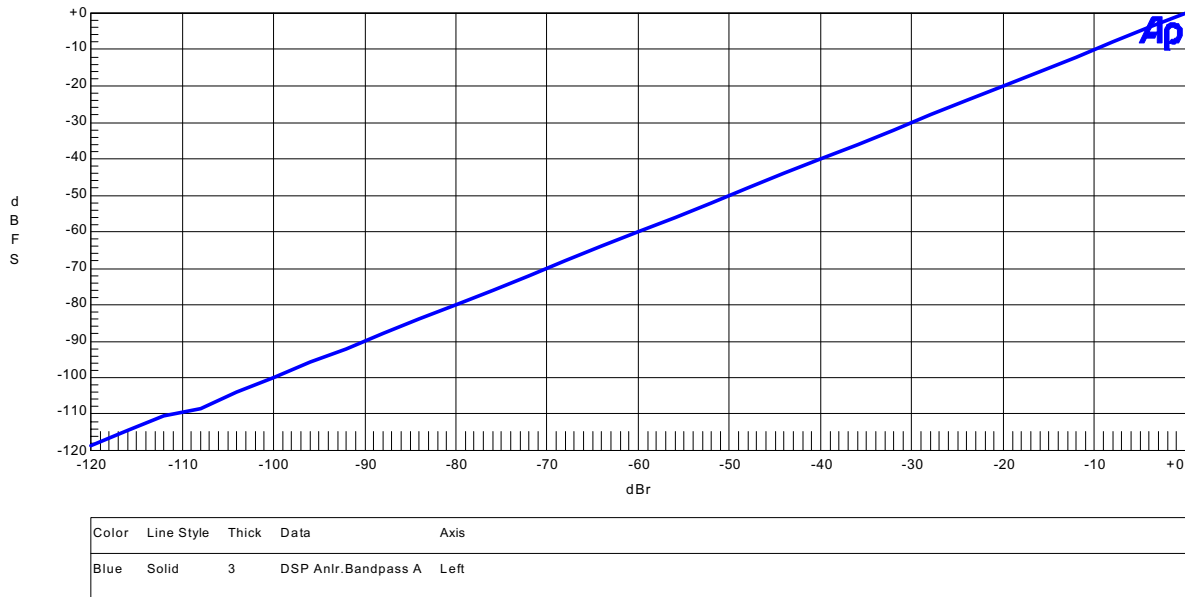


Figure 11. Linearity

AKM

AK4584 ADC Frequency Response
 VDD=5.0V, fs=96kHz, Input=-0.5dBr

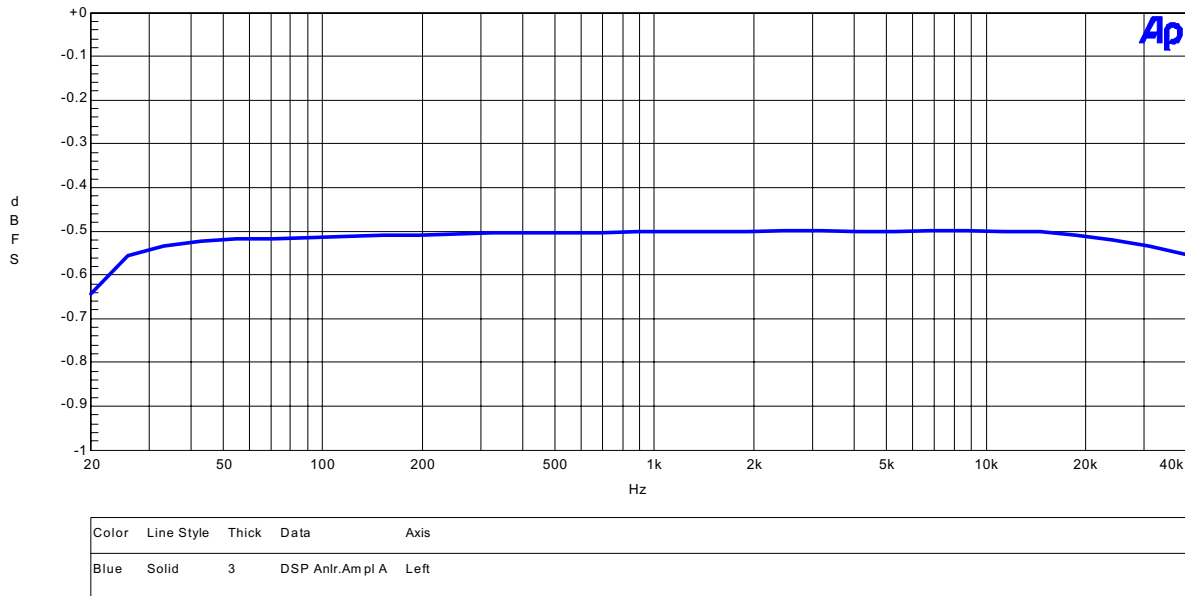


Figure 12. Frequency Response

AKM

AK4584 ADC Crosstalk
 VDD=5.0V, fs=96kHz, Input=-0.5dBr

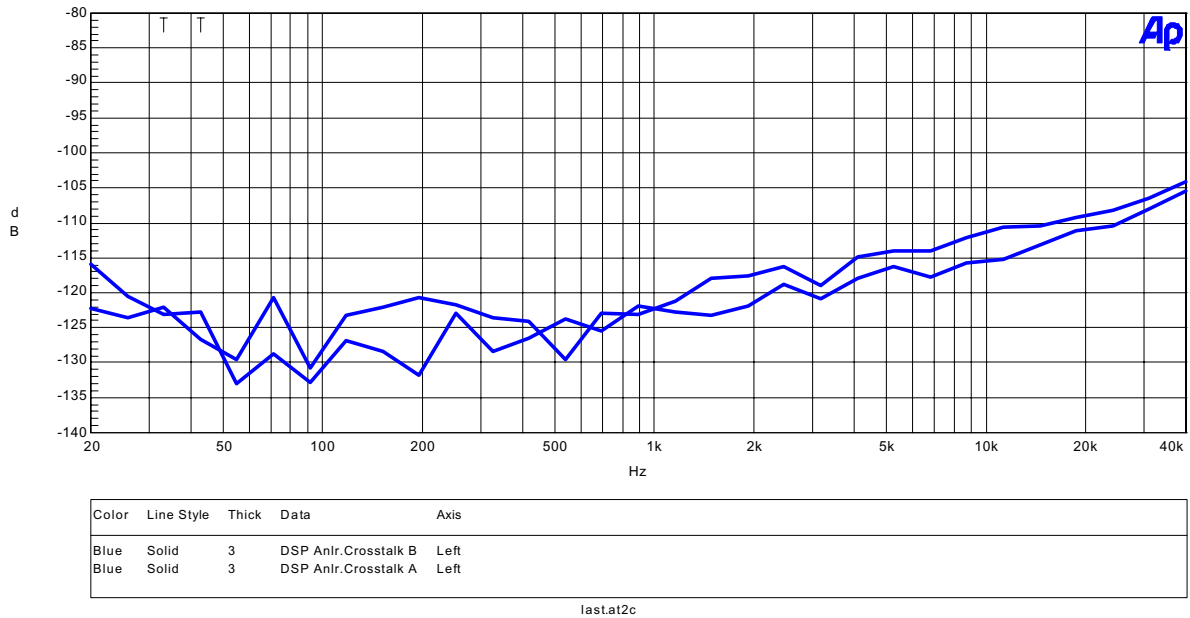


Figure 13. Crosstalk

AKM

AK4584 ADC FFT Plot
 VDD=5.0V, fs=96kHz, fin=1kHz, Input=-0.5dBr

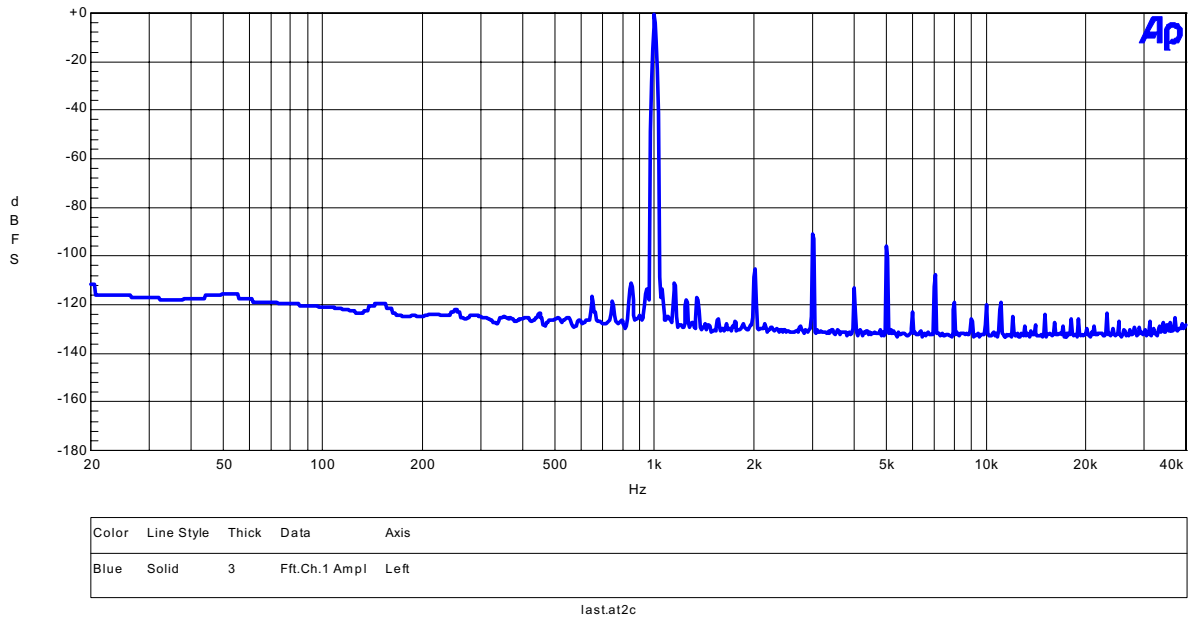


Figure 14. FFT Plot

AKM

AK4584 ADC FFT Plot
VDD=5.0V, fs=96kHz, fin=1kHz, Input=-60dB

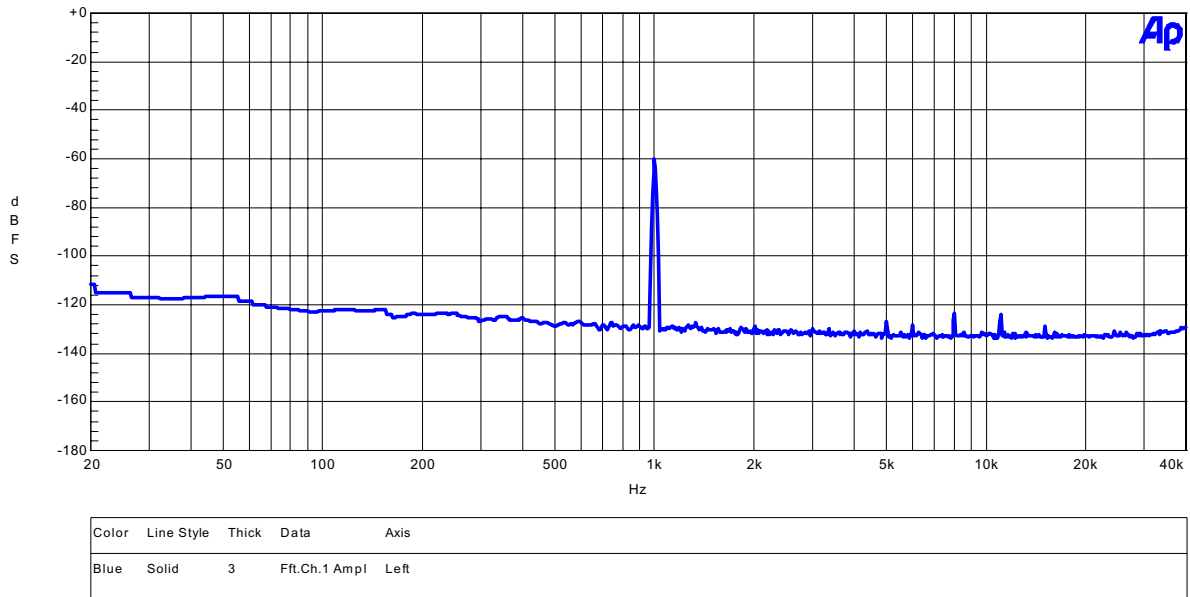


Figure 15. FFT Plot

AKM

AK4584 ADC FFT Plot
VDD=5.0V, fs=96kHz, fin=None

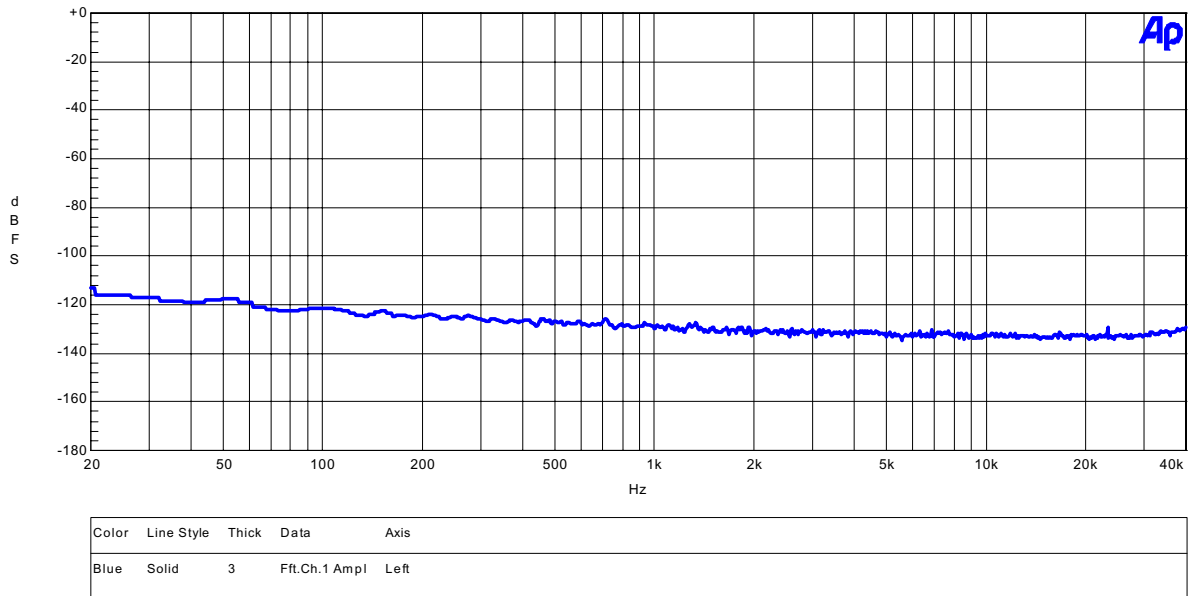


Figure 16. FFT Plot

[DAC Plot : fs=44.1kHz]

AKM

AK4584 DAC THD+N vs. Input Level
VDD=5.0V, fs=44.1kHz, fin=1kHz

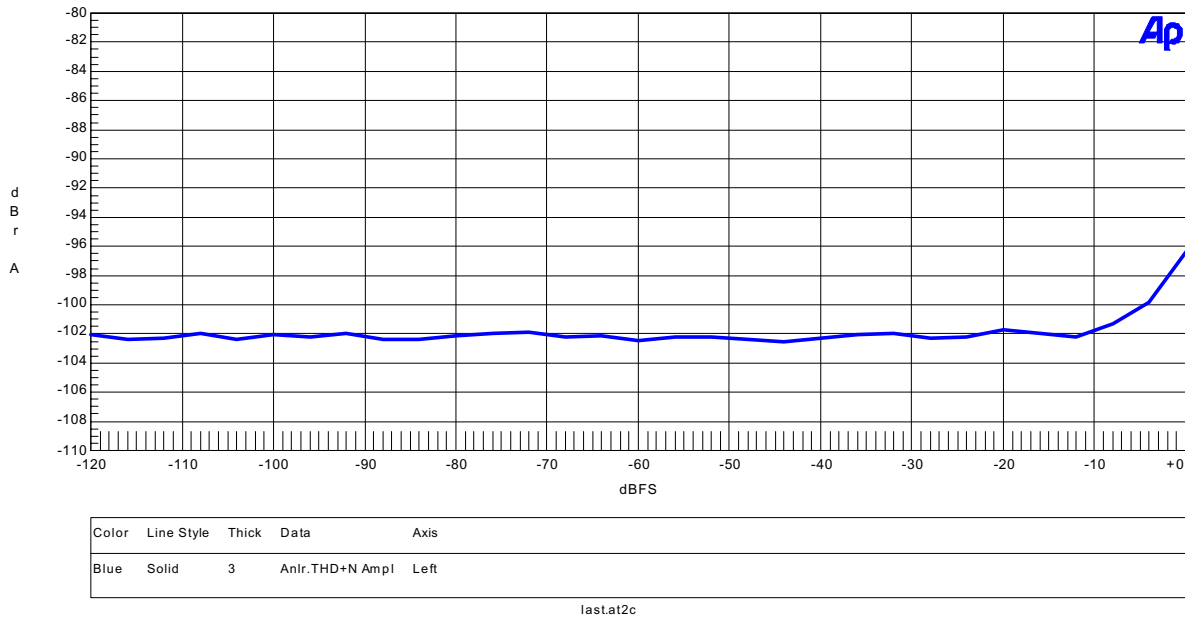


Figure 1. THD+N vs. Input Level

AKM

AK4584 DAC THD+N vs. Input Frequency
VDD=5.0V, fs=44.1kHz, Input=0dBFS

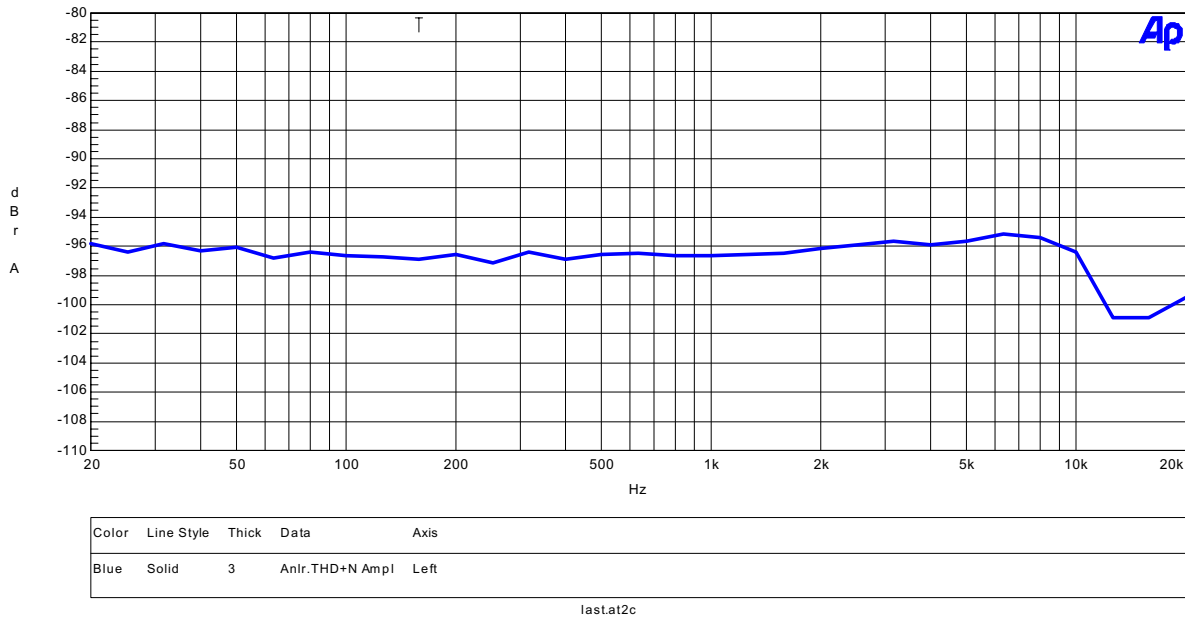


Figure 2. THD+N vs. Input Frequency

AKM

AK4584 DAC Linearity
VDD=5.0V, fs=44.1kHz, fin=1kHz



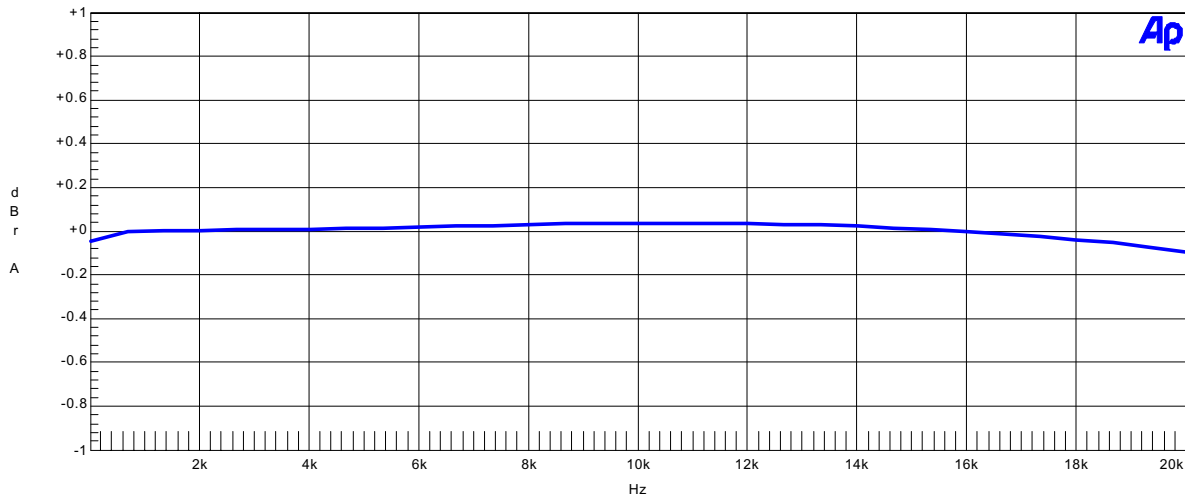
Color	Line Style	Thick	Data	Axis
Blue	Solid	3	Anlr.Bandpass	Left

last.at2c

Figure 3. Linearity

AKM

AK4584 DAC Frequency Response
VDD=5.0V, fs=44.1kHz, Input=0dBFS



Color	Line Style	Thick	Data	Axis
Blue	Solid	3	Anlr.Ampl	Left

last.at2c

Figure 4. Frequency Response

AKM

AK4584 DAC Crosstalk
 VDD=5.0V, fs=44.1kHz, Input=0dBFS

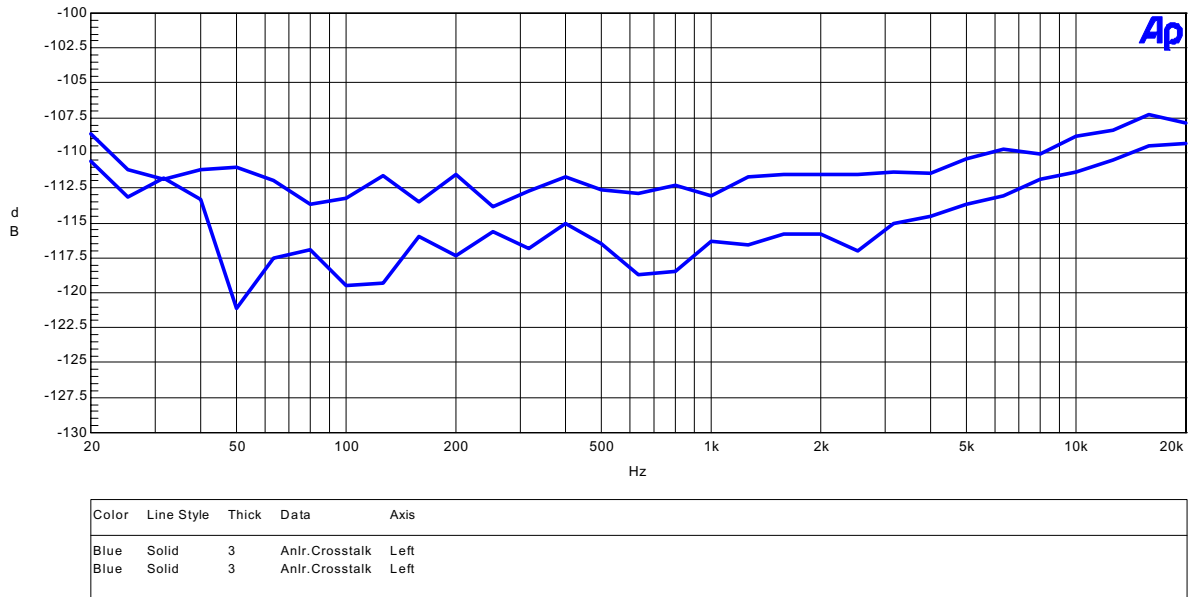


Figure 5. Crosstalk

AKM

AK4584 DAC FFT Plot
 VDD=5.0V, fs=44.1kHz, fin=1kHz, Input=0dBFS

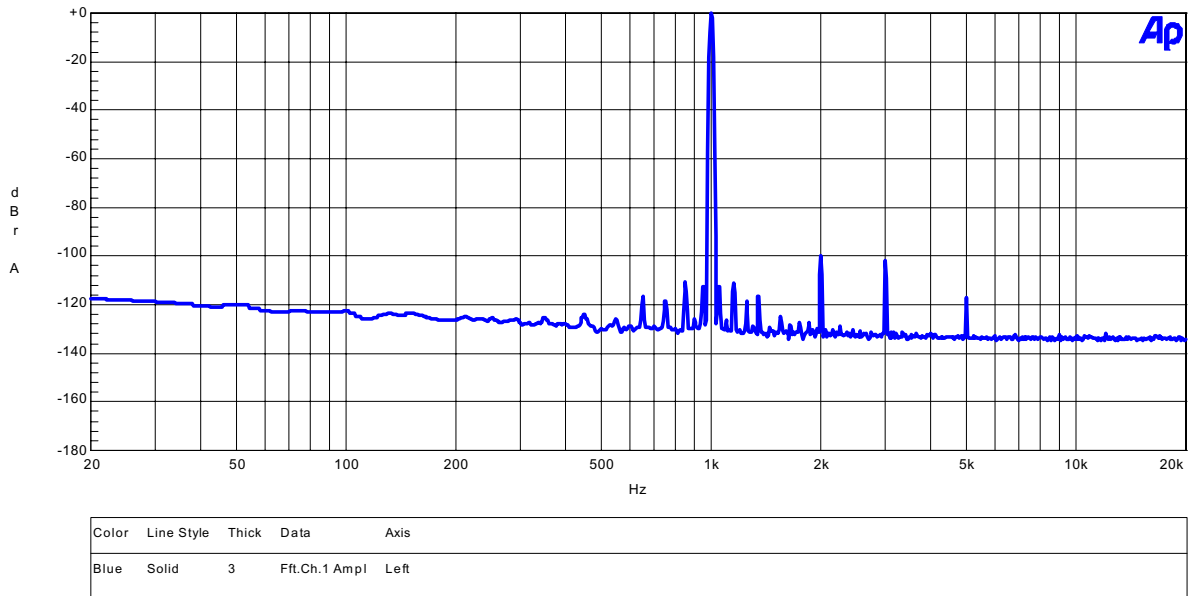


Figure 6. FFT Plot

AKM

AK4584 DAC FFT Plot
VDD=5.0V, fs=44.1kHz, fin=1kHz, Input=-60dBFS

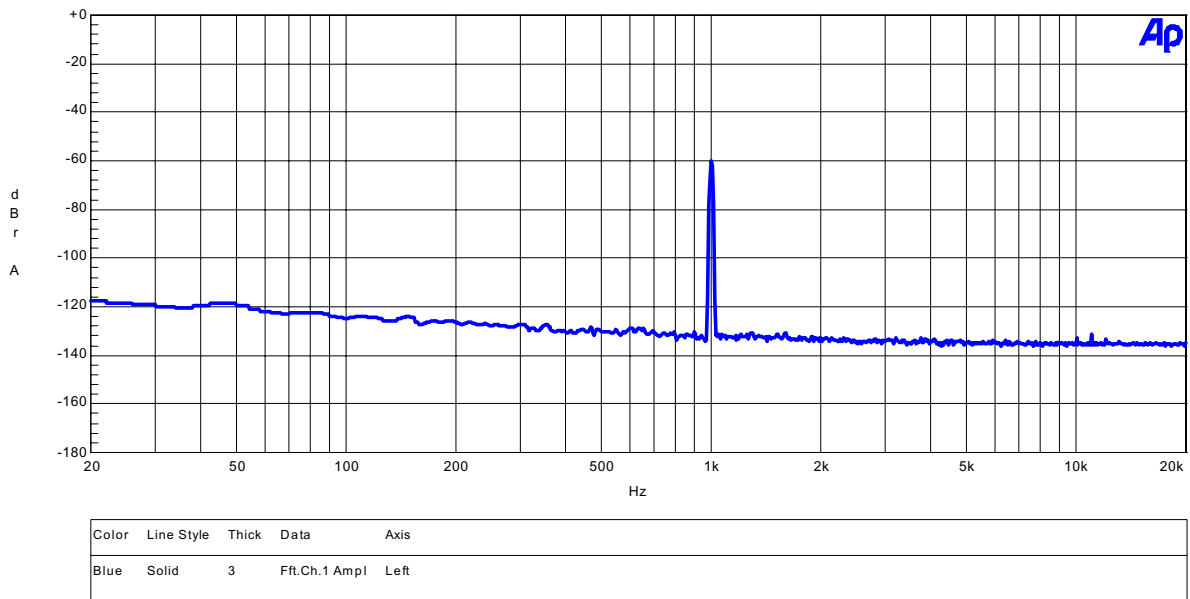


Figure 7. FFT Plot

AKM

AK4584 DAC FFT Plot
VDD=5.0V, fs=44.1kHz, fin=None

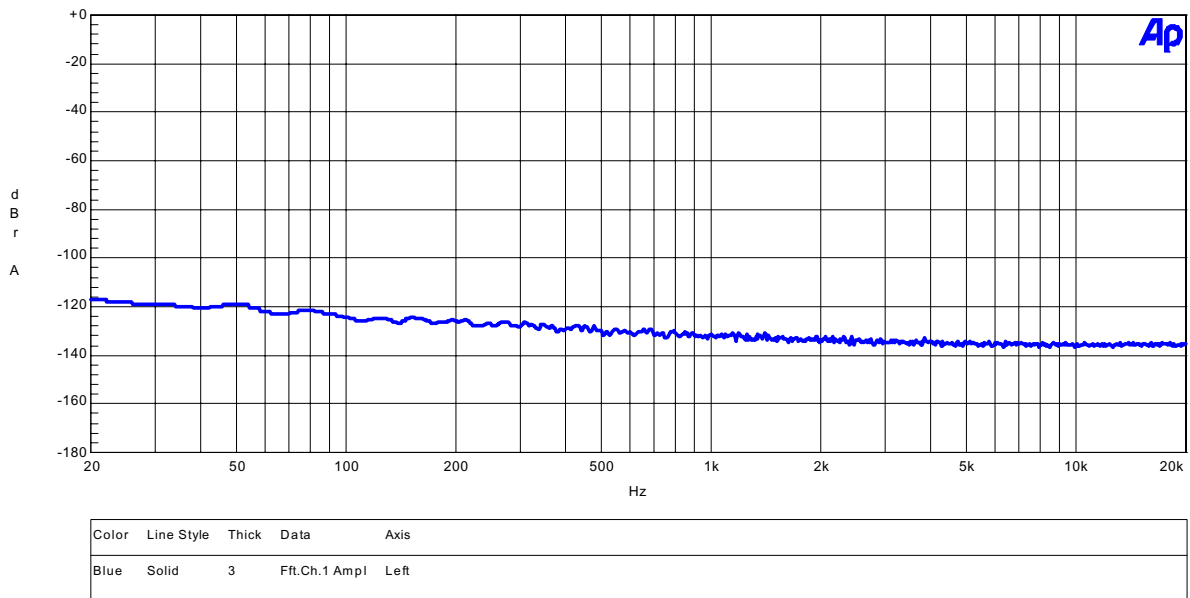
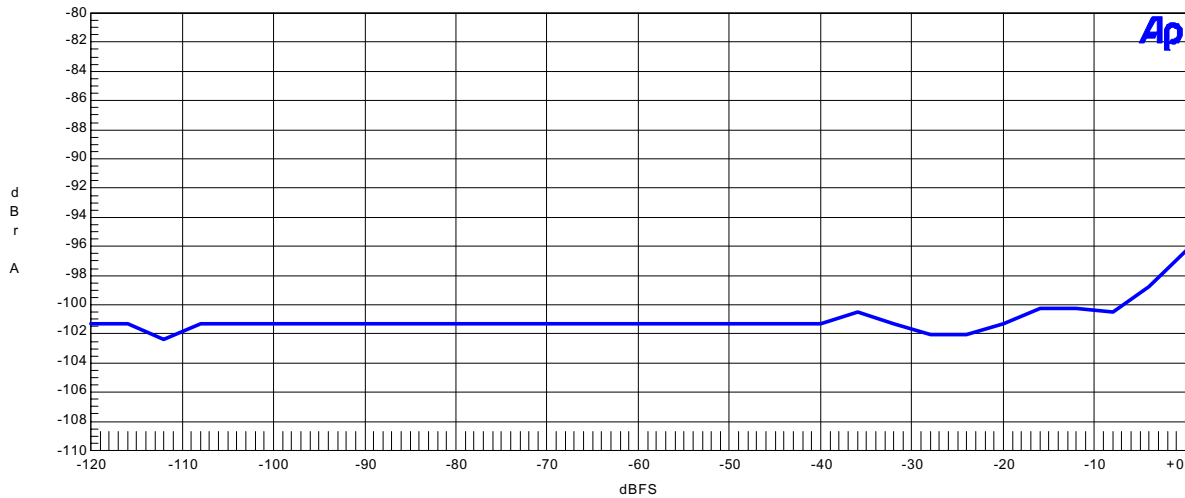


Figure 8. FFT Plot

[DAC Plot : fs=96kHz]

AKM

AK4584 DAC THD+N vs. Input Level
VDD=5.0V, fs=96kHz, fin=1kHz



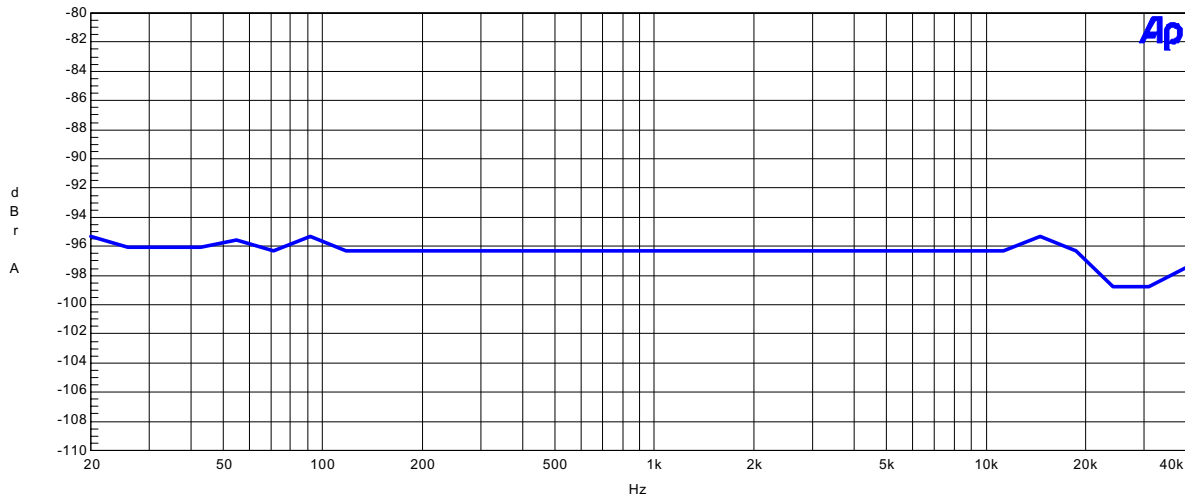
Color	Line Style	Thick	Data	Axis
Blue	Solid	3	Anlr.TH+D+N Ampl	Left

last.at2c

Figure 9. THD+N vs. Input Level

AKM

AK4584 DAC THD+N vs. Input Frequency
VDD=5.0V, fs=96kHz, Input=0dBFS



Color	Line Style	Thick	Data	Axis
Blue	Solid	3	Anlr.TH+D+N Ampl	Left

last.at2c

Figure 10. THD+N vs. Input Frequency

AKM

AK4584 DAC Frequency Response
VDD=5.0V, fs=96kHz, fin=1kHz

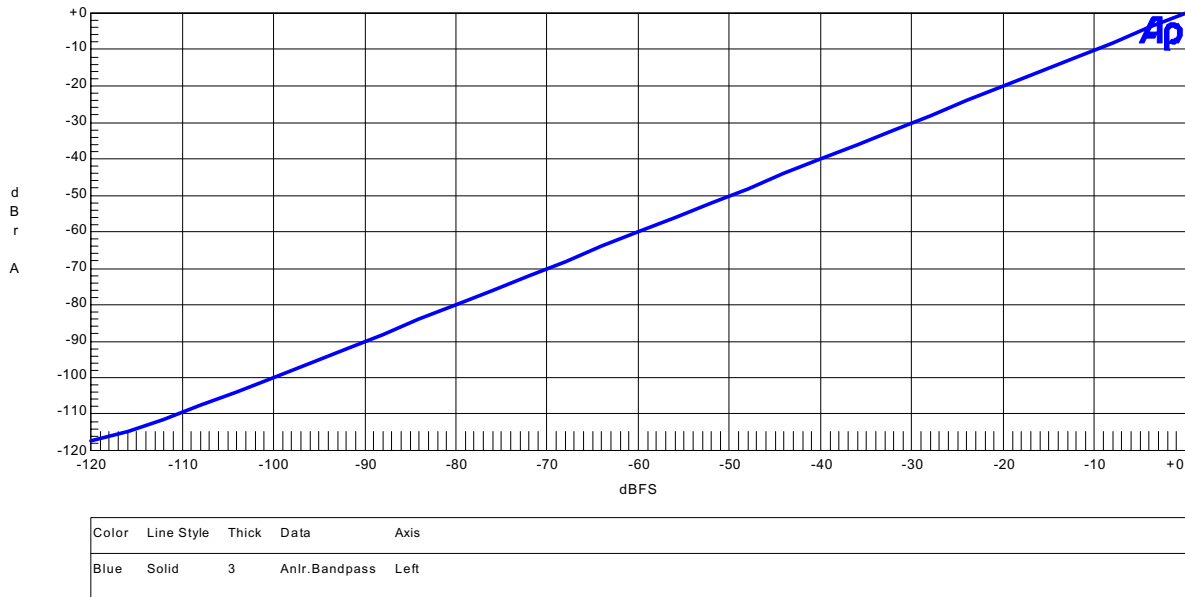


Figure 11. Linearity

AKM

AK4584 DAC Frequency Response
VDD=5.0V, fs=96kHz, Input=0dBFS

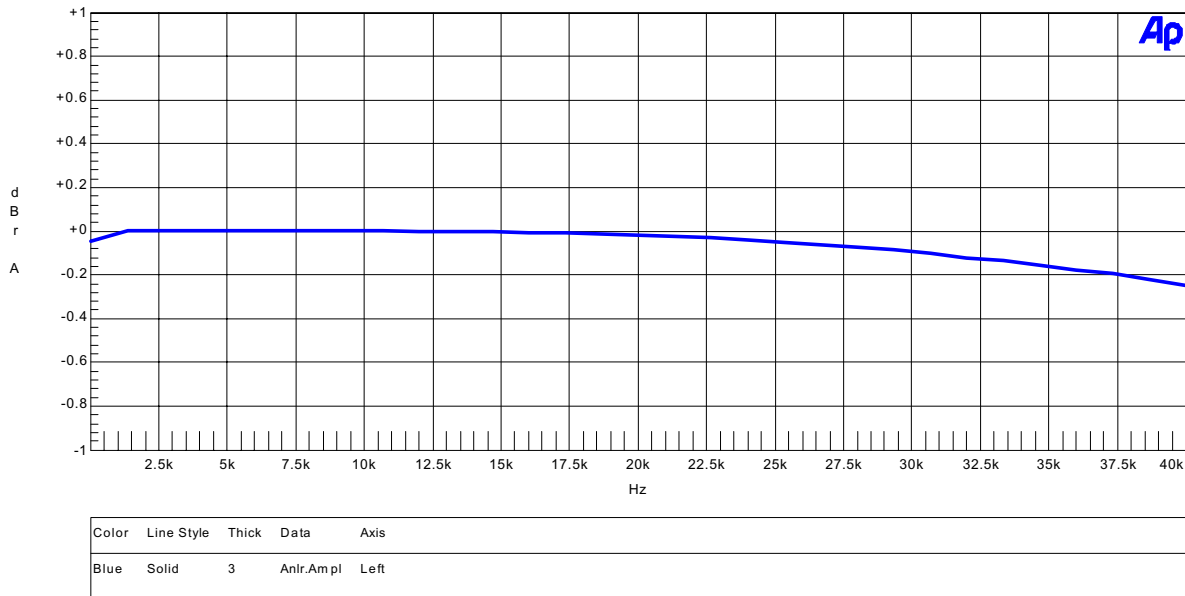


Figure 12. Frequency Response

AKM

AK4584 DAC Crosstalk
VDD=5.0V, fs=96kHz, Input=0dBFS

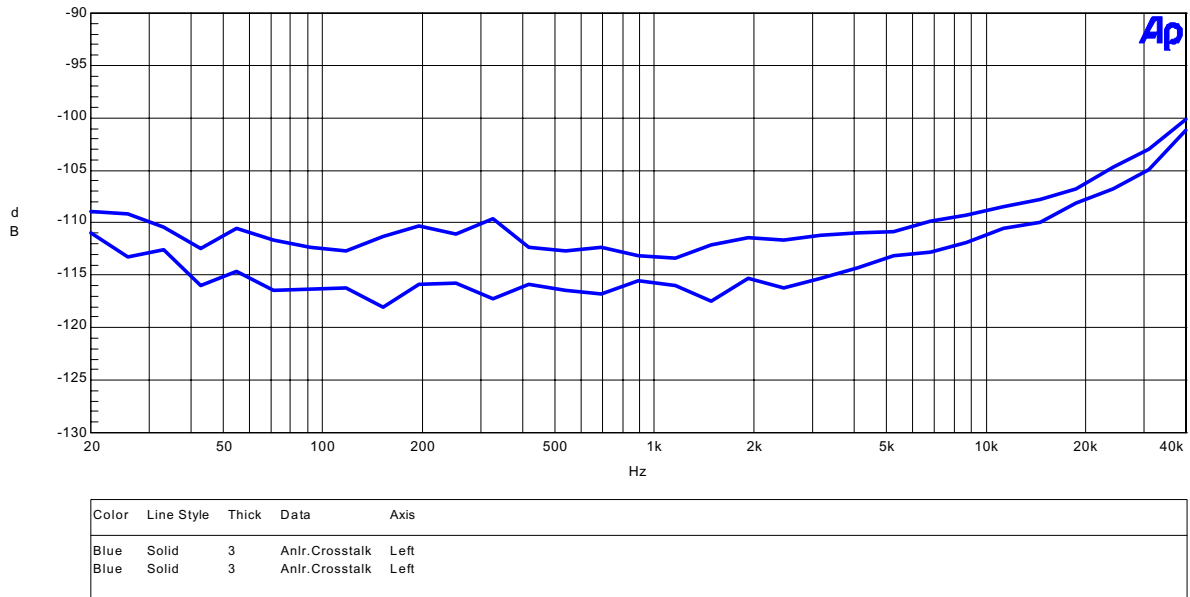


Figure 13. Crosstalk

AKM

AK4584 DAC FFT Plot
VDD=5.0V, fs=96kHz, fin=1kHz, Input=0dBFS

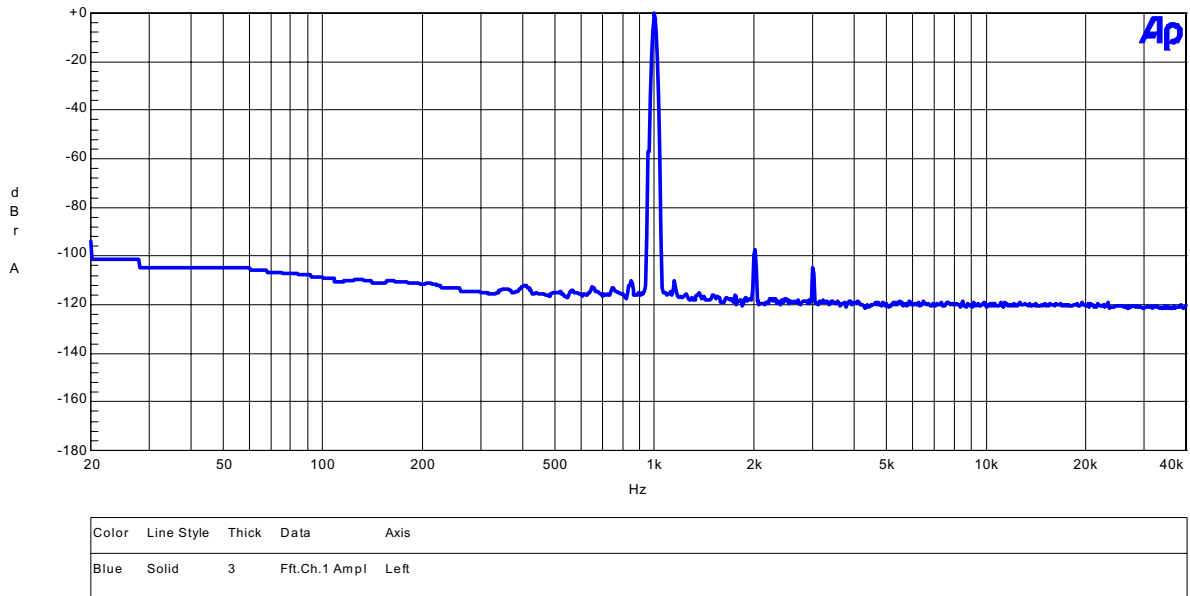


Figure 14. FFT Plot

AKM

AK4584 DAC FFT Plot
VDD=5.0V, fs=96kHz, fin=1kHz, Input=-60dBFS

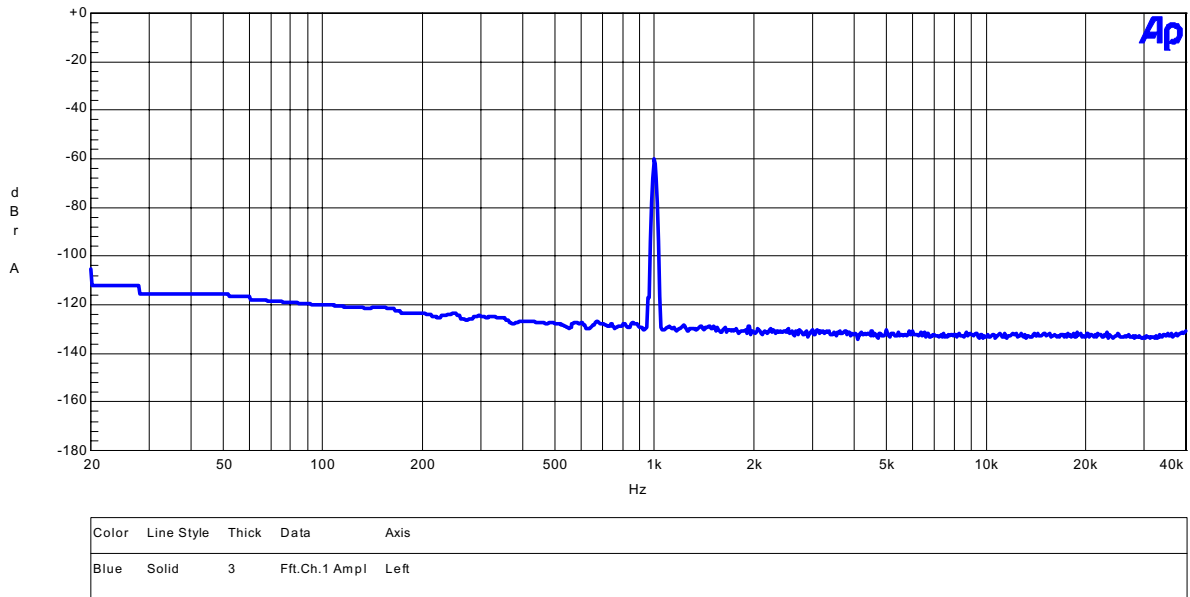


Figure 15. FFT Plot

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AK4584 DAC FFT Plot
VDD=5.0V, fs=96kHz, fin=None

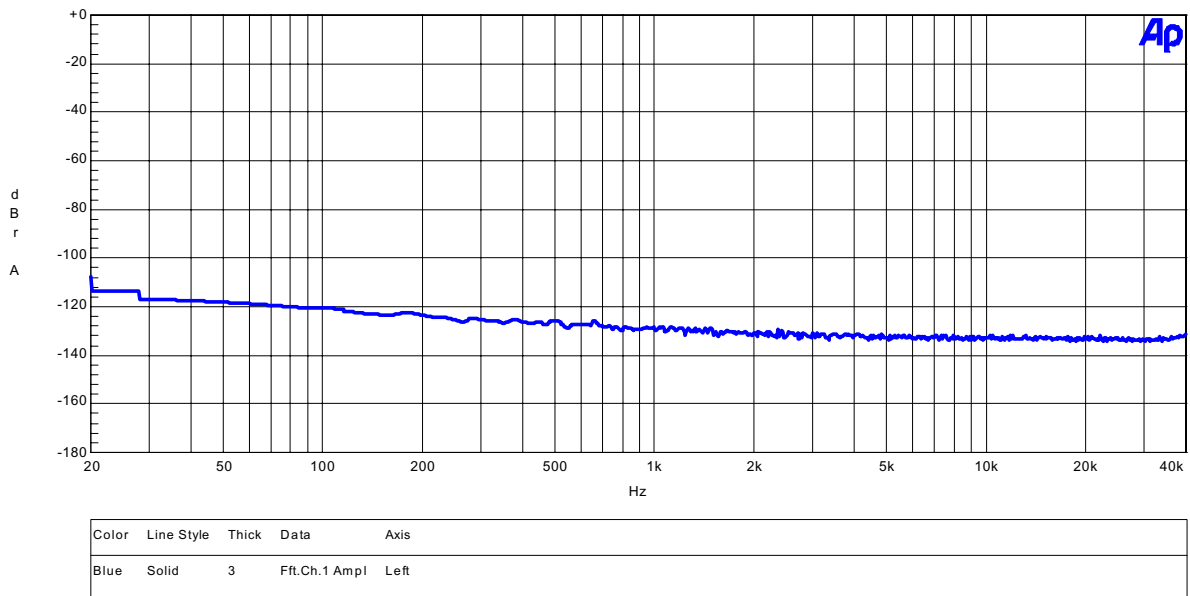


Figure 16. FFT Plot

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AK4584 DAC FFT Plot
VDD=5.0V, fs=44.1kHz, fin=None

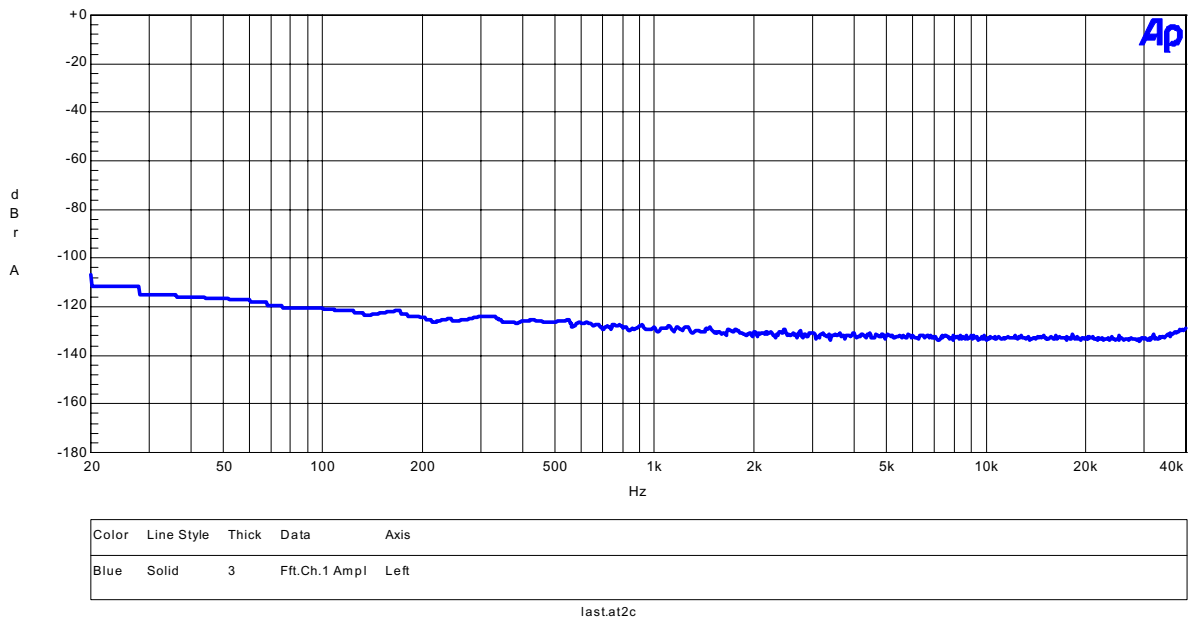


Figure 17. Outband Noise (fs=44.1kHz)

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AK4584 DAC FFT Plot
VDD=5.0V, fs=96kHz, fin=None

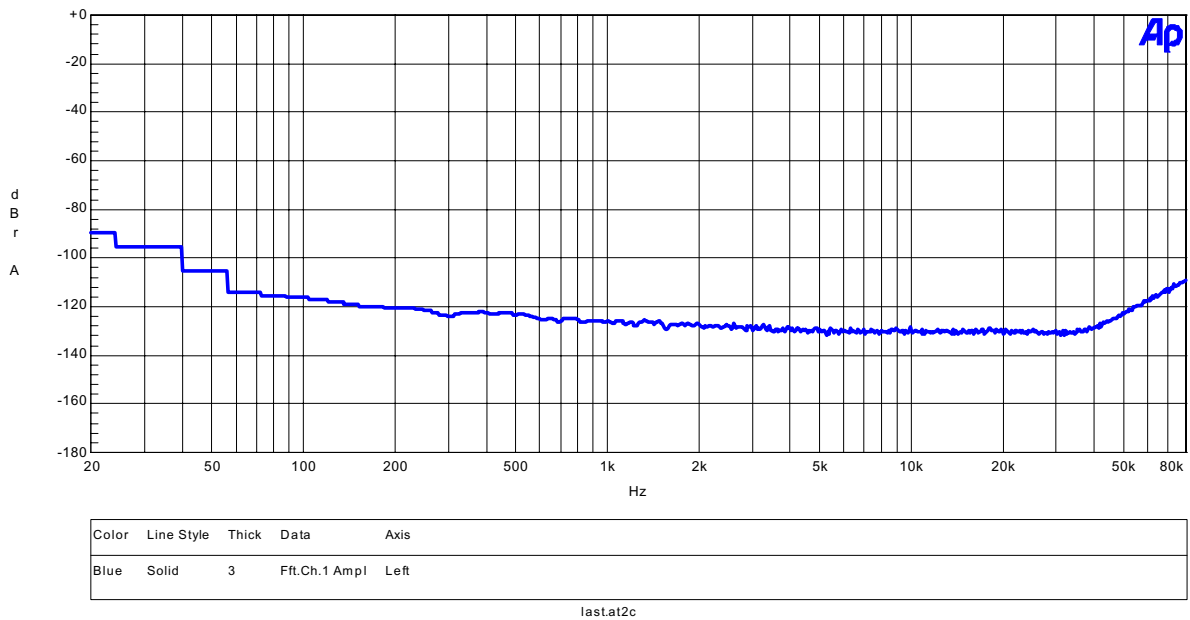
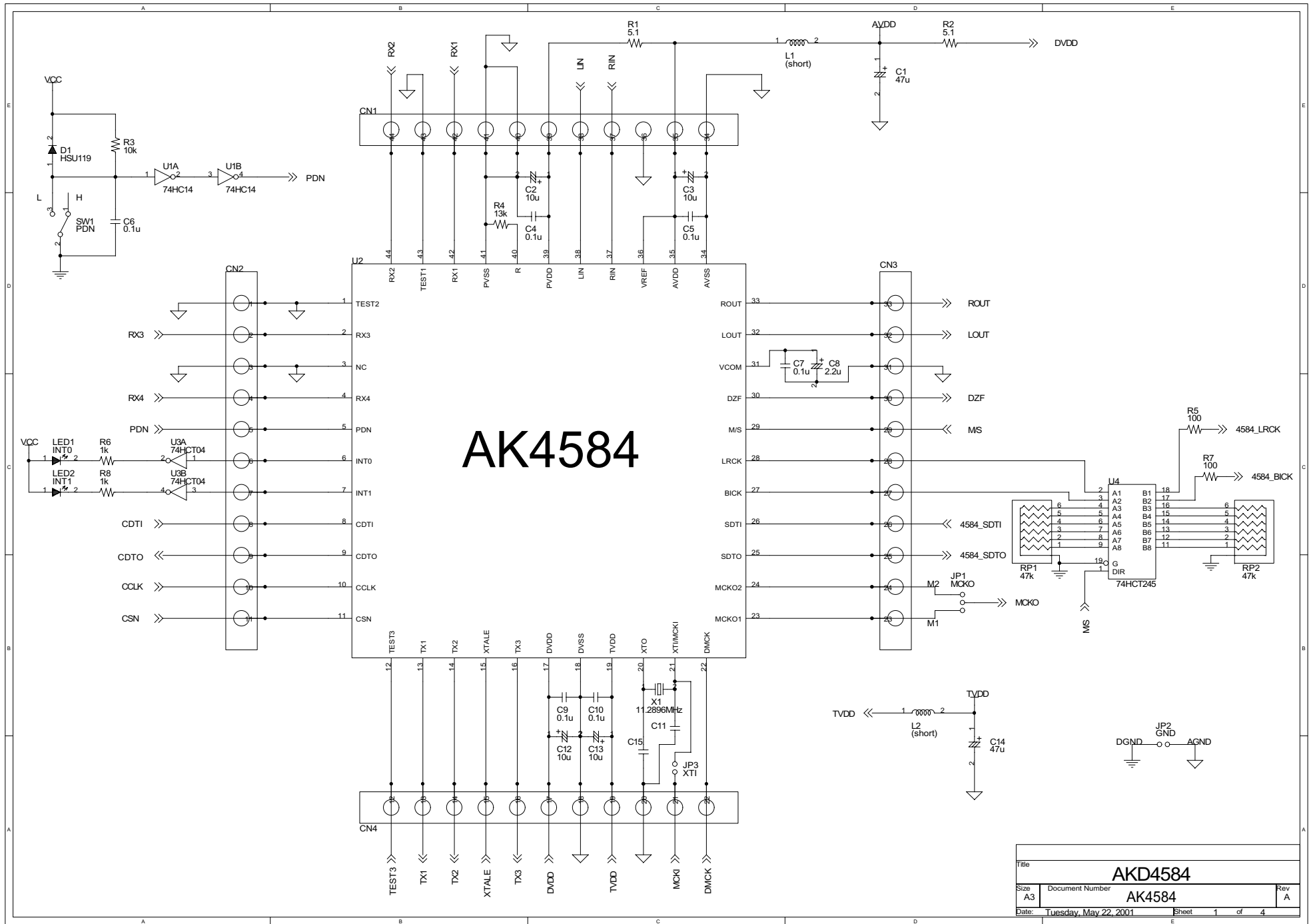


Figure 18. Outband Noise (fs=96kHz)

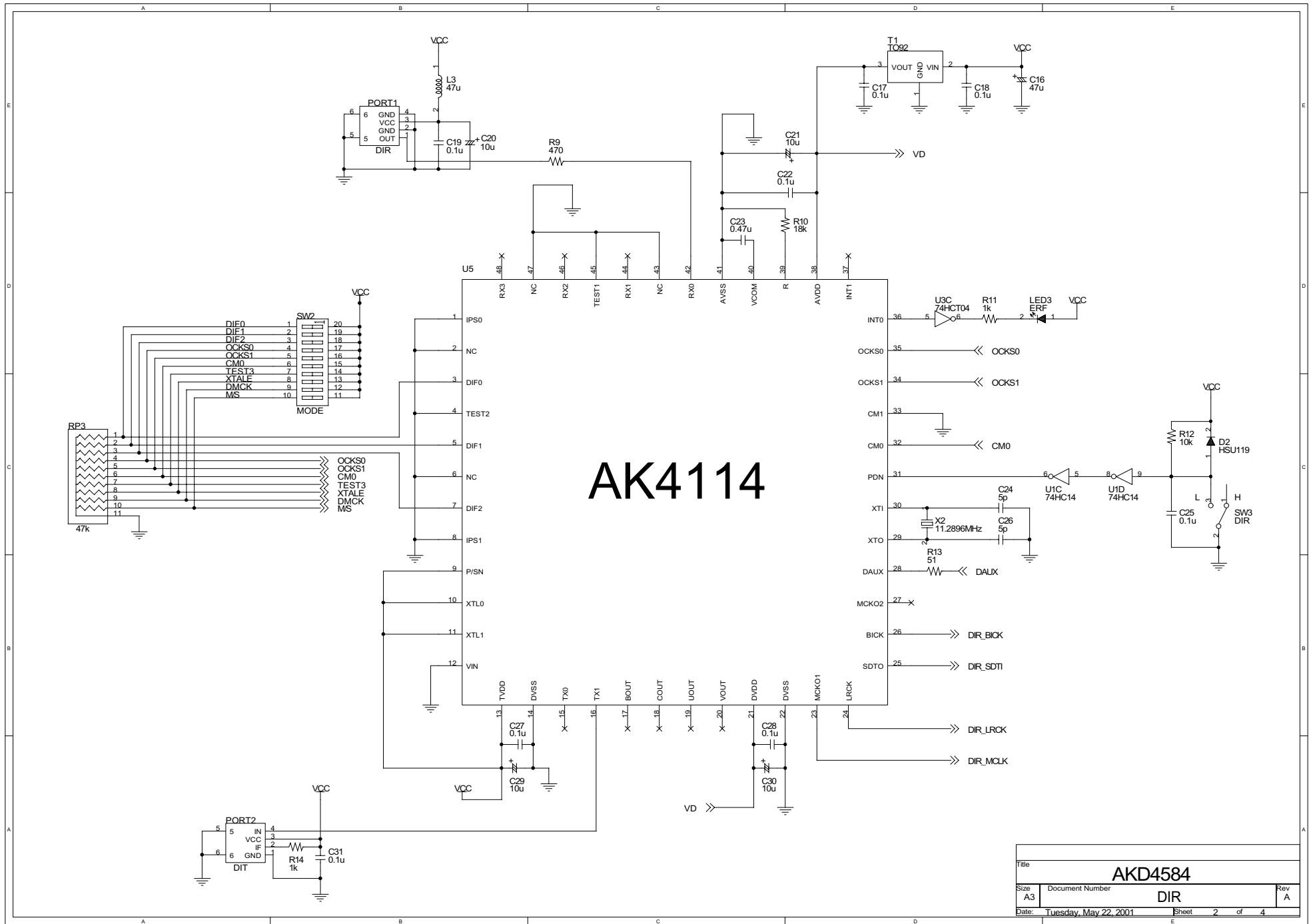
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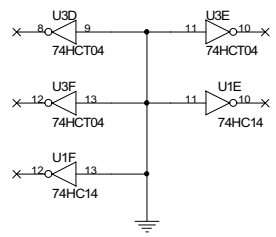
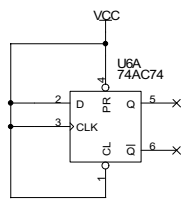
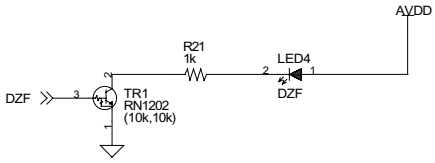
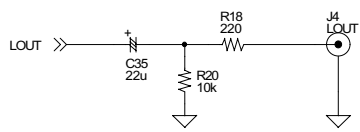
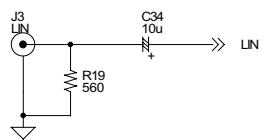
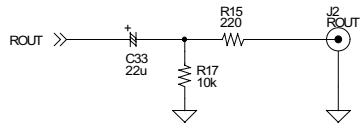
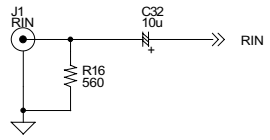
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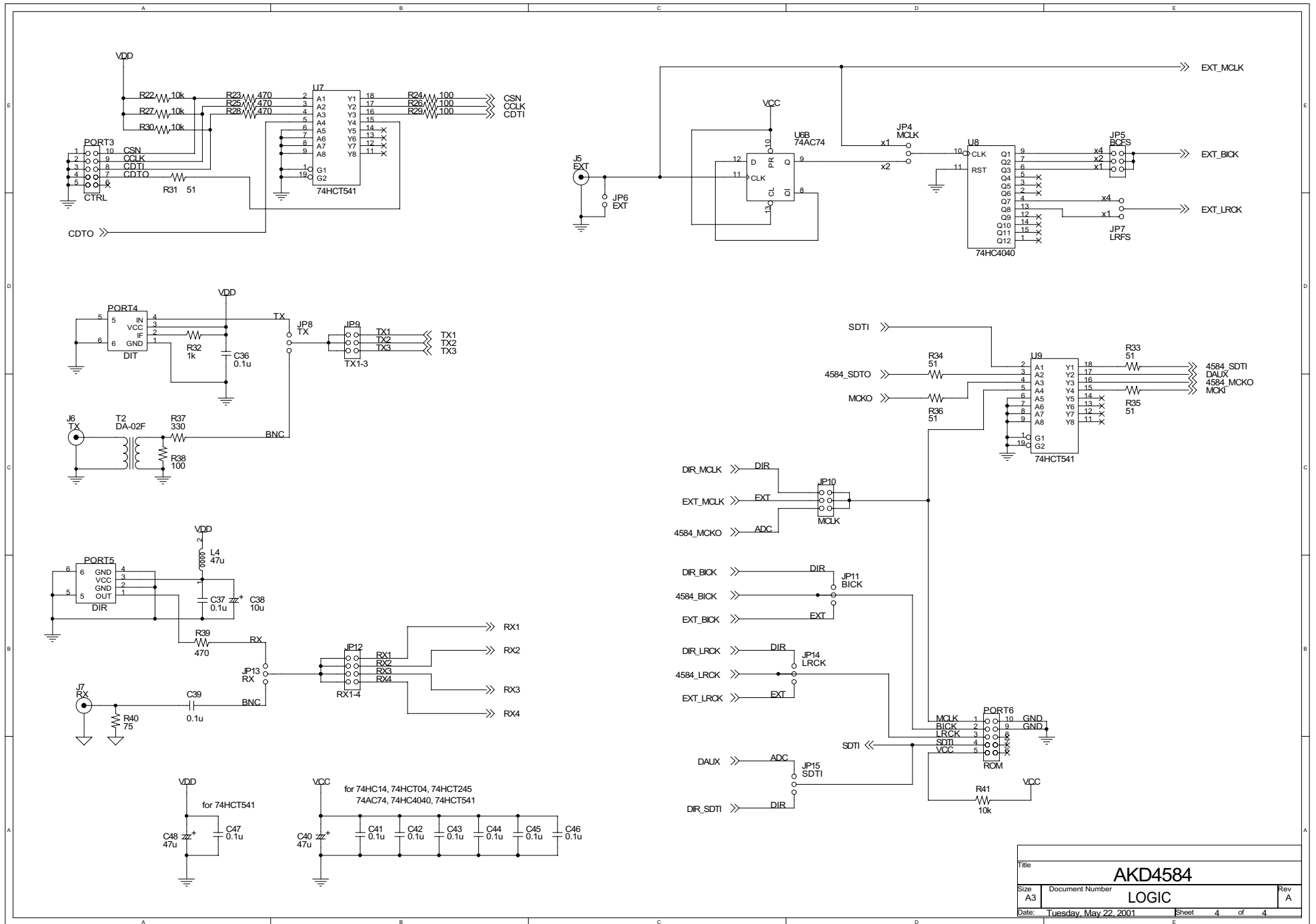


AK4114

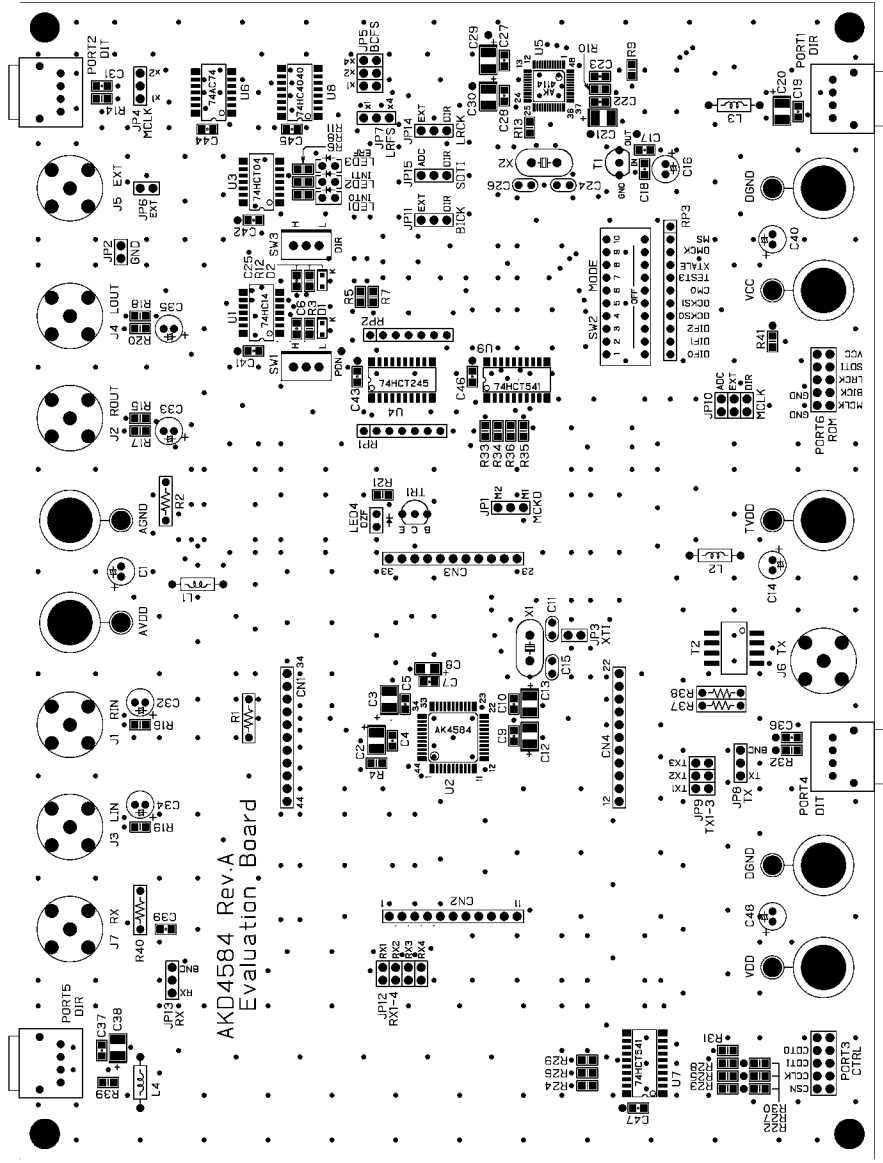
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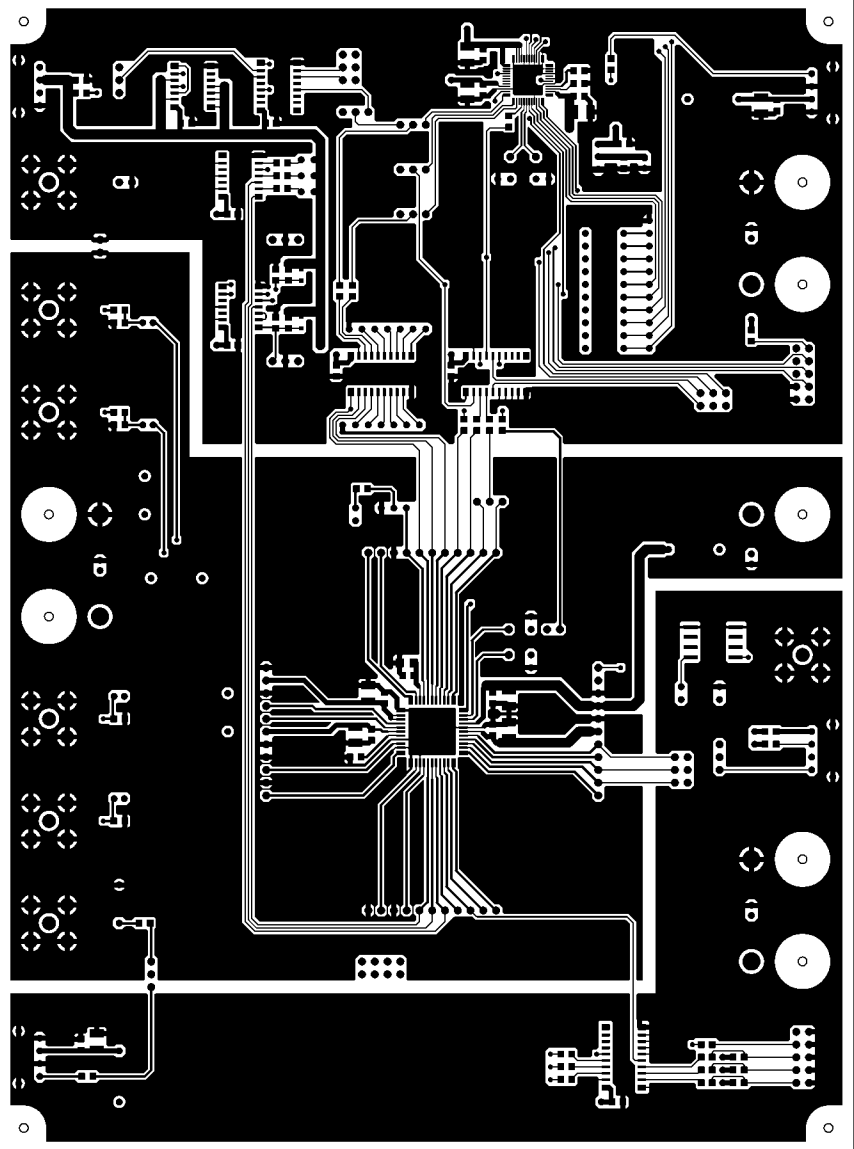


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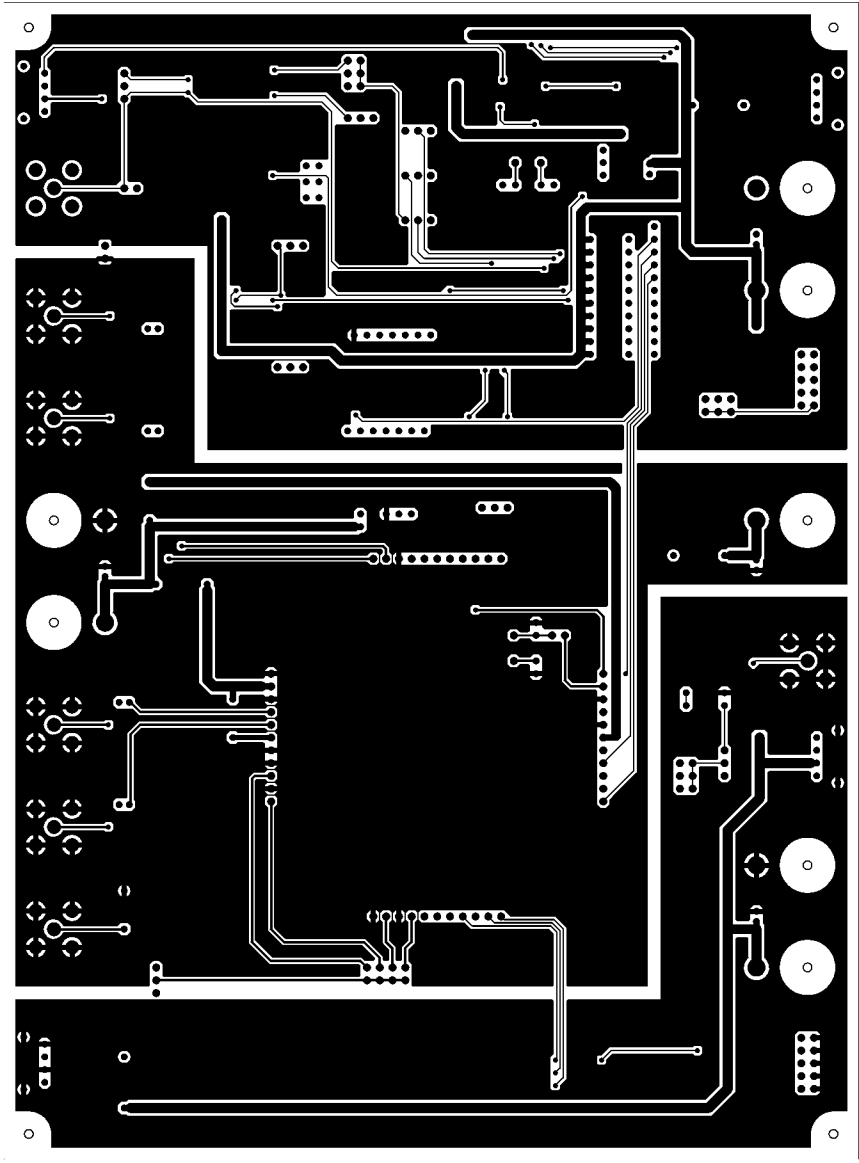


AKD4584 Rev.A
Evaluation Board

AKD4584 Rev.A L1 SR SILK



AKD4584 Rev.A L1



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