AKD4393
Evaluation board Rev.C for AK4393

General Description

The AKD4393 is an evaluation board for AK4393, which is 96kHz sampling 24Bit ΔΣ DAC. The AKD4393 includes a LPF which can add differential analog outputs from the AK4393 and also has a digital interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards. Therefore, it is easy to evaluate the AK4393.

■ **Ordering Guide**

AKD4393 Rev.C --- Evaluation board Rev.C for AK4393: differential output

Function

- On-board differential output buffer circuit
- On-board clock generator
- BNC connector for an external clock input
- Compatible with 3types of interface

1. Direct interface with evaluation boards for AKM's A/D converter (AKD539X, AKD535X)
2. Interface with a signal generator (AKD43XX)
3. On-board CS8414 as DIR which accepts optical input.

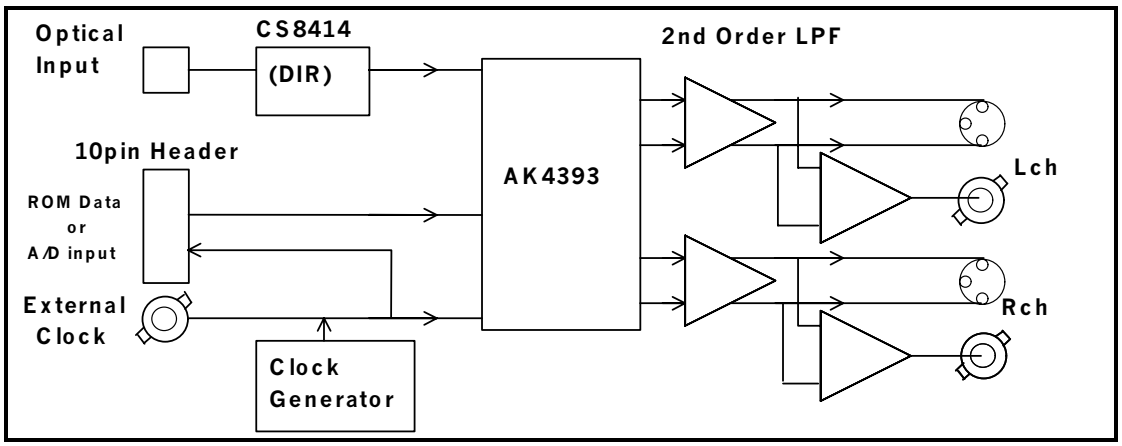


Fig.1 Block diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ External Analog Circuit (Rev.C)

The differential output circuit and LPF is implemented on board. The differential outputs of AK4393 is buffered by non-inverted circuit and output via Cannon connector(differential output). LPF adds differential outputs. NJM5534D is used for op-amp on this board that has low noise and high voltage torelance characteristics. Analog signal is output via Cannon and BNC connectors on the board. The output level is about 2.94Vrms(typ@VREF=5.0V) by Cannon and 2Vrms(typ@VREF=5.0V) by BNC.

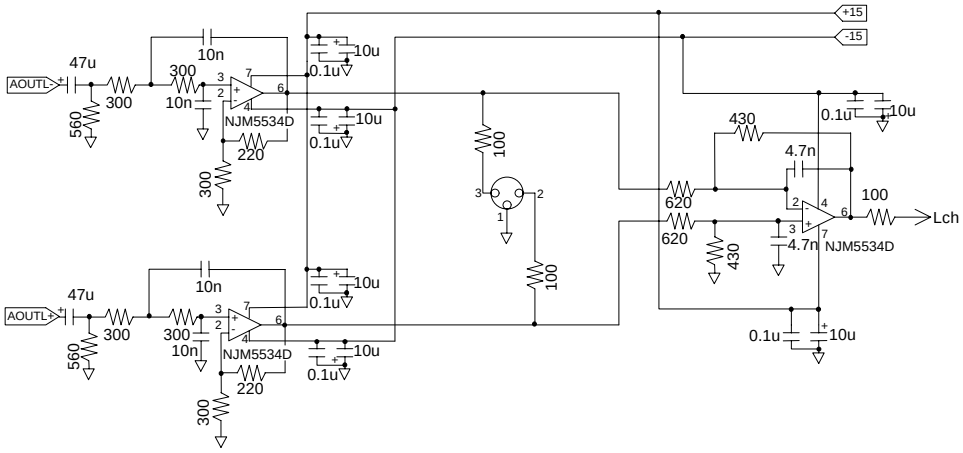


Fig.2 External Analog Filter

■ Operation sequence

1.Set up the jumpers for power supply.

[JP15(REG)] selects power supply for AVDD pin of AK4393.

short: 5V is supplied from regulator. (default)
Nothing should be connected to A5V jack.

open: 5V is supplied from A5V.

2.Set up the power supply lines.

+15V=15V, -15V=-15V: Power supply for op-amp. AVDD of AK4393 is supplied from "+15V" through regulator (JP15: short).

A5V=5V: This jack is used when AVDD of AK4393 is supplied from this. In this case, JP15 should be open.

DVDD=5V: Power supply for logic circuit on this board.

VP=3V~5.25V: Digital (set JP10 to VP),

AGND=DGND=0V .

Each supply line should be distributed from the power unit.

3.Set up the evaluation modes by jumper pins and DIP switches.(See next item.)

4.Power on.(The AK4393 should be reset once by bringing PD "L" upon power-up.)

*SW1 resets the AK4393 during operation.

The AK4393 is reset at SW1="L" and exits resetting at SW1="H".

■ The evaluation modes and corresponding jumper pins setting

1. Evaluation Modes

•Applicable Evaluation Mode

(1) DIR(Optical Link)
(2) Ideal sine wave generated by ROM data
(3) Using AD converted data
(4)All interface signals including master clock are fed externally.

(1) DIR(Optical Link) (default)

PORT2 is used for the evaluation using such as CD test disk. The DIR generates MCLK, BICK and LRCK SDATAfrom the received data through optical connector(PORT2: TORX176).

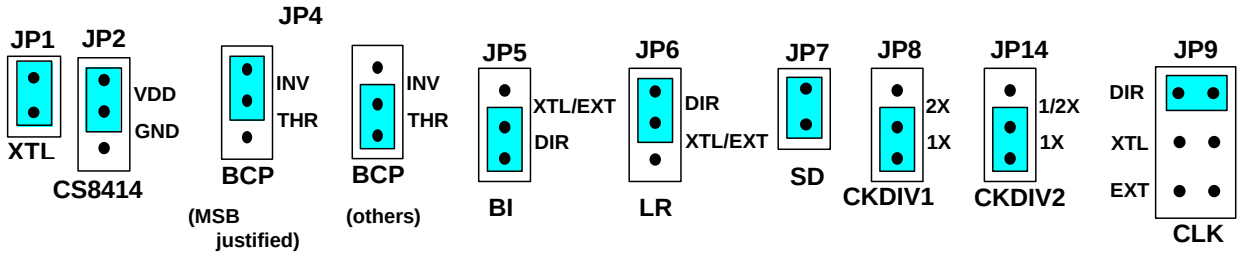


Fig.3 Jumper set-up (DIR)

(2) Ideal sine wave generated by ROM data

Digital signal generated by AKD43XX are used. PORT1 is used for the interface with AKD43XX. Master clock is sent from AKD4393 to AKD43XX then LRCK, BICK and SDATA are sent from AKD43XX to AKD4393.

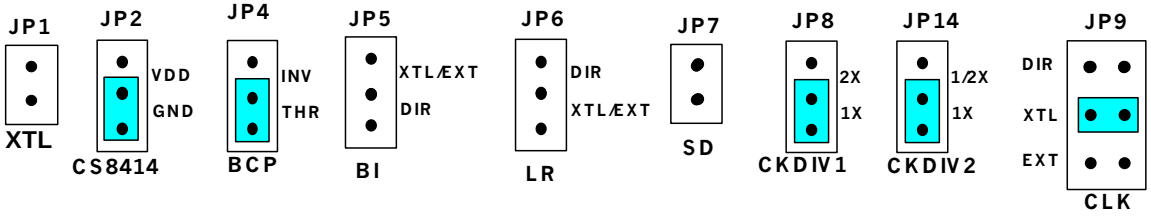


Fig.4 Jumper set-up (ROM data)

(3) Using AD converted data

AD converted data from AKM's AD evaluation boards(AKD539X, AKD535X) is used through PORT1.

* In case of using external clock through a BNC connector, select EXT of JP9 and short JP1.

* In case of using the double speed sampling mode, select 1/2X of JP8 and set S2-2(DFS) on.

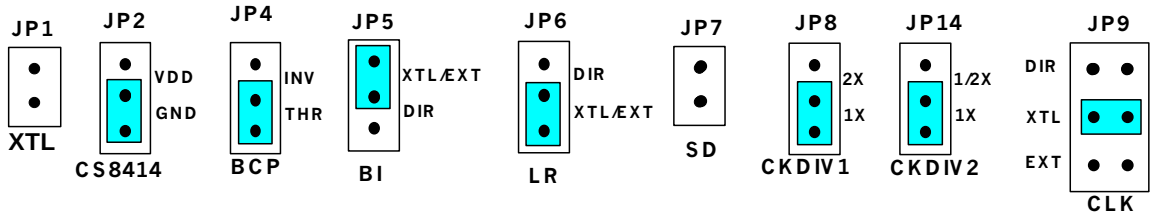


Fig.5 Jumper set-up (A/D)

(3) All interface signals including master clock are fed externally.

Under the following set-up, MCLK, LRCK and SCLK signals needed for the D/A to operate could be fed through PORT1.

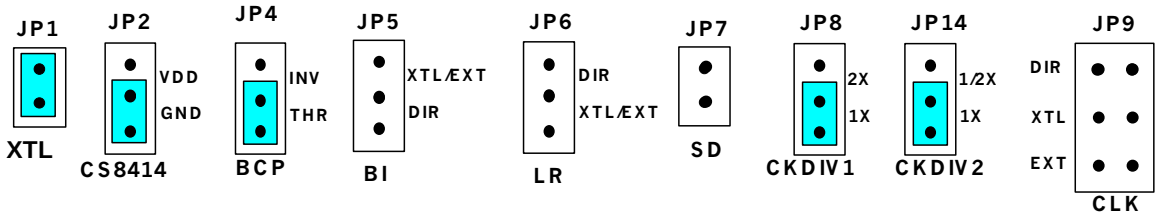


Fig.6 Jumper set-up (ext.)

2. MCLK set-up

When the LRCK is fed from the 74HC4040 on the board, The ratio of MCLK to LRCK can be selected by JP8 and JP14.

JP14	JP8	X'tal	MCLK	fs	MCLK/LRCK
1X	1X	12.288MHz	12.288MHz	48kHz	256
1X	2X	24.576MHz	24.576MHz	48kHz	512
1/2X	1X	24.576MHz	12.288MHz	96kHz	128
1/2X	2X	49.152MHz	12.288MHz	96kHz	128

Table.1 set-up example

3. BICK set-up

When BICK is supplied from U1(74HC4040), either 32fs or 64fs could be selected. Fig.8 shows 64fs mode. 64fs mode is recommended.

*Only mode 0(LSB justified 16bit mode) can correspond to 32fs.

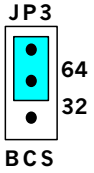


Fig.7 Jumper Set-up (BCS)

4. DIP switch set-up

Confirm the set-up of the DIP switch before the operation. “ON” means “H” and “OFF” means “L”.

4-1. Set-up of SW3, SW4(Mode set-up of AK4393: see the data sheet of AK4393)

DIF2	DIF1	DIF0	Mode	BICK	
OFF	OFF	OFF	0: LSB justified, 16bit	≥32fs	
OFF	OFF	ON	1: LSB justified, 20bit	≥40fs	
OFF	ON	OFF	2: LSB justified, 24bit	≥48fs	
OFF	ON	ON	3: I^2S	≥48fs	(default)
ON	OFF	OFF	4: MSB justified, 24bit	≥48fs	

Table 2 Audio Serial Interface Format Select Pins (SW3-5,6,7)

4-2. Set-up of SW6 (Mode set-up of CS8414. About details, see the data-sheet of CS8414)

Adjust the audio data format of CS8414 (DIR) to AK4393. CS8414 does not match the LSB justified 20bit/24bit mode of AK4393.

M3 (SW6-2)	M2 (SW6-3)	M1 (SW6-4)	M0 (SW6-5)	Data format	JP4	
OFF	OFF	OFF	OFF	MSB justified, 24bit	INV	
OFF	OFF	ON	OFF	I^2S	THR	(default)
OFF	ON	OFF	ON	LSB justified, 16bit	THR	

Table 3. Set-up of SW6

SW6-1 (SEL): Usually ON.

SW6-6 (CS12): Select the channel for indicating the channel status.

ON: Rch (default), OFF: Lch

5. Parallel/Serial Control

SW5: set up P/S pin of AK4393.

H: parallel mode. PORT3 is used JP11, 12 and 13 should be open.

L: serial mode. PORT3 is used. JP11, 12 and 13 should be open.

6. Other set-up

SW1: Reset of AK4393. Select "H" during operation.

SW2: Soft-mute of AK4393. The soft-mute is executed during SW2 pushed.

LE1 : This LED shows pre-emphasis status. It turns on when the data is pre-emphasized.

LE2 : This LED shows the output of VERF pin in CS8414. It turns on when the error is occured in CS8414.

■ AK4393 Measurement Example

Conditions:

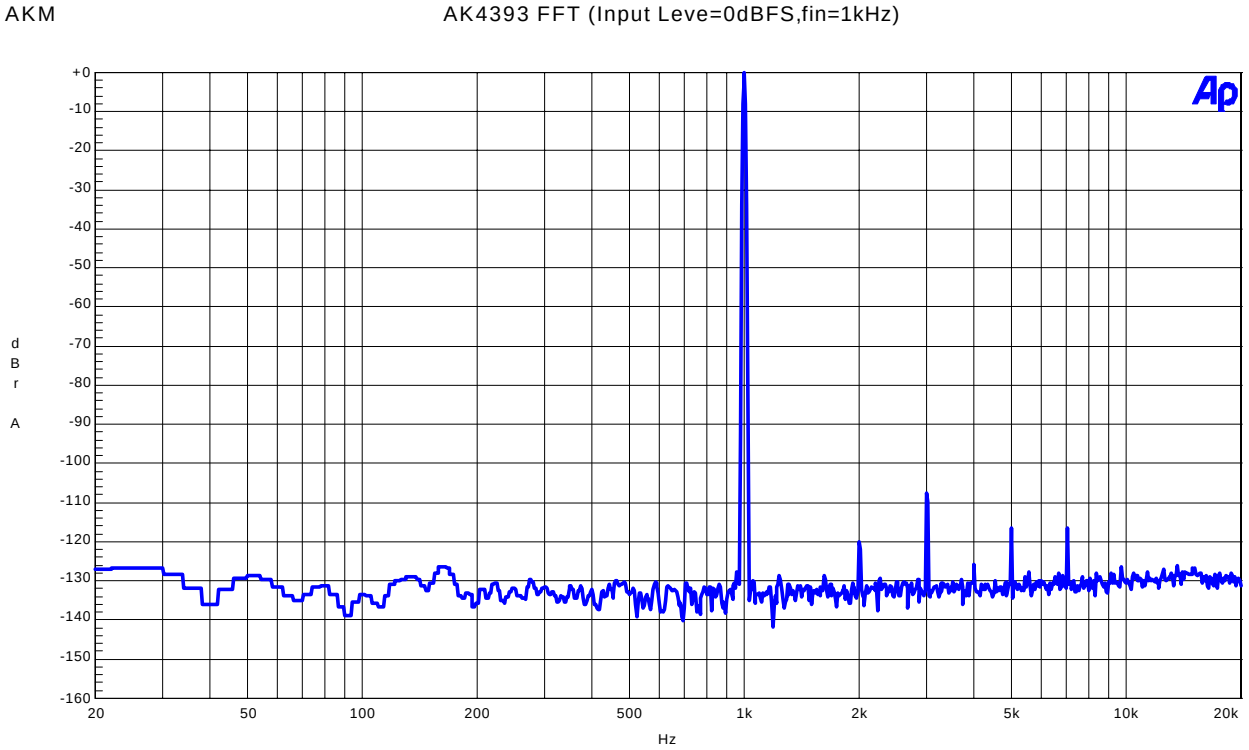
AVDD =DVDD= 5.0V
Interface = DIR (44.1kHz, 96kHz)
MCLK = 256fs(fs=44.1kHz, 96kHz)
BICK = 64fs
fs = 44.1kHz, 96kHz
Input data = 24bit
Measurement unit: Audio Precision System Two Cascade (fs=44.1kHz, 96kHz)

(AKD4393 Rev.C: differential output)

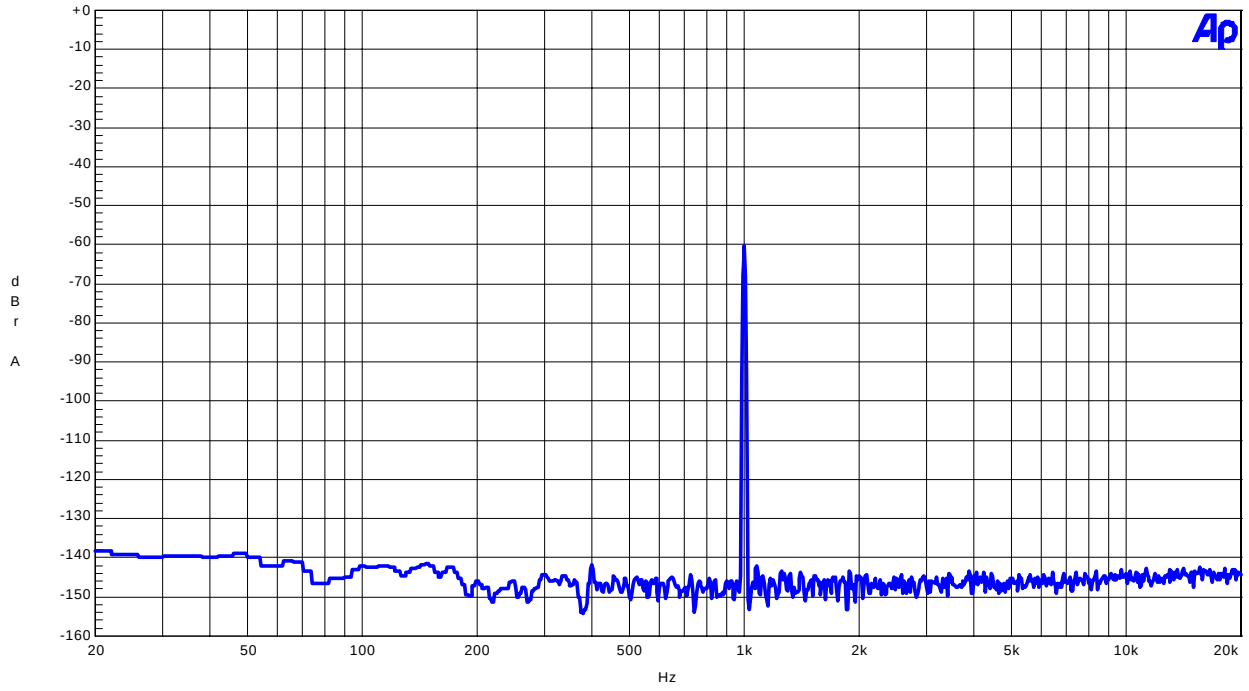
fs		Result	
44.1kHz	THD+N	102.3	20kLPF
	DR	120.0	22kLPF + A-weighted
	S/N	119.9	22kLPF + A-weighted
96kHz	THD+N	100.9	40kLPF
	DR	119.5	80kLPF + A-weighted
	S/N	119.7	80kLPF + A-weighted

Plot
FFT Point: 16384
Window: Equiripple
Averages: 4

(fs=44.1kHz)



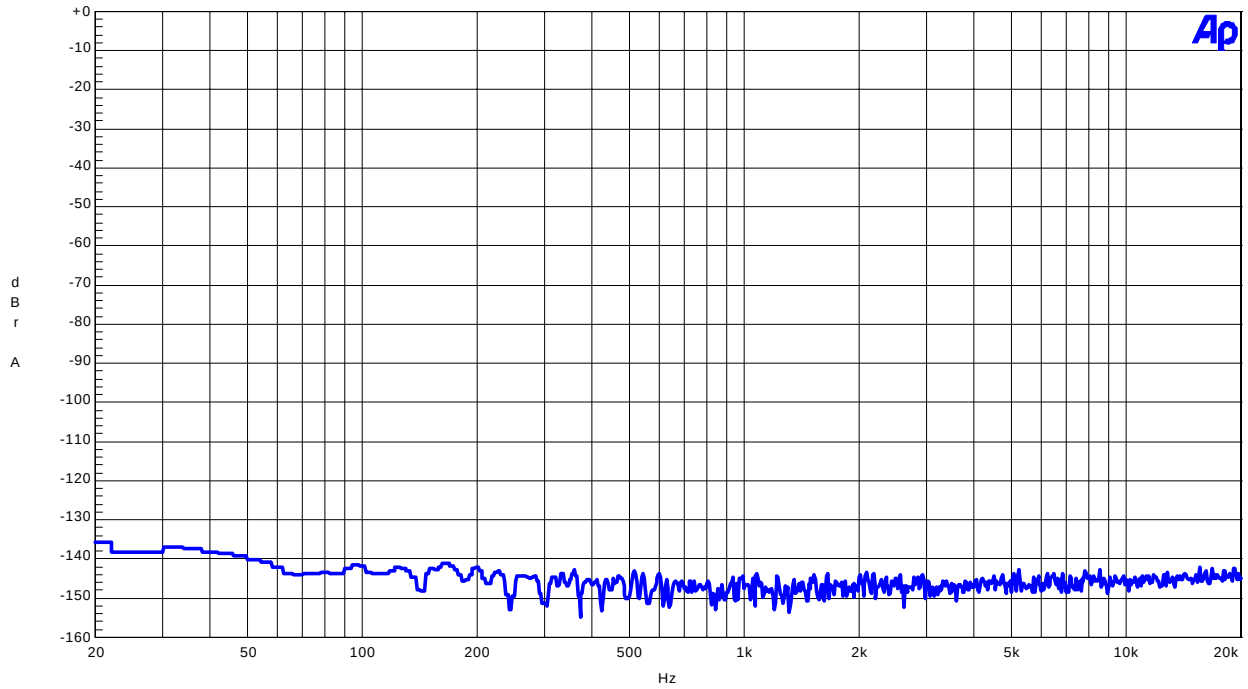
FFT (Input Level=0dBFS, fin=1kHz)



FFT (Input Level=-60dBFS, fin=1kHz)

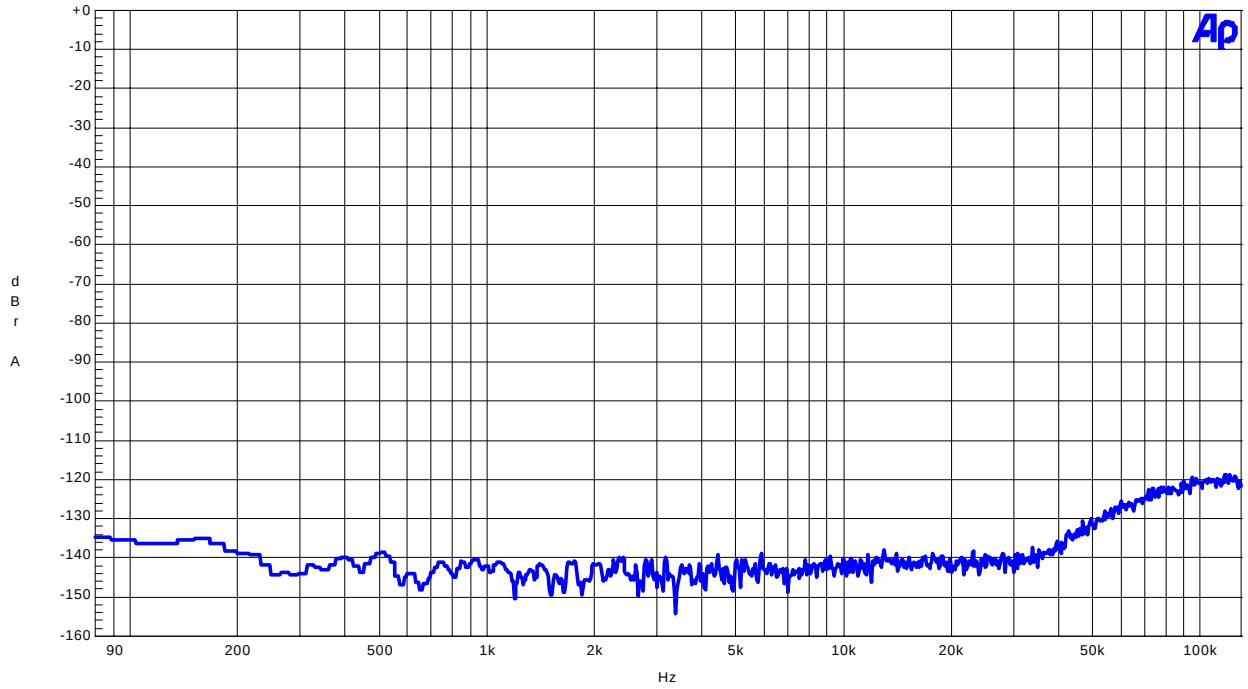
(fs=44.1kHz)

AKM AK4393 FFT (Input = "0"data)



FFT (noise floor)

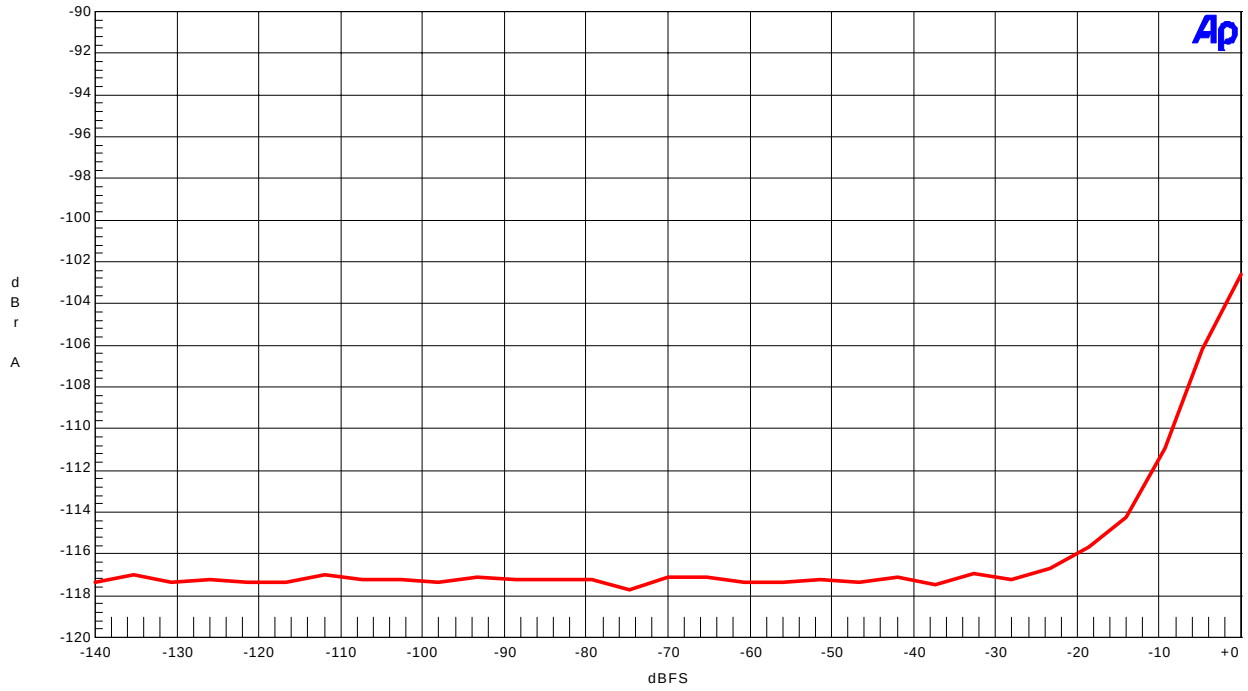
AKM AK4393 FFT (Input = "0"data,out-of band)



FFT (noise floor, out-of band)

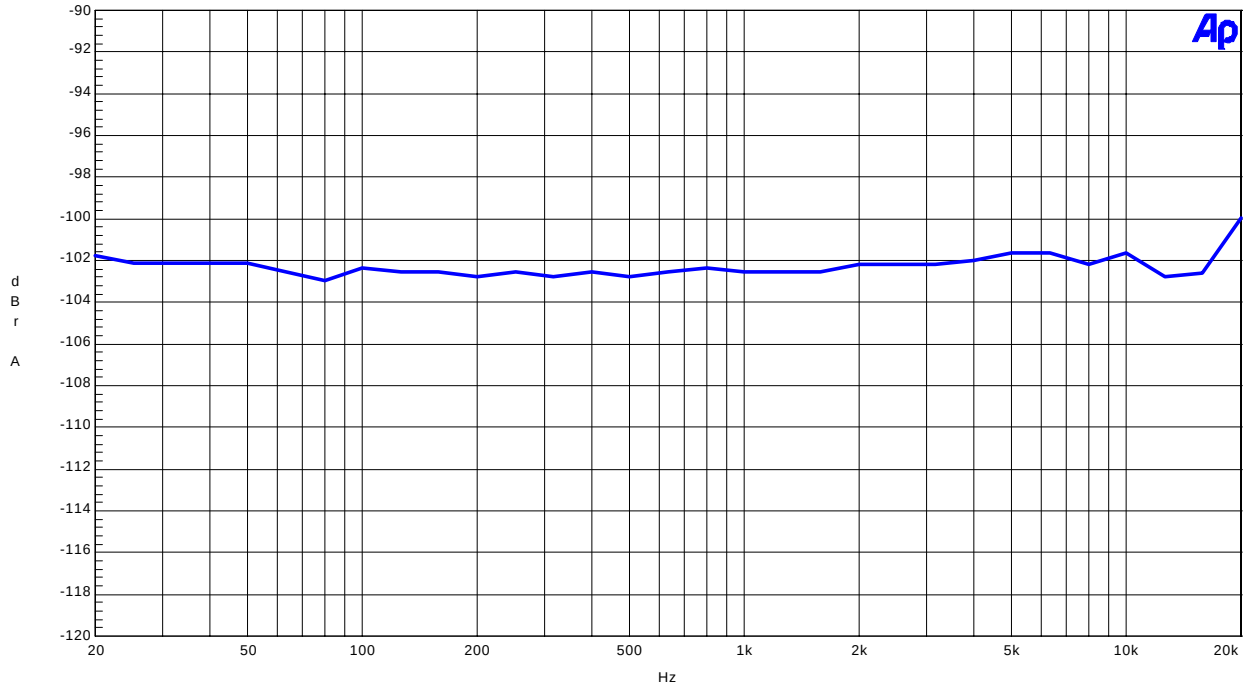
(fs=44.1kHz)

AKM AK4393 THD + N vs Amplitude (fin=1kHz)



THD + N vs Amplitude (fin=1kHz)

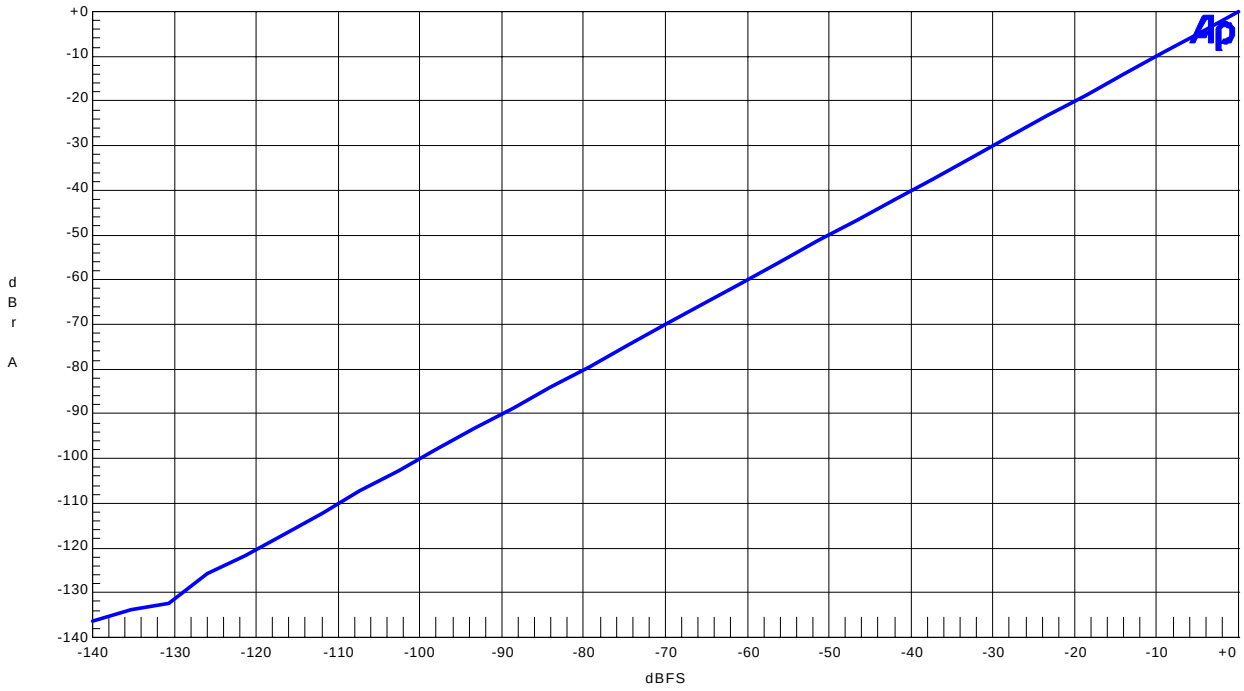
AKM AK4393 THD + N vs Input Frequency(Input Level=0dBFS)



THD + N vs Input Frequency (Input Level=0dBFS)

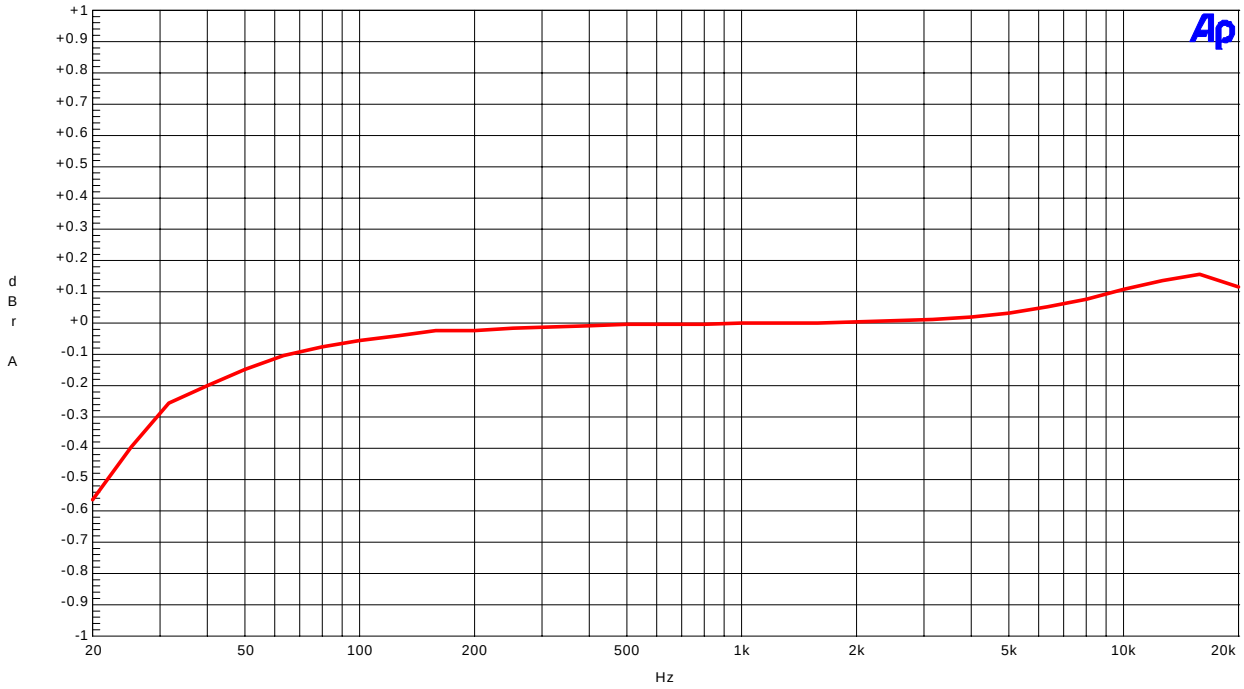
(fs=44.1kHz)

AKM AK4393 Linearity



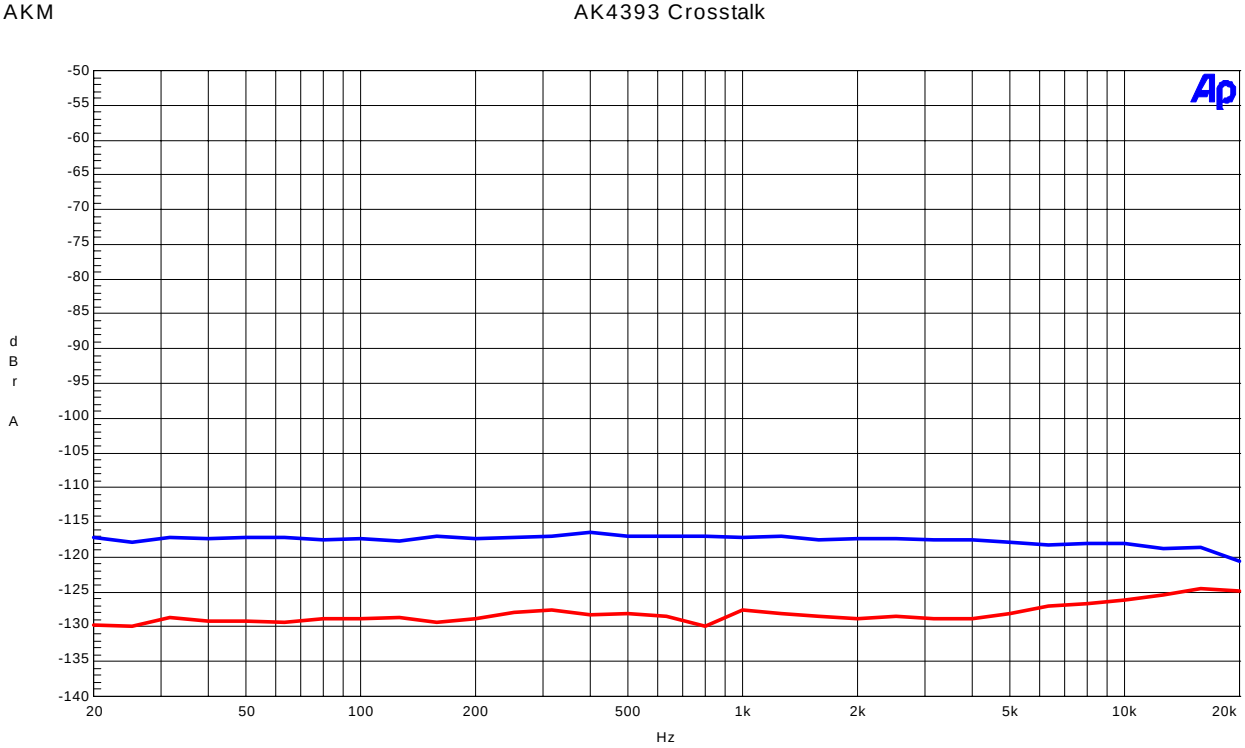
Linearity (fin=1kHz)

AKM AK4393 Frequency Response



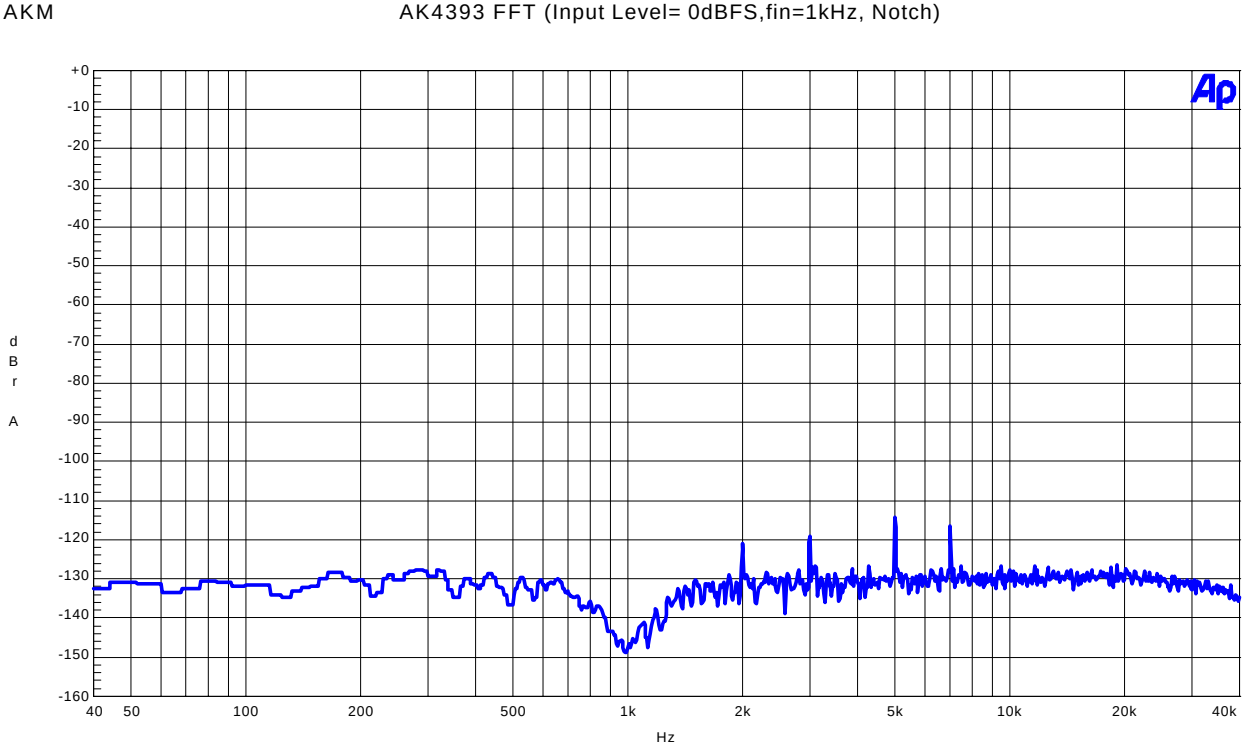
Frequency Response (Input Level=0dBFS)

(fs=44.1kHz)

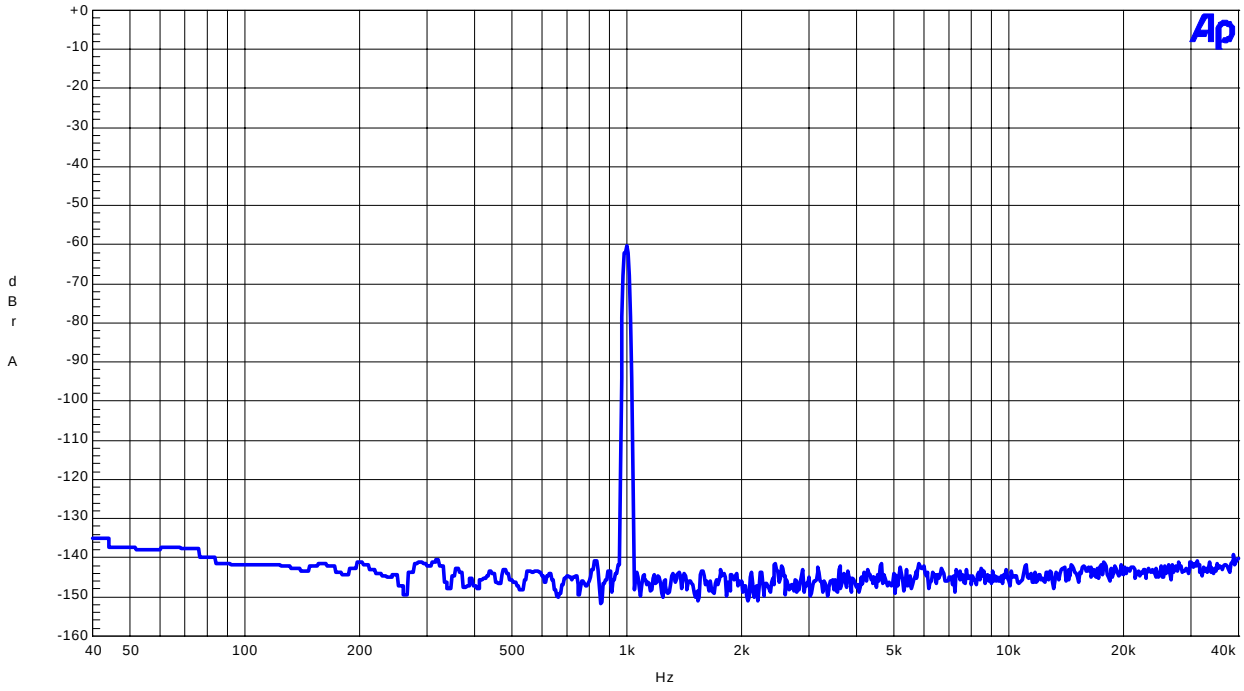


Crosstalk (upper = Rch, Lower = Lch)

(fs=96kHz)

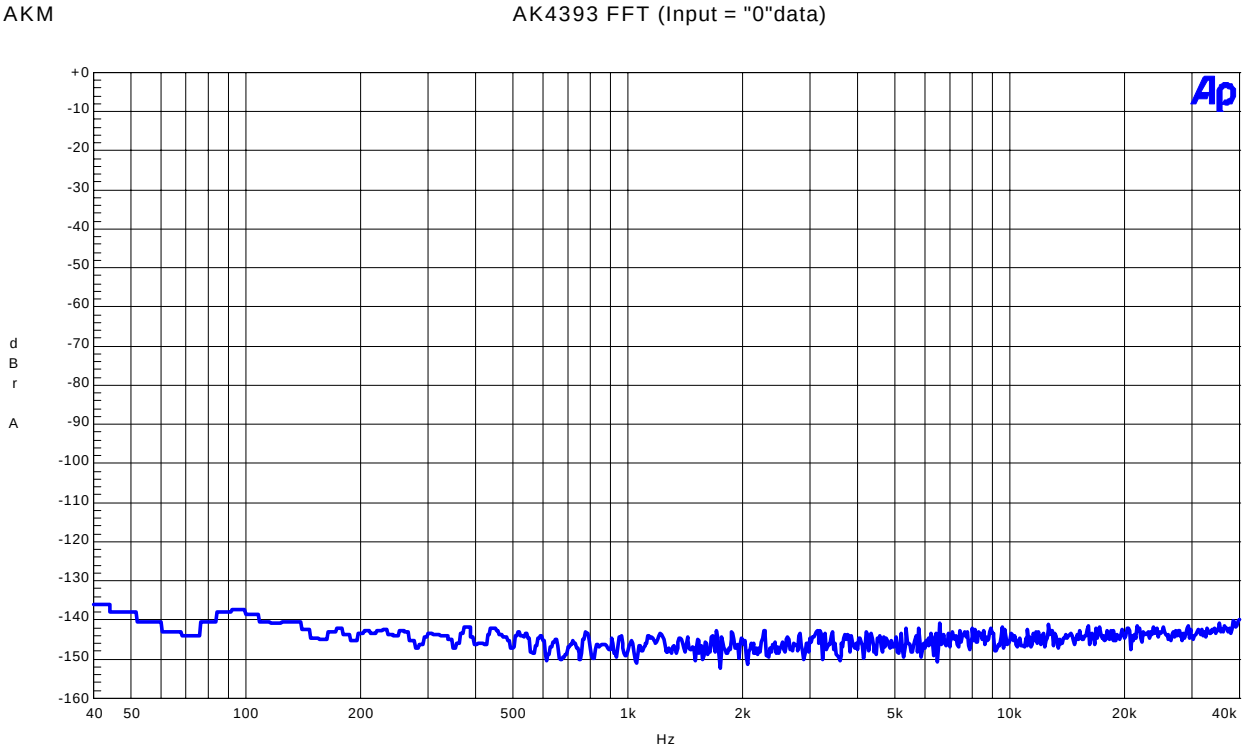


FFT (Input Level=0dBFS, fin=1kHz, notch)

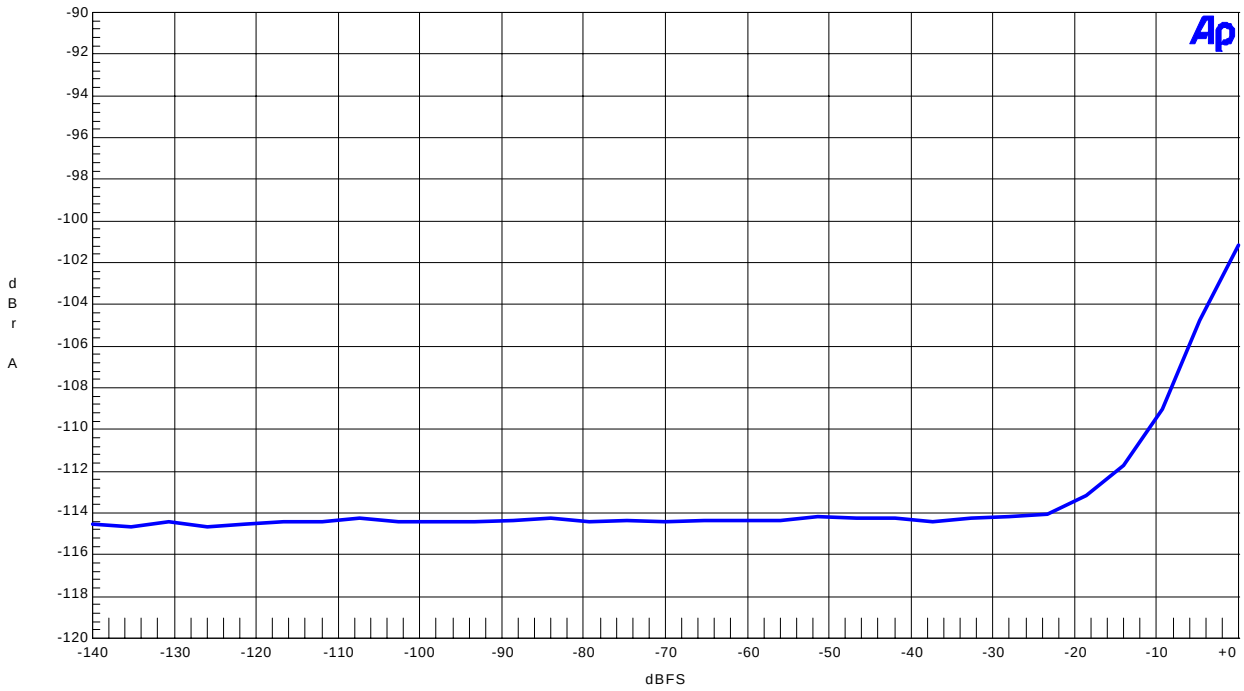


FFT (Input Level=-60dBFS, fin=1kHz)

(fs=96kHz)

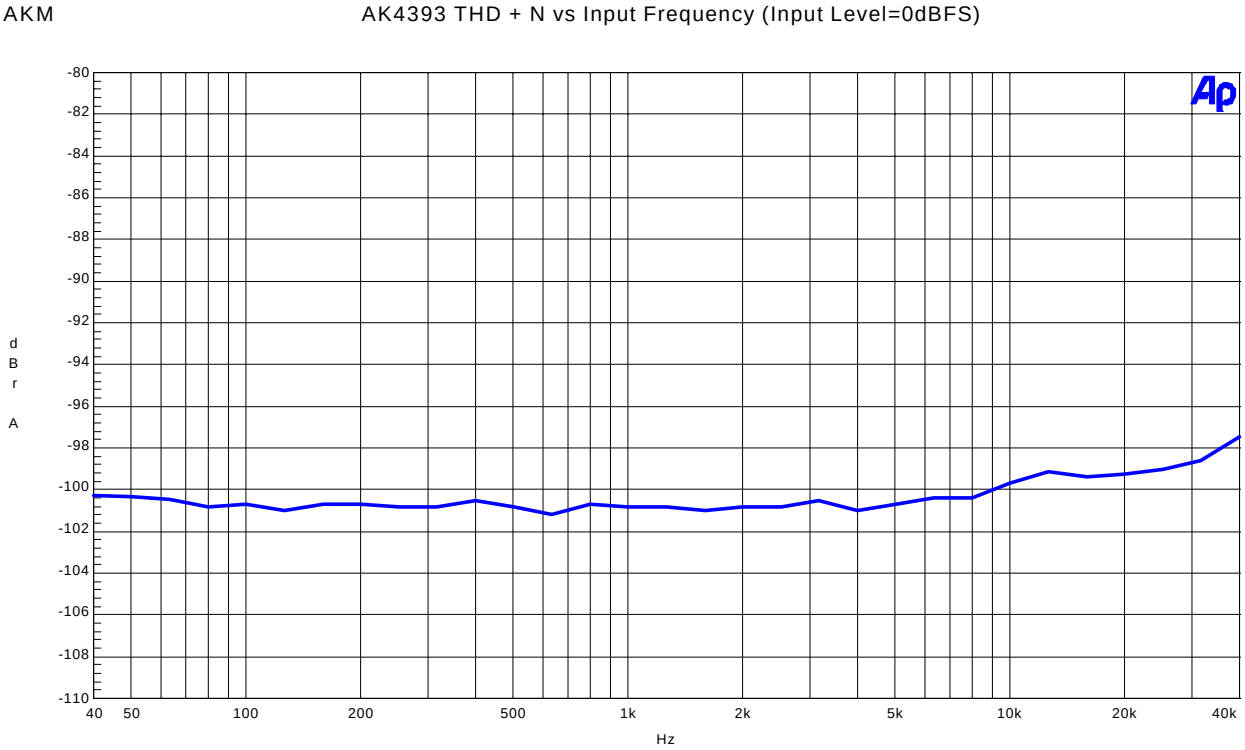


FFT (noise floor)

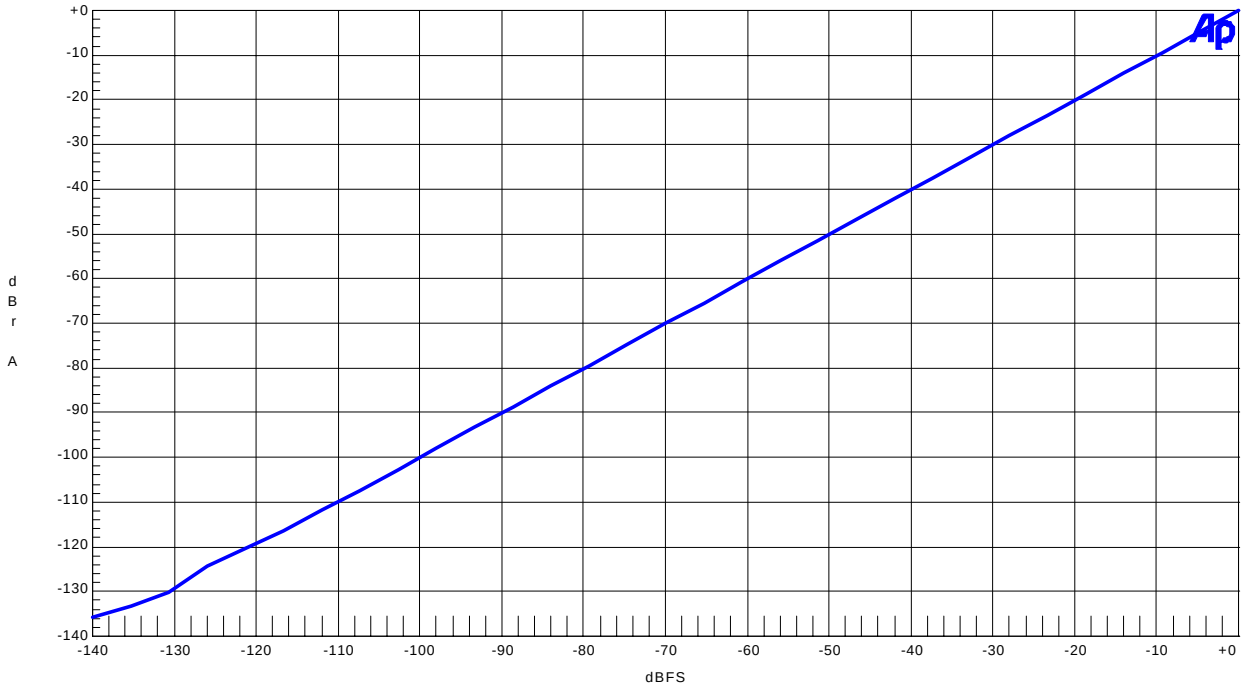


THD + N vs Amplitude (fin=1kHz)

(fs=96kHz)

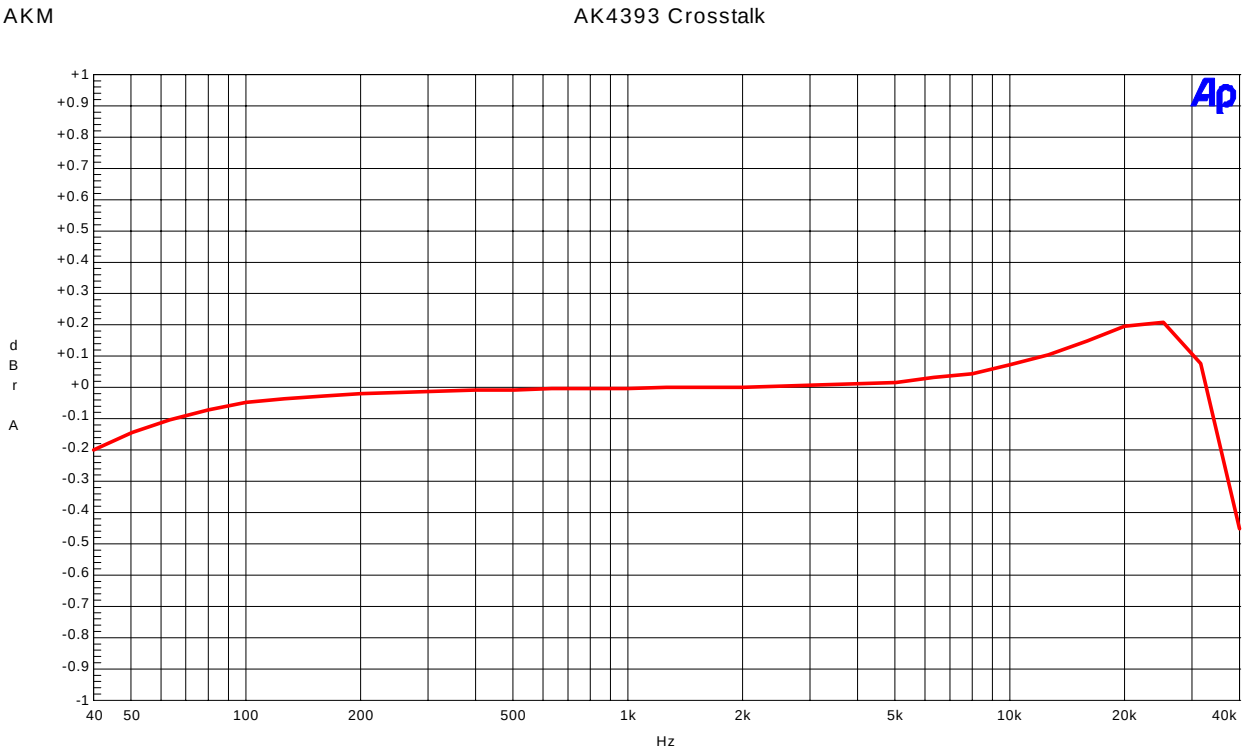


THD + N vs Input Frequency (Input Level=0dBFS)

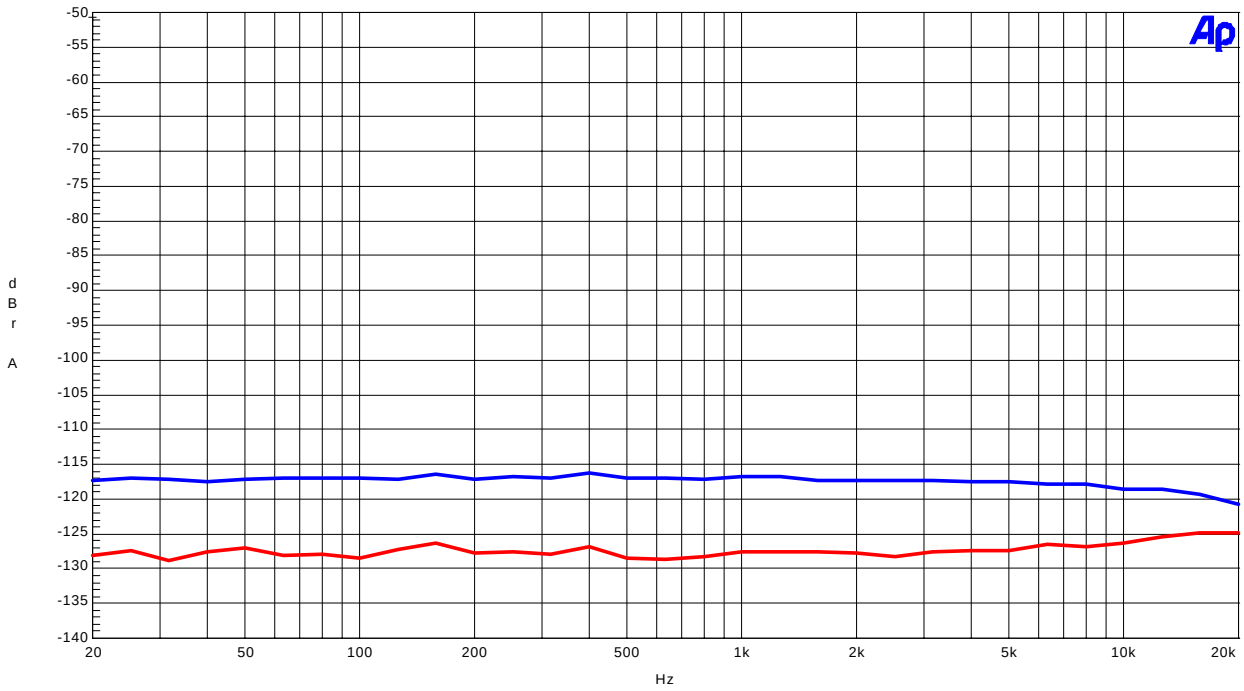


Linearity (fin=1kHz)

(fs=96kHz)



Frequency Response (Input Level=0dBFS)



Crosstalk (upper = Rch, Lower = Lch)

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  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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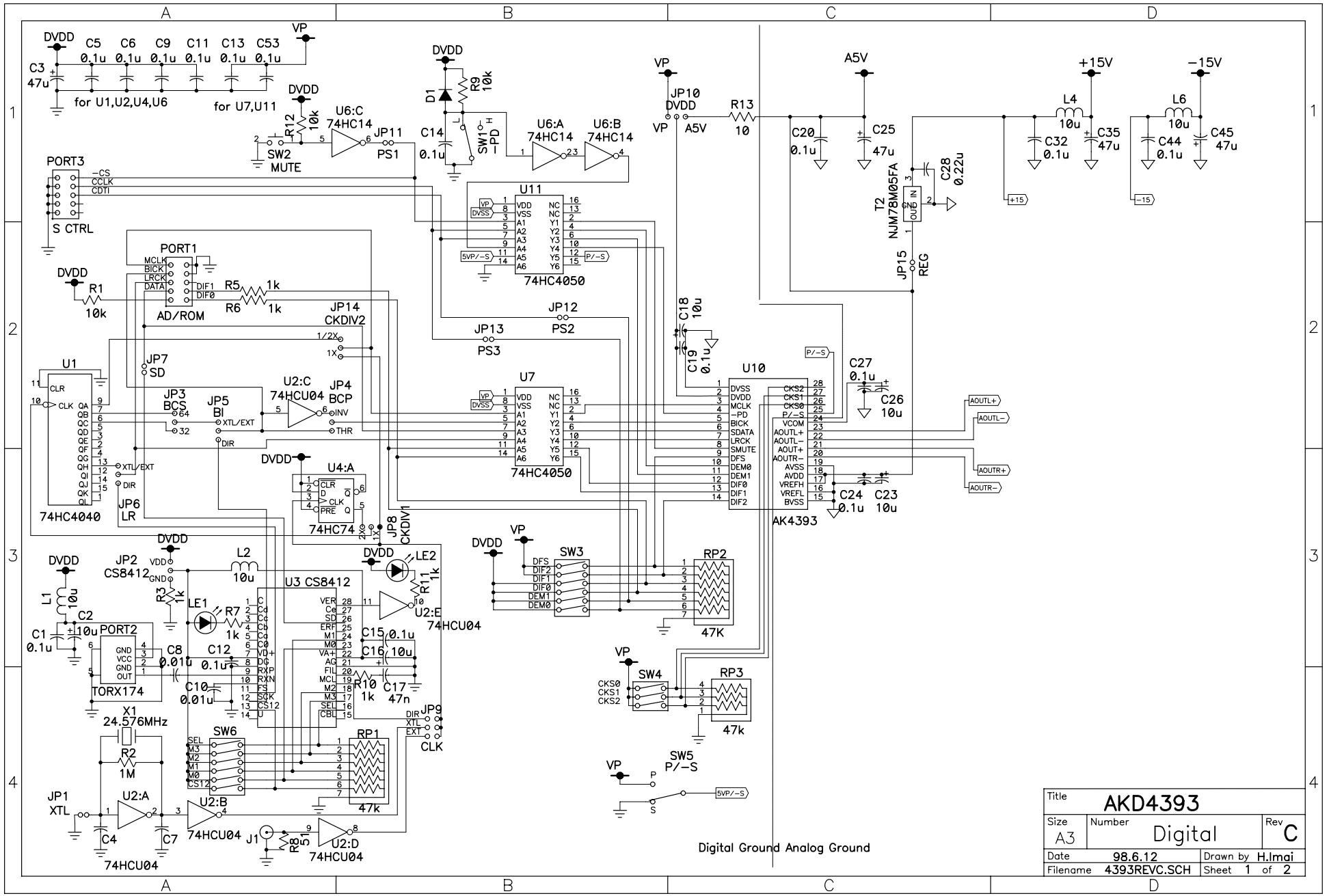
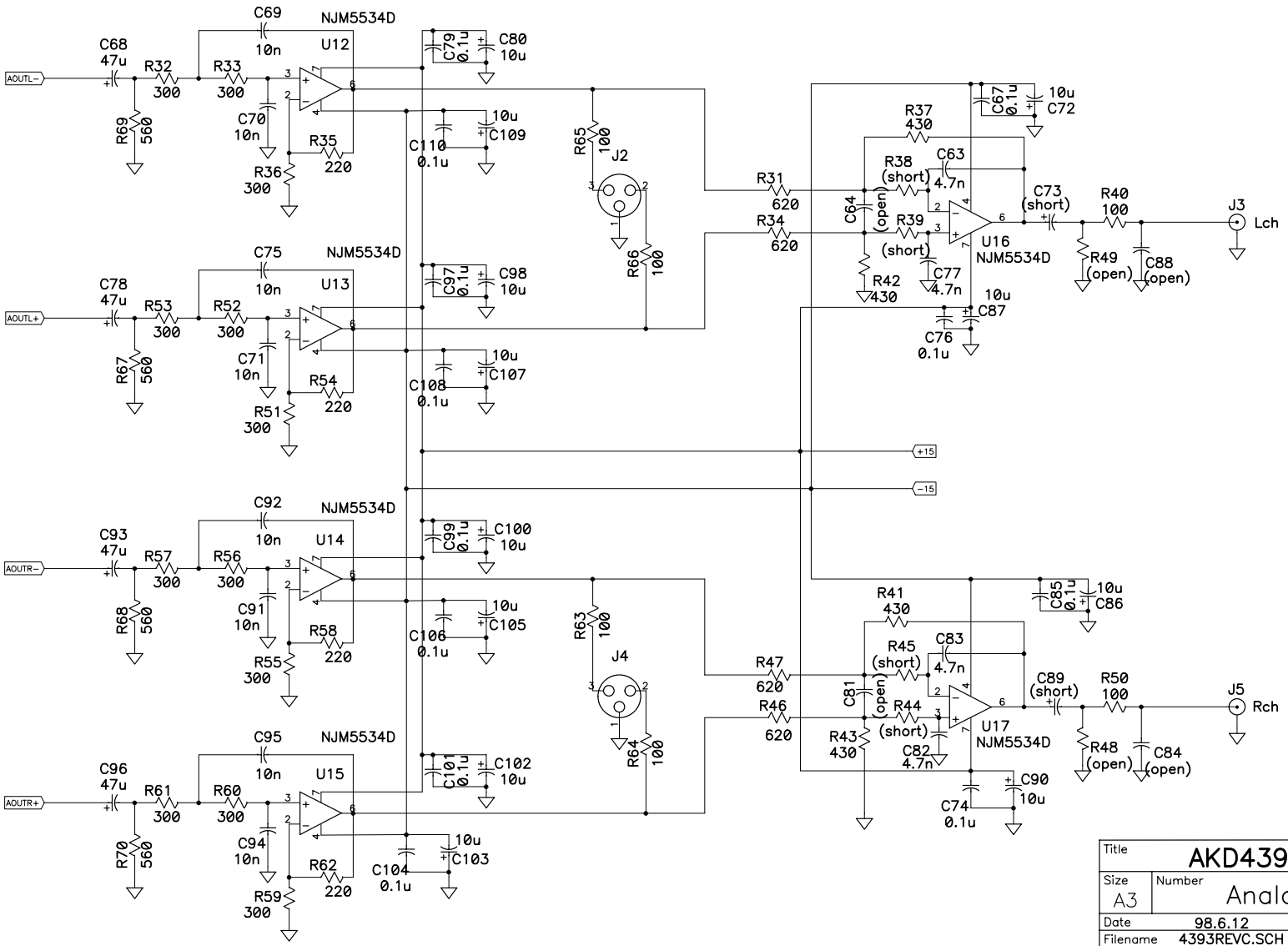

DVDD
VP
C3 47u
C5 C6 C9 C11 C13 C53 0.1u
for U1,U2,U4,U6
for U7,U11
R12 10k
SW2 MUTE
U6:C 74HC14
JP11 PS1
D1
R9 10k
C14 0.1u
SW1 −PD
U6:A 74HC14
U6:B 74HC14
JP10 DVDD VP
A5V
R13 10
C20 0.1u
C25 47u
C28 0.22u
T2 NJM78M05FA
JP15 REG
L4 10u
C32 0.1u
C35 47u
L6 10u
C44 0.1u
C45 47u
+15V
−15V
PORT3
−CS
CCLK
CDTI
S CTRL
U11
74HC4050
PORT1
MCLK
BICK
LRCK
DATA
DIF1
DIF0
AD/ROM
R1 10k
R5 1k
R6 1k
JP14 CKDIV2
1/2X
1X
JP12 PS2
JP13 PS3
C18 10u
C19 0.1u
U1
74HC4040
JP7 SD
JP3 BCS
JP5 BI
XTL/EXT
DIR
U2:C 74HCU04
JP4 BCP
INV
THR
U7
74HC4050
U10
AK4393
C27 0.1u
C26 10u
C24 0.1u
C23 10u
AOUTL+
AOUTL−
AOUTR+
AOUTR−
U4:A
74HC74
JP6 LR
JP8 CKDIV1
JP2 CS8412
L2 10u
L1 10u
C2 10u
C1 0.1u
R3 1k
LE1
R7 1k
LE2
R11 1k
U2:E 74HCU04
U3 CS8412
C12 0.1u
C8 0.01u
C10 0.01u
C15 0.1u
C16 10u
C17 47n
R10 1k
PORT2
TORX174
X1 24.576MHz
R2 1M
JP9 XTL EXT CLK
SW3
RP2
47K
SW4
RP3
47k
SW5 P/−S
SW6
RP1
47k
JP1 XTL
U2:A
U2:B
U2:D
74HCU04
C4
C7
J1
R8 51
Digital Ground Analog Ground
Title AKD4393
Size A3
Number Digital
Rev C
Date 98.6.12
Drawn by H.Imai
Filename 4393REVC.SCH
Sheet 1 of 2


AOUTL−
AOUTL+
AOUTR−
AOUTR+
NJM5534D
U12
U13
U14
U15
U16
U17
C68 47u
C69 10n
C70 10n
C71 10n
C75 10n
C78 47u
C91 10n
C92 10n
C93 47u
C94 10n
C95 10n
C96 47u
R32 300
R33 300
R35 220
R36 300
R51 300
R52 300
R53 300
R54 220
R55 300
R56 300
R57 300
R58 220
R59 300
R60 300
R61 300
R62 220
R67 560
R68 560
R69 560
R70 560
C79 0.1u
C80 10u
C97 0.1u
C98 10u
C99 0.1u
C100 10u
C101 0.1u
C102 10u
C104 0.1u
C106 0.1u
C108 0.1u
C110 0.1u
C103 10u
C105 10u
C107 10u
C109 10u
R65 100
R66 100
R63 100
R64 100
J2
J4
+15
−15
R31 620
R34 620
R47 620
R46 620
R37 430
R38 (short)
R39 (short)
R42 430
R41 430
R45 (short)
R44 (short)
R43 430
C63 4.7n
C64 (open)
C77 4.7n
C81 (open)
C82 4.7n
C83 4.7n
C67 0.1u
C72 10u
C73 (short)
C76 0.1u
C87 10u
C85 0.1u
C86 10u
C89 (short)
C74 0.1u
C90 10u
R40 100
R49 (open)
C88 (open)
R50 100
R48 (open)
C84 (open)
J3
Lch
J5
Rch
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H.Imai
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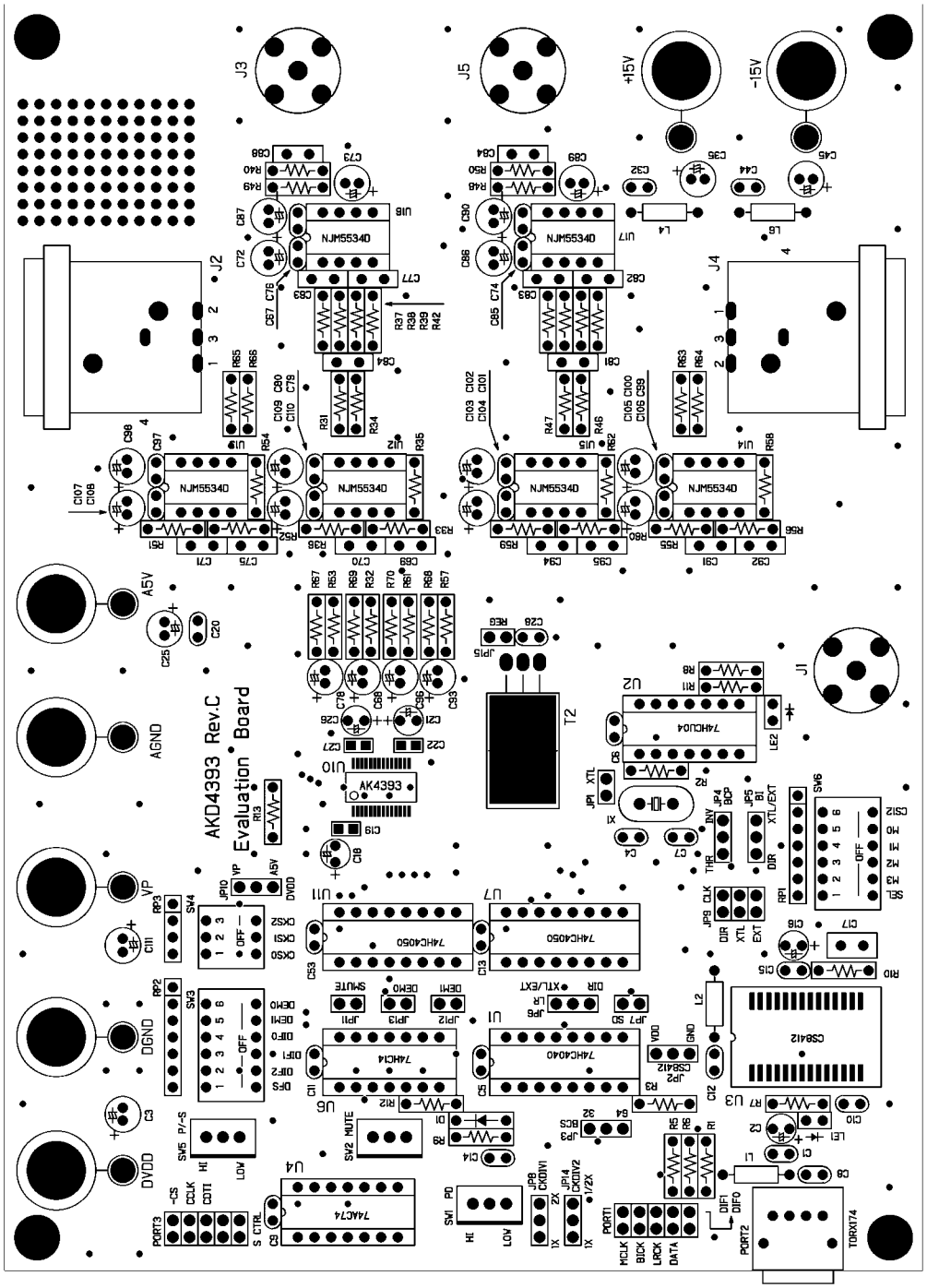
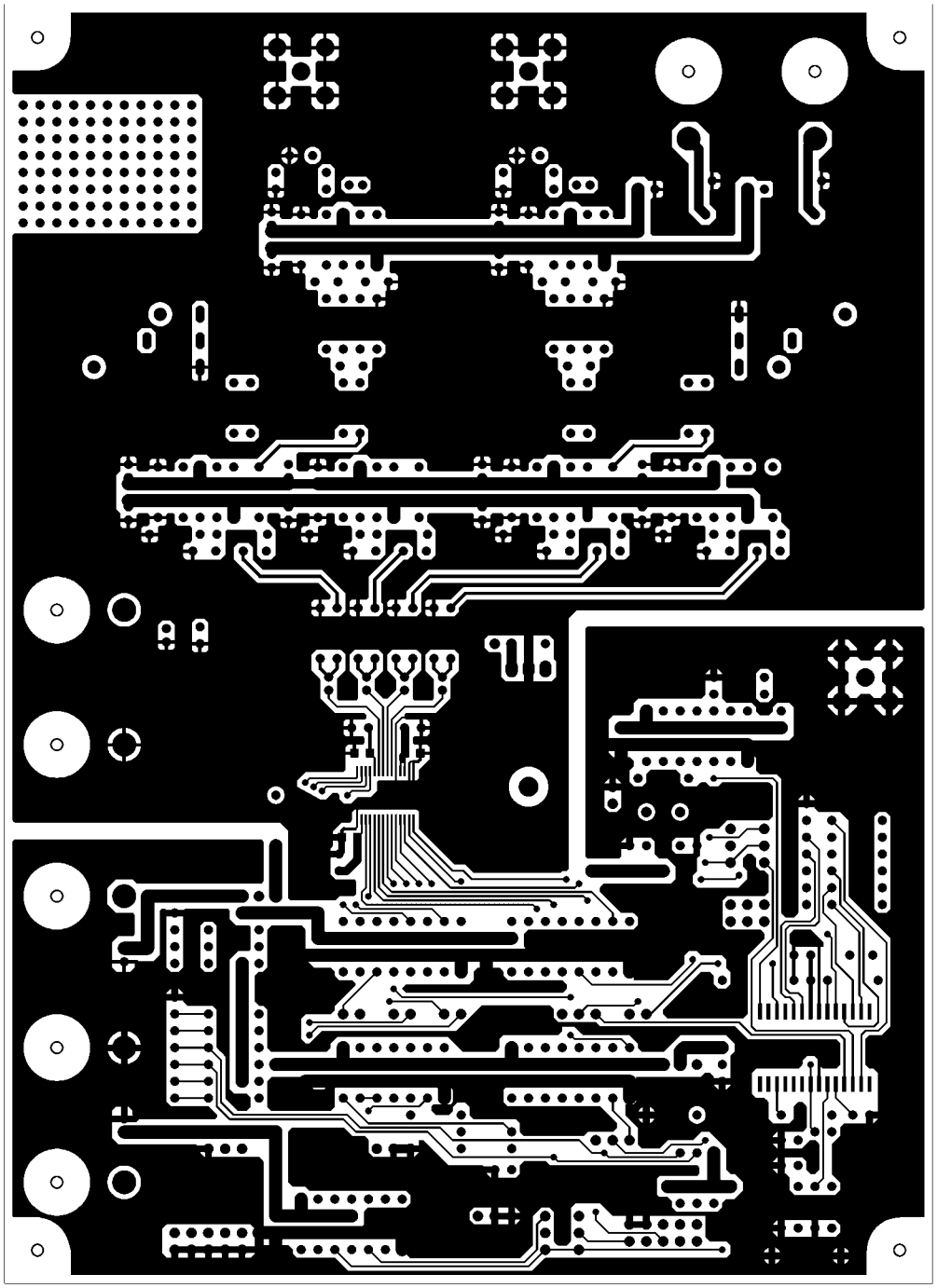


4393C L1 SR SILK



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L2 C3936