

# DATA SHEET

## **74LVC1G80**

Single D-type flip-flop;  
positive-edge trigger

Product specification  
Supersedes data of 2004 Jun 29

2004 Sep 10

## Single D-type flip-flop; positive-edge trigger

## 74LVC1G80

## FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- $\pm 24$  mA output drive ( $V_{CC} = 3.0$  V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C.

## DESCRIPTION

The 74LVC1G80 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G80 provides a single positive-edge triggered D-type flip-flop.

Information on the data input is transferred to the  $\bar{Q}$  output pin on the LOW-to-HIGH transition of the clock pulse. The input pin D must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

## QUICK REFERENCE DATA

$GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay CP to $\bar{Q}$	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k $\Omega$	3.4	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ $\Omega$	2.3	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	2.5	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	2.4	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	1.8	ns
$f_{max}$	maximum frequency	$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	350	MHz
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per buffer	$V_{CC} = 3.3$ V; notes 1 and 2	17	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = GND$  to  $V_{CC}$ .

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## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
CP	D	$\bar{Q}$
↑	L	H
↑	H	L
L	X	$\bar{q}$

## Note

- H = HIGH voltage level;  
L = LOW voltage level;  
↑ = LOW-to-HIGH CP transition;  
X = don't care;  
 $\bar{q}$  = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

## ORDERING INFORMATION

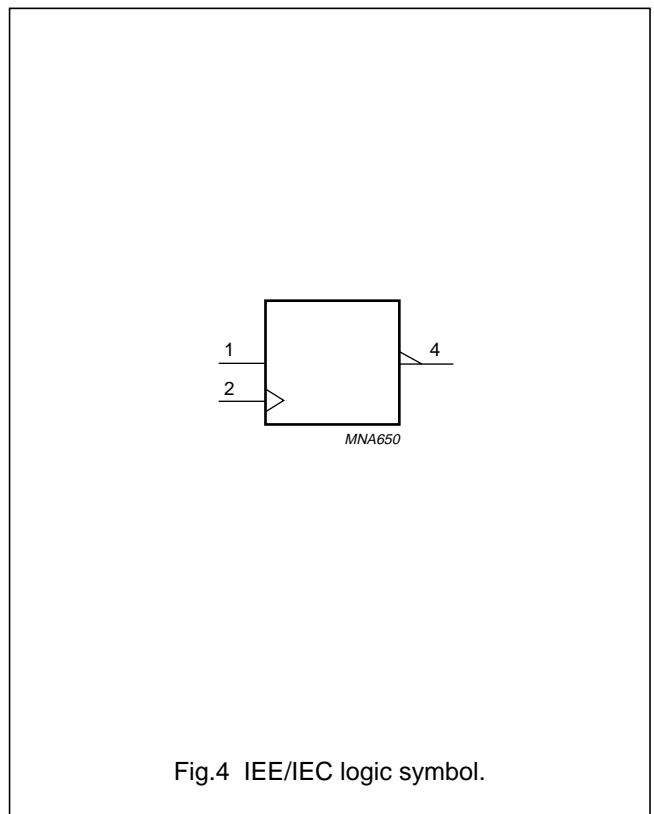
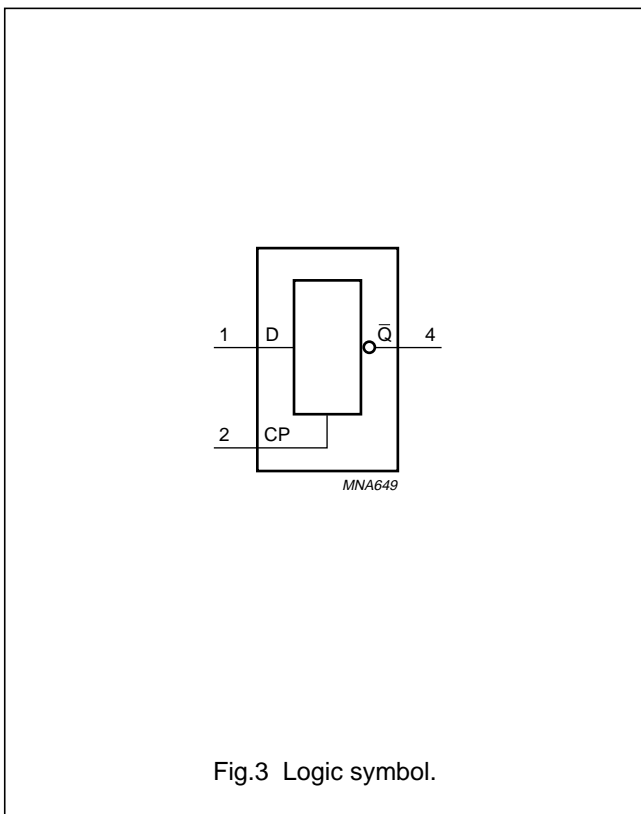
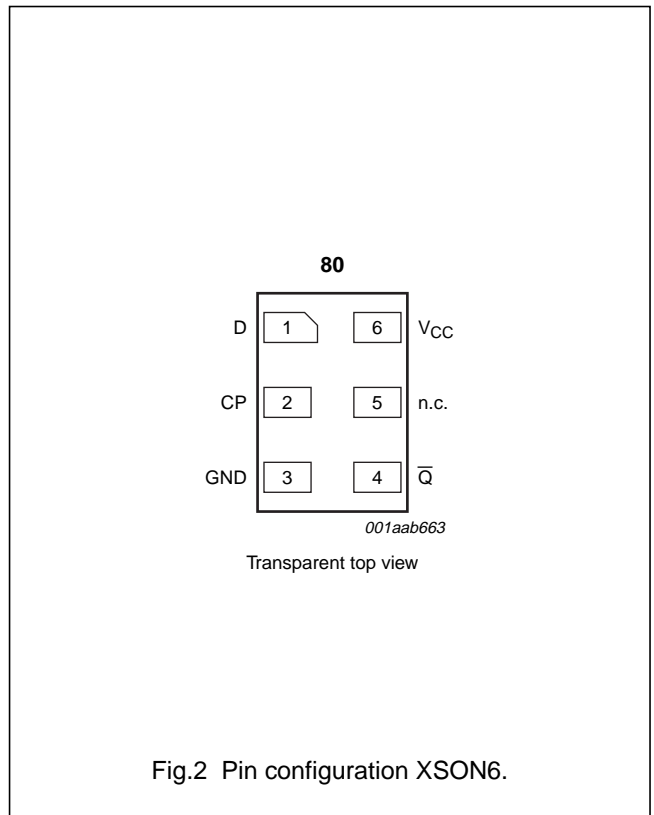
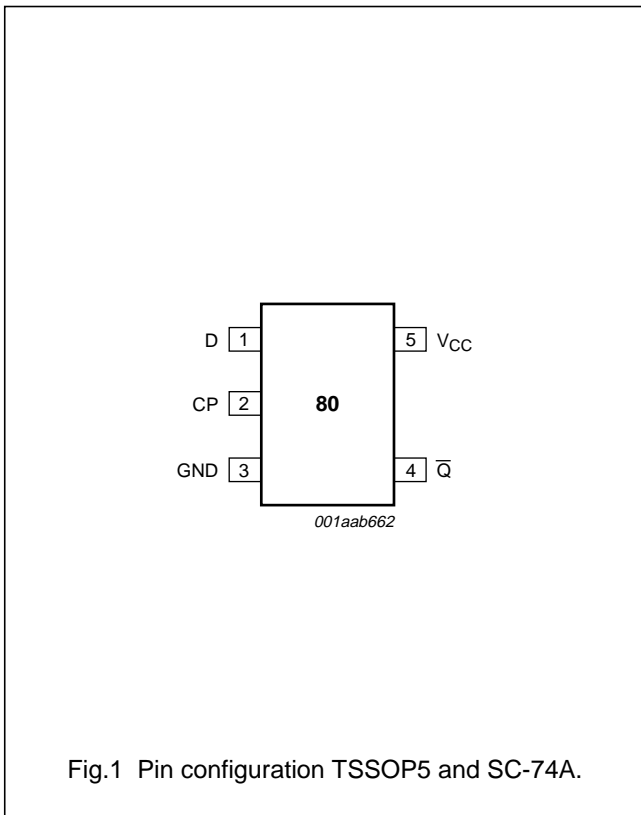
TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G80GW	-40 °C to +125 °C	5	SC-88A	plastic	SOT353-1	VT
74LVC1G80GV	-40 °C to +125 °C	5	SC-74A	plastic	SOT753	V80
74LVC1G80GM	-40 °C to +125 °C	6	XSON6	plastic	SOT886	VT

## PINNING

PIN TSSOP5; SC-74A	PIN XSON6	SYMBOL	DESCRIPTION
1	1	D	input D
2	2	CP	clock pulse input CP
3	3	GND	ground (0 V)
4	4	$\bar{Q}$	output $\bar{Q}$
-	5	n.c.	not connected
5	6	V <sub>CC</sub>	supply voltage

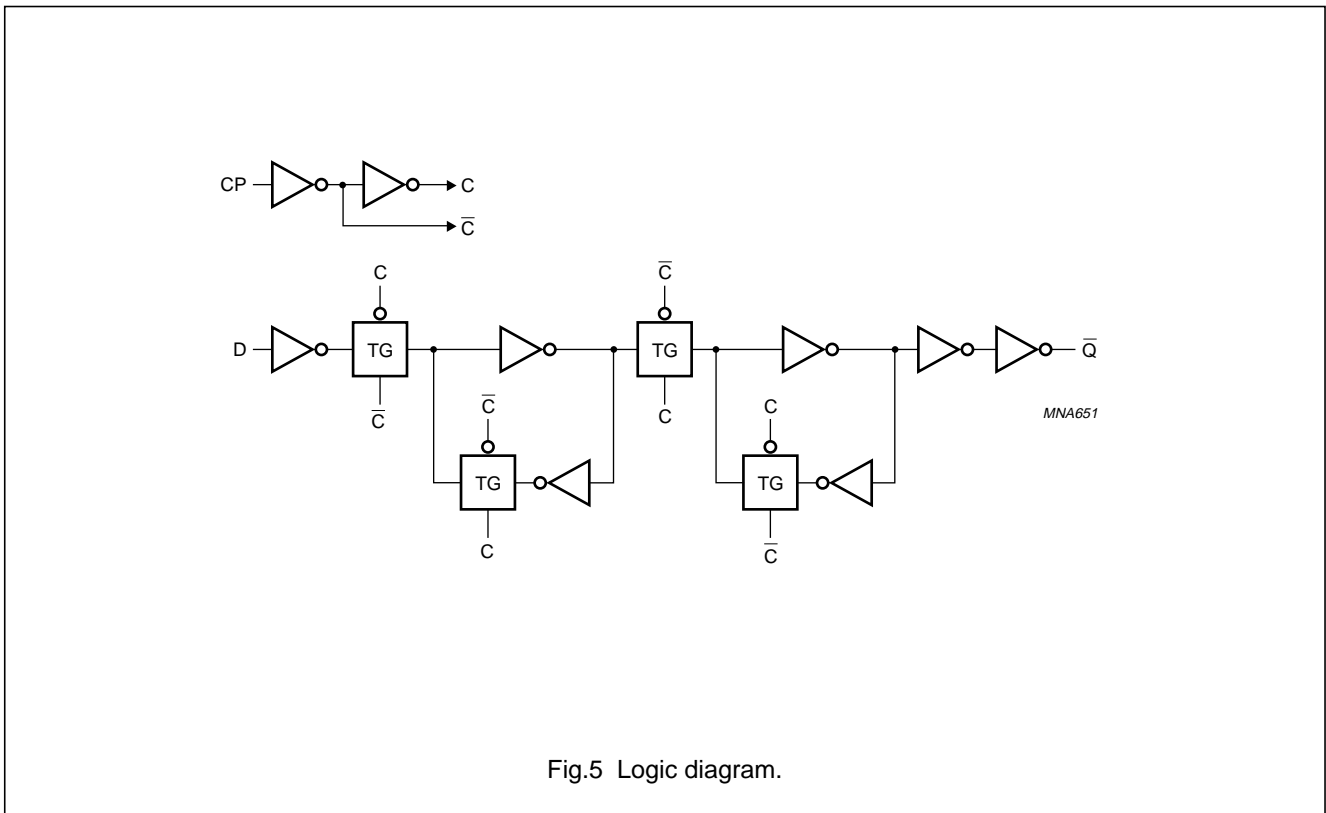
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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	active mode	0	$V_{CC}$	V
		$V_{CC} = 0$ V; Power-down mode	0	5.5	V
$T_{amb}$	operating ambient temperature		-40	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$ V	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
$V_O$	output voltage	active mode; note 1	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; note 1	-0.5	+6.5	V
$I_O$	output source or sink current	$V_O = 0$ V to $V_{CC}$	-	±50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	±100	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ °C to +125 °C	-	250	mW

## Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
T <sub>amb</sub> = -40 °C to +85 °C; note 1							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.45	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.3	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.55	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	–	–	V
		I <sub>O</sub> = -4 mA	1.65	1.2	–	–	V
		I <sub>O</sub> = -8 mA	2.3	1.9	–	–	V
		I <sub>O</sub> = -12 mA	2.7	2.2	–	–	V
		I <sub>O</sub> = -24 mA	3.0	2.3	–	–	V
		I <sub>O</sub> = -32 mA	4.5	3.8	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	5.5	–	±0.1	±5	μA
I <sub>off</sub>	power OFF leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	±0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.3 to 5.5	–	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.7	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.45	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.60	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.80	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.80	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	–	–	V
		I <sub>O</sub> = -4 mA	1.65	0.95	–	–	V
		I <sub>O</sub> = -8 mA	2.3	1.7	–	–	V
		I <sub>O</sub> = -12 mA	2.7	1.9	–	–	V
		I <sub>O</sub> = -24 mA	3.0	2.0	–	–	V
		I <sub>O</sub> = -32 mA	4.5	3.4	–	–	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	5.5	–	–	±100	μA
I <sub>off</sub>	power OFF leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	–	±200	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	200	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.3 to 5.5	–	–	5000	μA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.



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## AC CHARACTERISTICS

GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay CP to $\bar{Q}$	see Figs 6 and 8	1.65 to 1.95	1.0	3.4	9.9	ns
			2.3 to 2.7	0.5	2.3	7.0	ns
			2.7	0.5	2.5	6.0	ns
			3.0 to 3.6	0.9	2.4	5.0	ns
			4.5 to 5.5	0.5	1.8	4.5	ns
t <sub>su</sub>	set-up time D to CP	see Figs 7 and 8	1.65 to 1.95	2.3	0.8	–	ns
			2.3 to 2.7	1.5	0.6	–	ns
			2.7	1.5	0.5	–	ns
			3.0 to 3.6	1.3	0.4	–	ns
			4.5 to 5.5	1.1	0.5	–	ns
t <sub>h</sub>	hold time D to CP	see Figs 7 and 8	1.65 to 1.95	0	-0.6	–	ns
			2.3 to 2.7	0	-0.4	–	ns
			2.7	+0.5	-0.2	–	ns
			3.0 to 3.6	0.9	0.2	–	ns
			4.5 to 5.5	+0.5	-0.1	–	ns
t <sub>w</sub>	clock pulse with HIGH or LOW	see Figs 7 and 8	1.65 to 1.95	3.0	1.1	–	ns
			2.3 to 2.7	2.5	0.7	–	ns
			2.7	2.5	0.6	–	ns
			3.0 to 3.6	2.5	0.6	–	ns
			4.5 to 5.5	2.0	0.5	–	ns
f <sub>max</sub>	maximum clock pulse frequency	see Figs 7 and 8	1.65 to 1.95	160	300	–	MHz
			2.3 to 2.7	160	350	–	MHz
			2.7	160	350	–	MHz
			3.0 to 3.6	160	350	–	MHz
			4.5 to 5.5	200	400	–	MHz

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay CP to $\bar{Q}$	see Figs 6 and 8	1.65 to 1.95	1.0	–	13.0	ns
			2.3 to 2.7	0.5	–	9.0	ns
			2.7	0.5	–	8.0	ns
			3.0 to 3.6	0.9	–	6.5	ns
			4.5 to 5.5	0.5	–	6.0	ns
t <sub>su</sub>	set-up time D to CP	see Figs 7 and 8	1.65 to 1.95	2.3	–	–	ns
			2.3 to 2.7	1.5	–	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	1.3	–	–	ns
			4.5 to 5.5	1.1	–	–	ns
t <sub>h</sub>	hold time D to CP	see Figs 7 and 8	1.65 to 1.95	0	–	–	ns
			2.3 to 2.7	0	–	–	ns
			2.7	0.5	–	–	ns
			3.0 to 3.6	0.9	–	–	ns
			4.5 to 5.5	0.5	–	–	ns
t <sub>w</sub>	clock pulse with HIGH or LOW	see Figs 7 and 8	1.65 to 1.95	3.0	–	–	ns
			2.3 to 2.7	2.5	–	–	ns
			2.7	2.5	–	–	ns
			3.0 to 3.6	2.5	–	–	ns
			4.5 to 5.5	2.0	–	–	ns
f <sub>max</sub>	maximum clock pulse frequency	see Figs 7 and 8	1.65 to 1.95	160	–	–	MHz
			2.3 to 2.7	160	–	–	MHz
			2.7	160	–	–	MHz
			3.0 to 3.6	160	–	–	MHz
			4.5 to 5.5	200	–	–	MHz

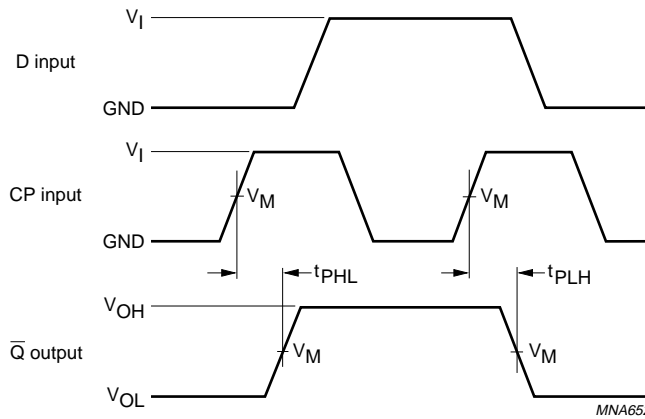
**Note**

1. All typical values are measured at T<sub>amb</sub> = 25 °C.

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AC WAVEFORMS



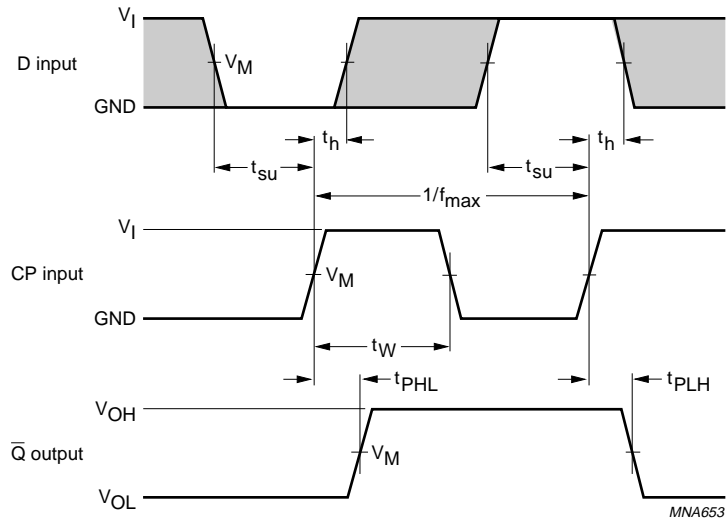
$V_{CC}$	$V_M$	INPUT	
		$V_I$	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2.0$ ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2.0$ ns
2.7 V	1.5 V	2.7 V	$\leq 2.5$ ns
3.0 V to 3.6 V	1.5 V	2.7 V	$\leq 2.5$ ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2.5$ ns

$V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.6 Clock (CP) to output ( $\bar{Q}$ ) propagation delay times.

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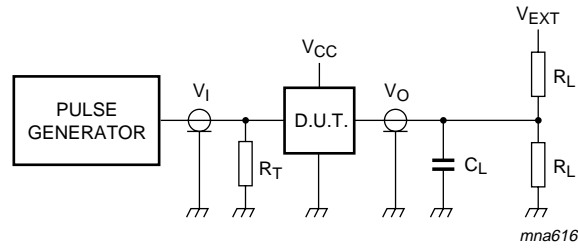
$V_{CC}$	$V_M$	INPUT	
		$V_I$	$t_r = t_f$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2.0$ ns
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2.0$ ns
2.7 V	1.5 V	2.7 V	$\leq 2.5$ ns
3.0 V to 3.6 V	1.5 V	2.7 V	$\leq 2.5$ ns
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2.5$ ns

The shaded areas indicate when the input is permitted to change for predictable output performance.  $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.7 Clock (CP) to output ( $\bar{Q}$ ) propagation delays, clock pulse width, D to CP set-up times, the D to CP hold times and maximum clock pulse frequency.

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V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.65 V to 1.95 V	V <sub>CC</sub>	30 pF	1 kΩ	open	GND	2 × V <sub>CC</sub>
2.3 V to 2.7 V	V <sub>CC</sub>	30 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V <sub>CC</sub>	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

Definitions for test circuit:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.8 Load circuitry for switching times.

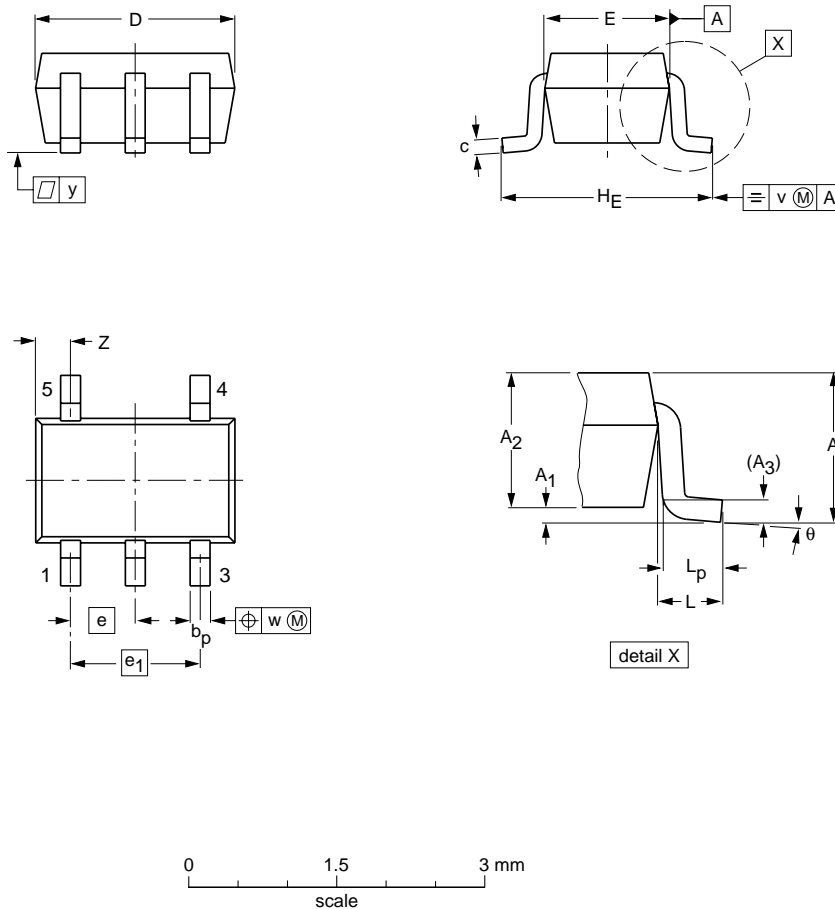
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PACKAGE OUTLINES

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

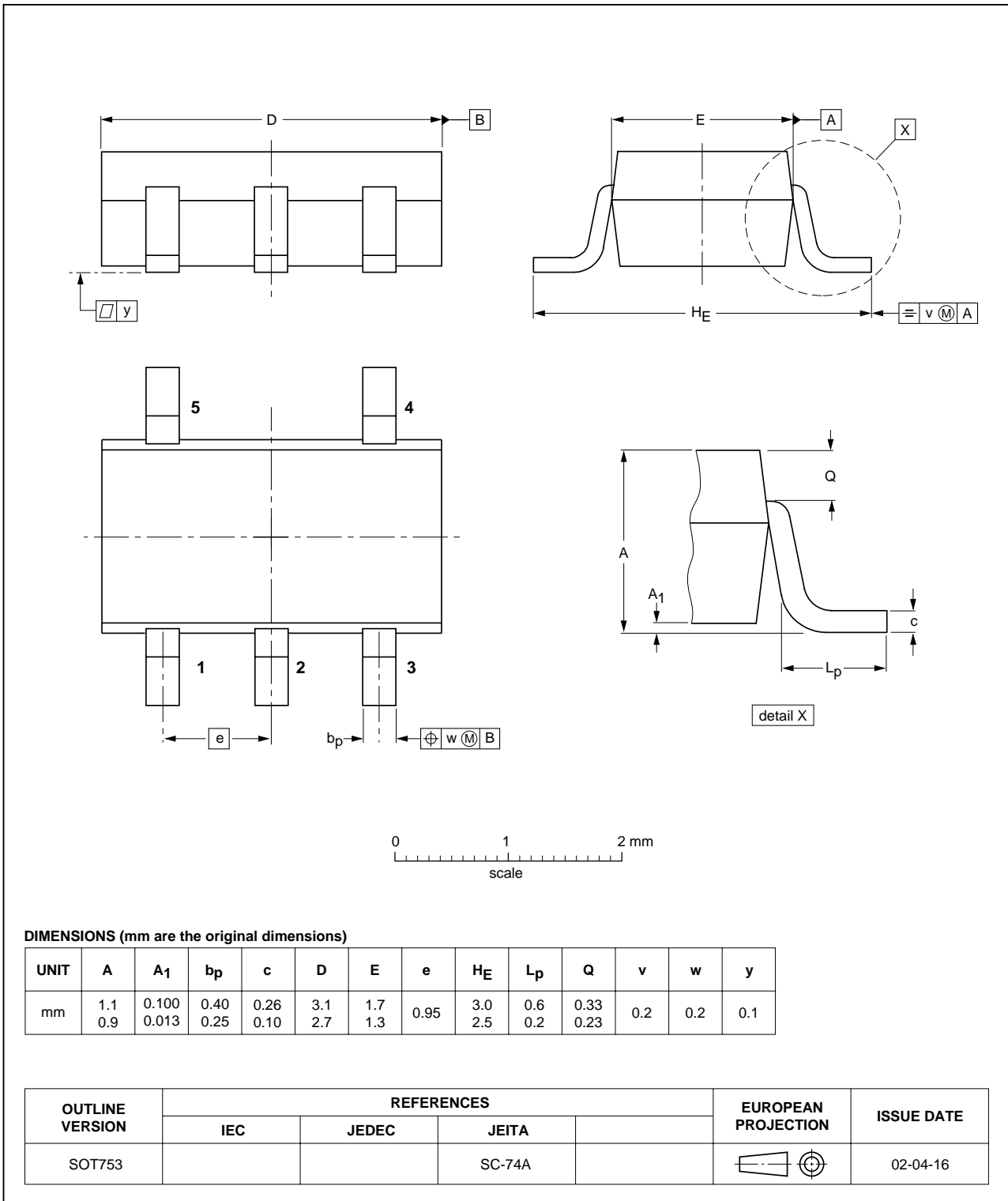
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT353-1		MO-203	SC-88A		00-09-01 03-02-19

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Plastic surface mounted package; 5 leads

SOT753

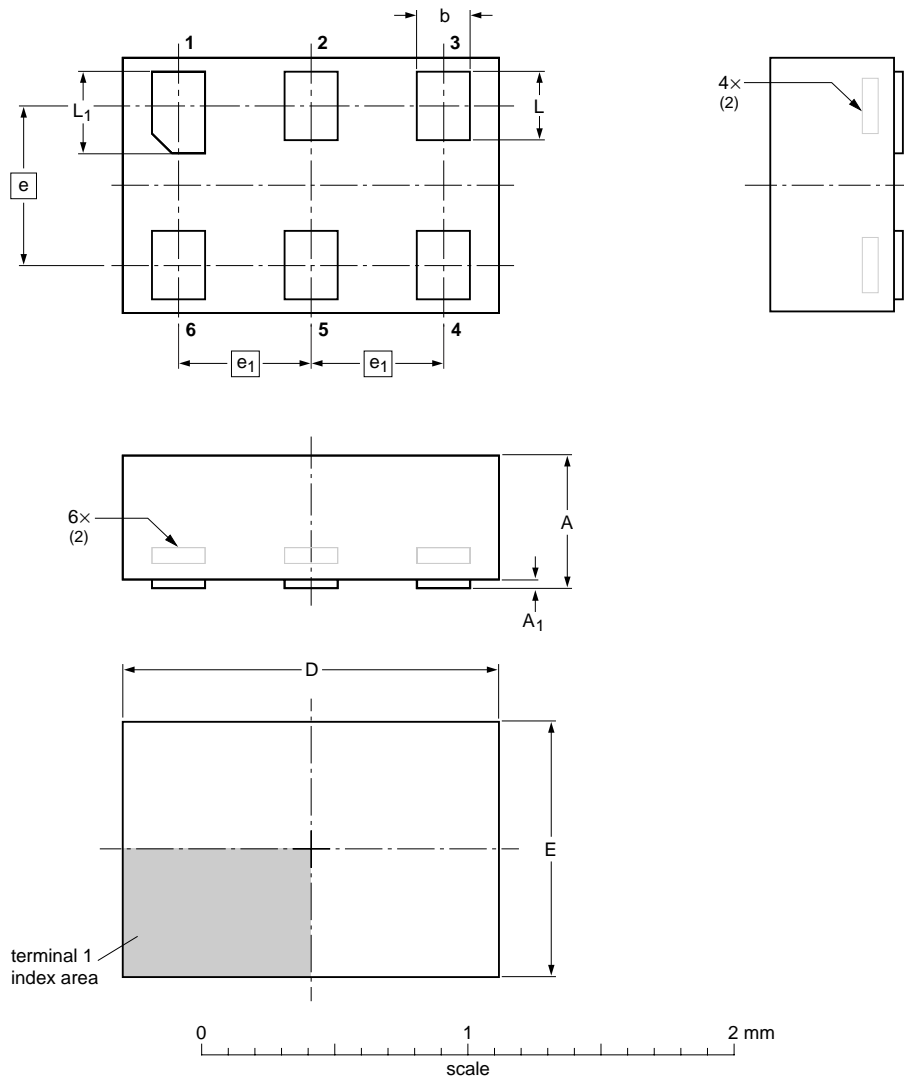


Single D-type flip-flop; positive-edge trigger

74LVC1G80

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max	A <sub>1</sub> max	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT886		MO-252			04-07-15 04-07-22



## Single D-type flip-flop; positive-edge trigger

74LVC1G80

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## **Contact information**

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

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