
4AM16

Silicon N-Channel/P-Channel Power MOS FET Array

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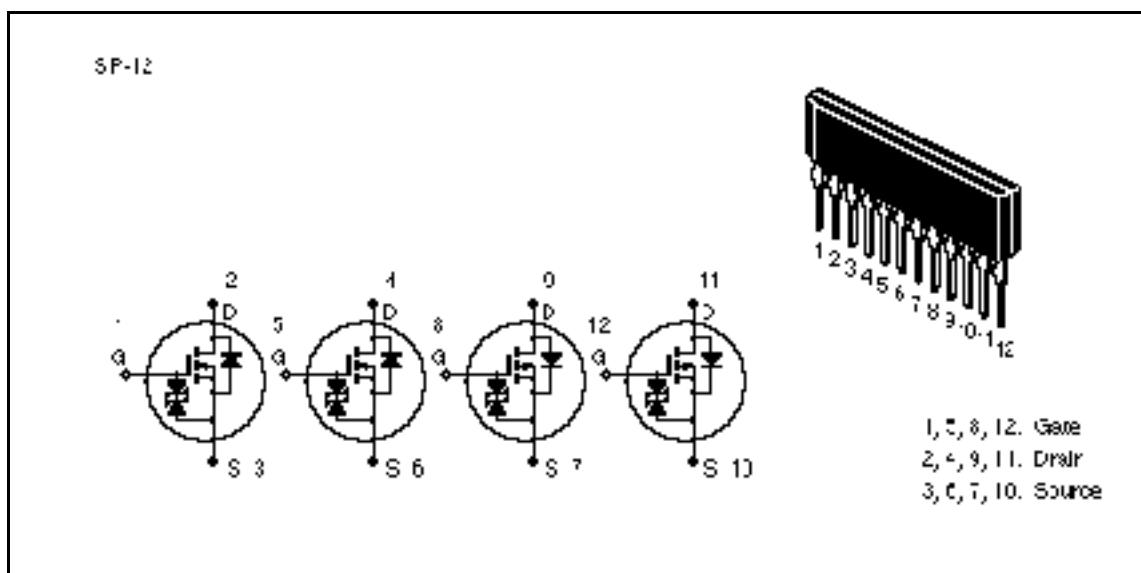
Application

High speed power switching

Features

- Low on-resistance
N Channel: $R_{DS(on)} = 0.17 \Omega$, $V_{GS} = 10 \text{ V}$, $I_D = 4 \text{ A}$
P Channel: $R_{DS(on)} = 0.2 \Omega$, $V_{GS} = -10 \text{ V}$, $I_D = -4 \text{ A}$
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline



4AM16

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		
		Nch	Pch	Unit
Drain to source voltage	V _{DSS}	60	-60	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	8	-8	A
Drain peak current	I _{D(pulse)} ^{*1}	32	-32	A
Body to drain diode reverse drain current	I _{DR}	8	-8	A
Channel dissipation	Pch (Tc = 25°C) ^{*2}	28		W
	Pch ^{*2}	4.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	-55 to +150		°C

Notes: 1. PW 10 µs, duty cycle 1%

2. 4 Device Operation

Electrical Characteristics (Ta = 25°C)

Item	Symbol	N channel			Unit	Test conditions
		Min	Typ	Max		
Drain to source breakdown voltage	V _{(BR)DSS}	60	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	±20	—	—	V	I _G = ±100 µA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	µA	V _{GS} = ±16 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-250	µA	V _{DS} = 50 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	1.0	—	2.0	V	I _D = 1 mA, V _{DS} = 10 V
Static drain to source on state resistance	R _{DS(on)}	—	0.13	0.17		I _D = 4 A, V _{GS} = 10 V ^{*1}
		—	0.18	0.24		I _D = 4 A, V _{GS} = 4 V ^{*1}
Forward transfer admittance	y _{fs}	3.5	5.5	—	S	I _D = 4 A V _{DS} = 10 V ^{*1}
Input capacitance	C _{iss}	—	400	—	pF	V _{DS} = 10 V
Output capacitance	C _{oss}	—	220	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	60	—	pF	f = 1 MHz
Turn-on delay time	t _{d(on)}	—	5	—	ns	I _D = 4 A
Rise time	t _r	—	45	—	ns	V _{GS} = 10 V
Turn-off delay time	t _{d(off)}	—	150	—	ns	R _L = 7.5
Fall time	t _f	—	85	—	ns	
Body to drain diode forward voltage	V _{DF}	—	1.2	—	V	I _F = 8 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	120	—	ns	I _F = 8 A, V _{GS} = 0, dI/dt = 50 A/µs

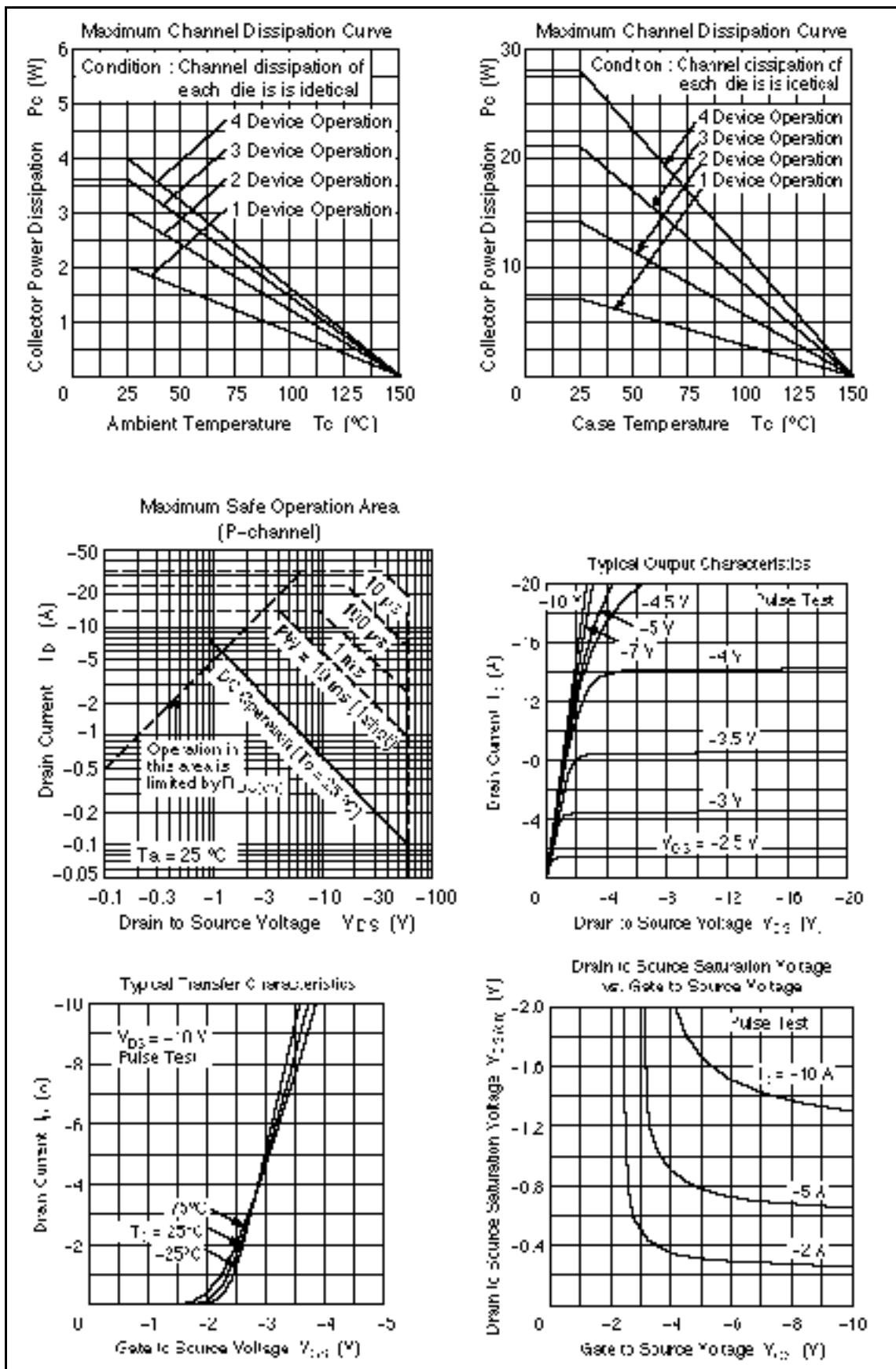
Note: 1. Pulse Test

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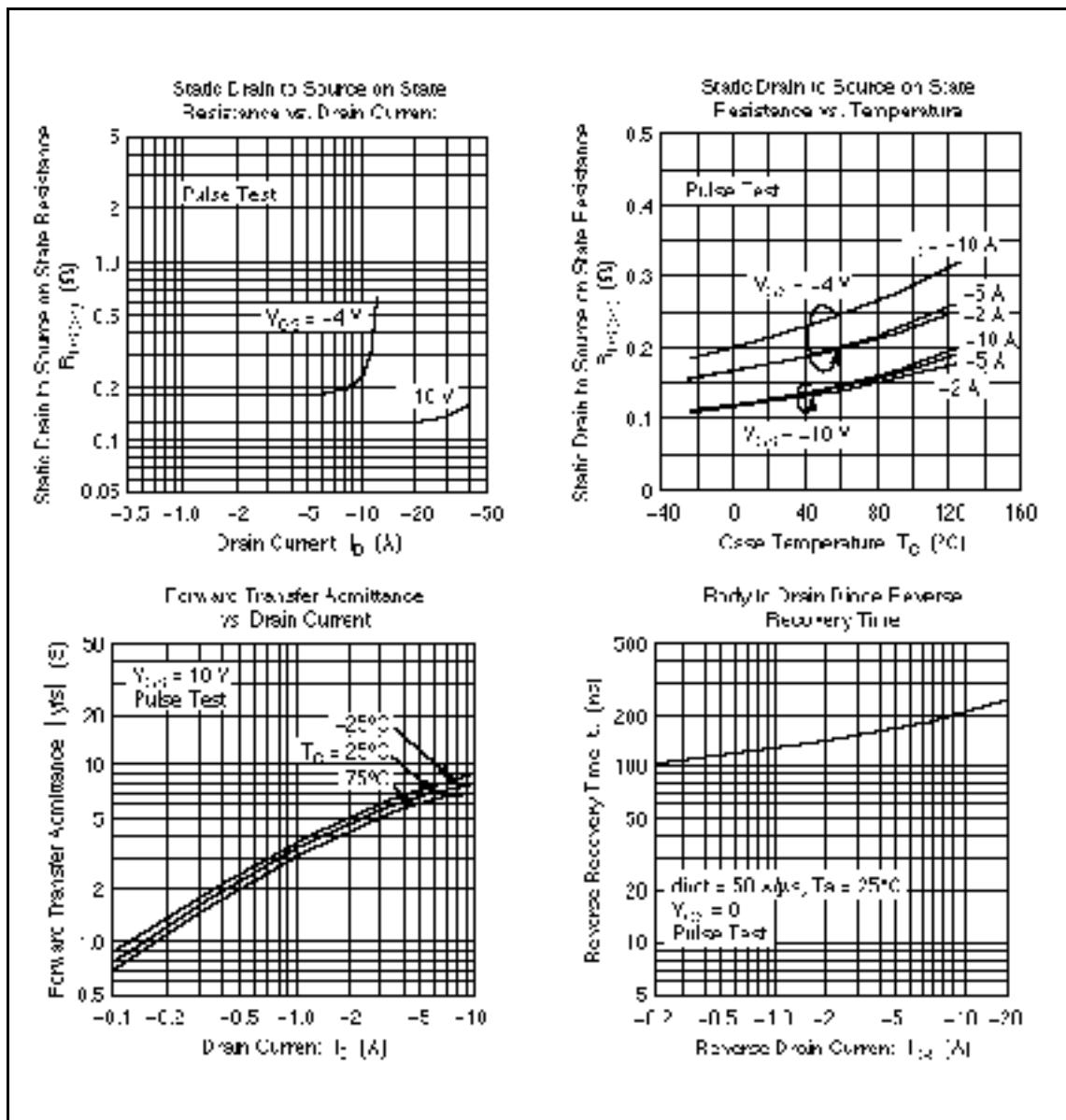
Electrical Characteristics (Ta = 25°C)

Item	Symbol	P channel			Unit	Test conditions
		Min	Typ	Max		
Drain to source breakdown voltage	V _{(BR)DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	±20	—	—	V	I _G = ±100 µA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	µA	V _{GS} = ±16 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-250	µA	V _{DS} = -50 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	-1.0	—	-2.0	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS(on)}	—	0.15	0.20		I _D = -4 A, V _{GS} = -10 V ^{*1}
		—	0.20	0.27		I _D = -4 A, V _{GS} = -4 V ^{*1}
Forward transfer admittance	y _{fs}	3.5	6.0	—	S	I _D = -4 A V _{DS} = -10 V ^{*1}
Input capacitance	C _{iss}	—	900	—	pF	V _{DS} = -10 V
Output capacitance	C _{oss}	—	460	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	130	—	pF	f = 1 MHz
Turn-on delay time	t _{d(on)}	—	8	—	ns	I _D = -4 A
Rise time	t _r	—	50	—	ns	V _{GS} = -10 V
Turn-off delay time	t _{d(off)}	—	180	—	ns	R _L = 7.5
Fall time	t _f	—	95	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-1.2	—	V	I _F = -8 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	185	—	ns	I _F = -8 A, V _{GS} = 0, dI/dt = 50 A/µs

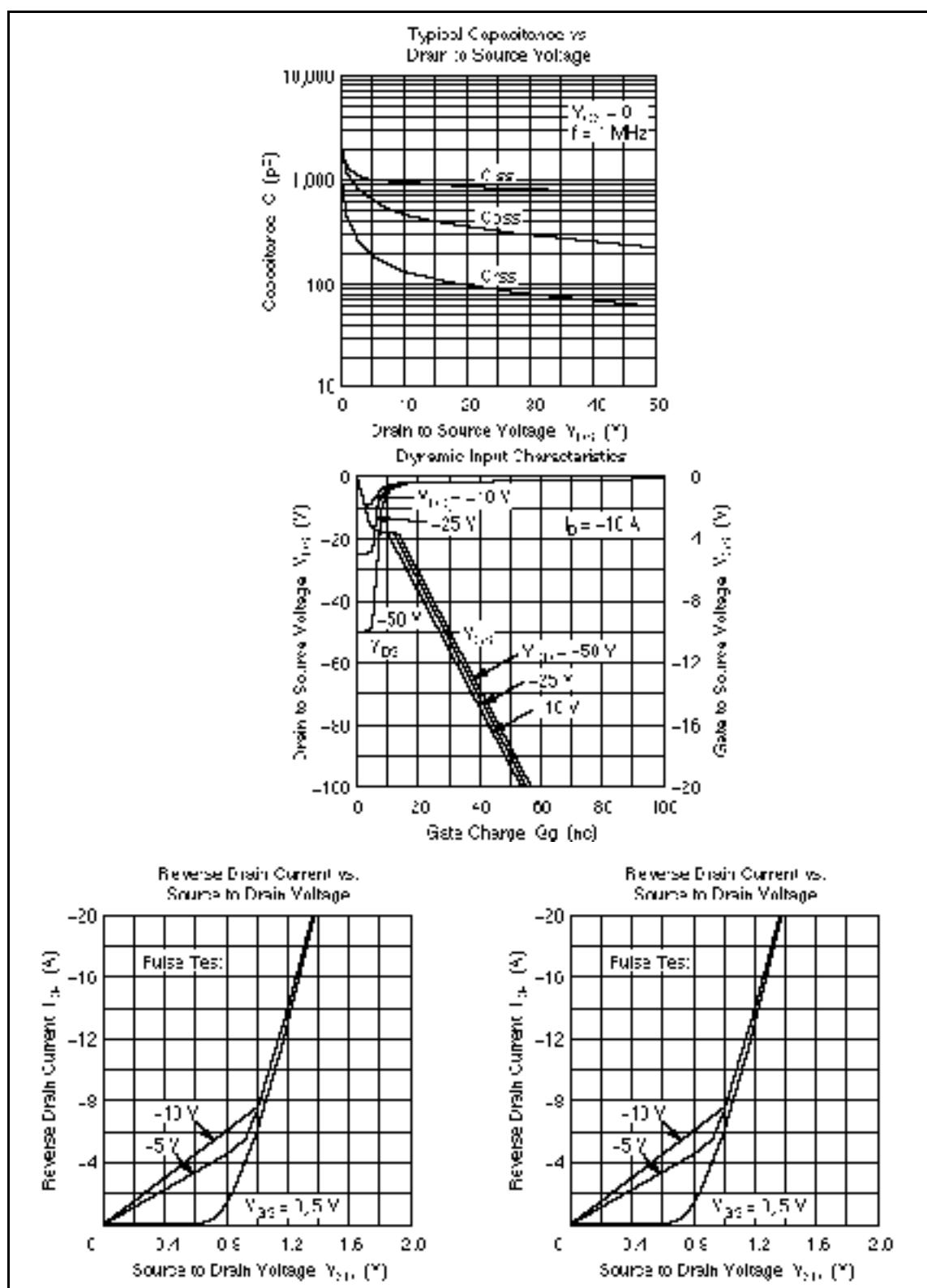
Note: 1. Pulse Test



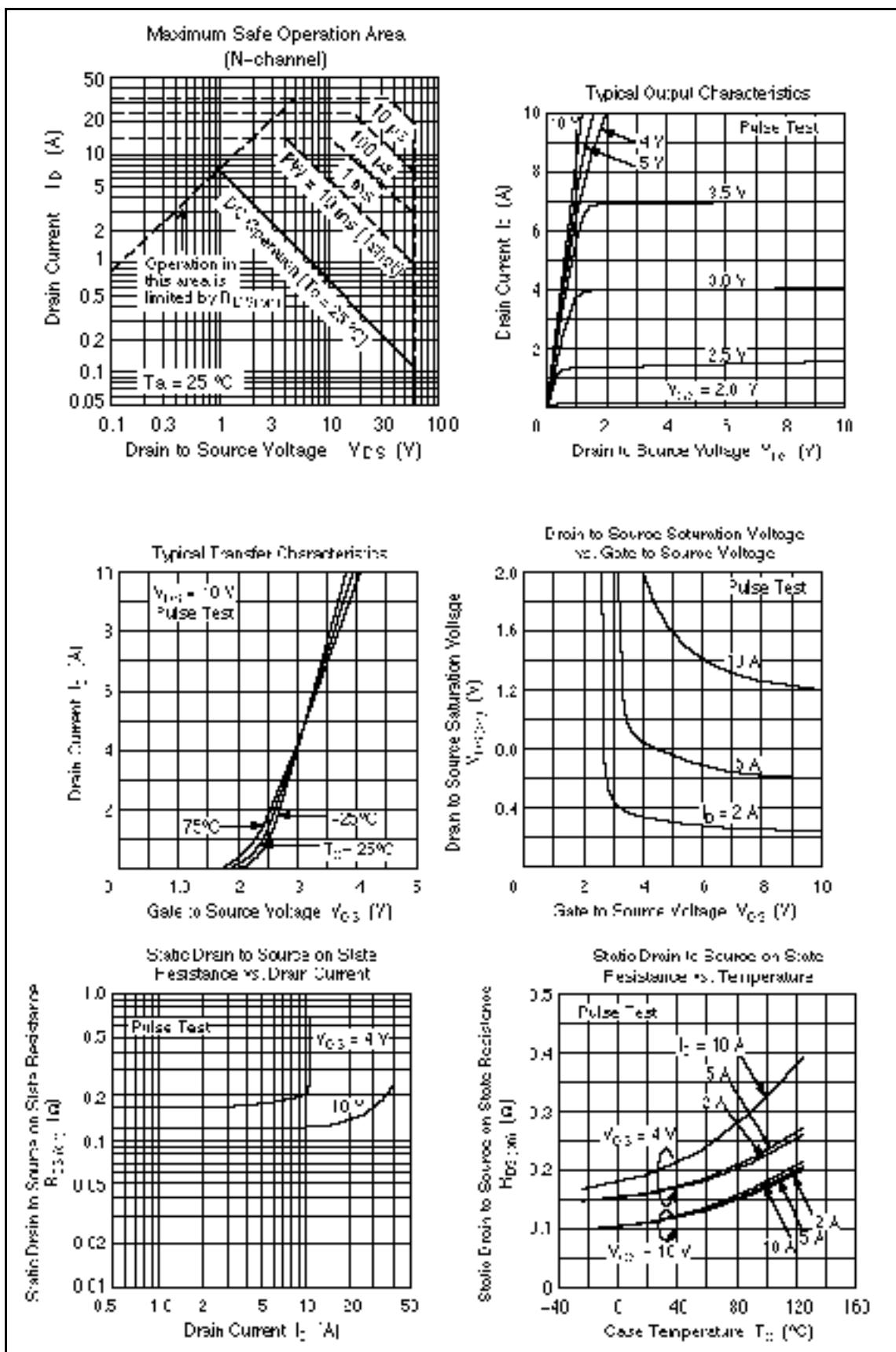
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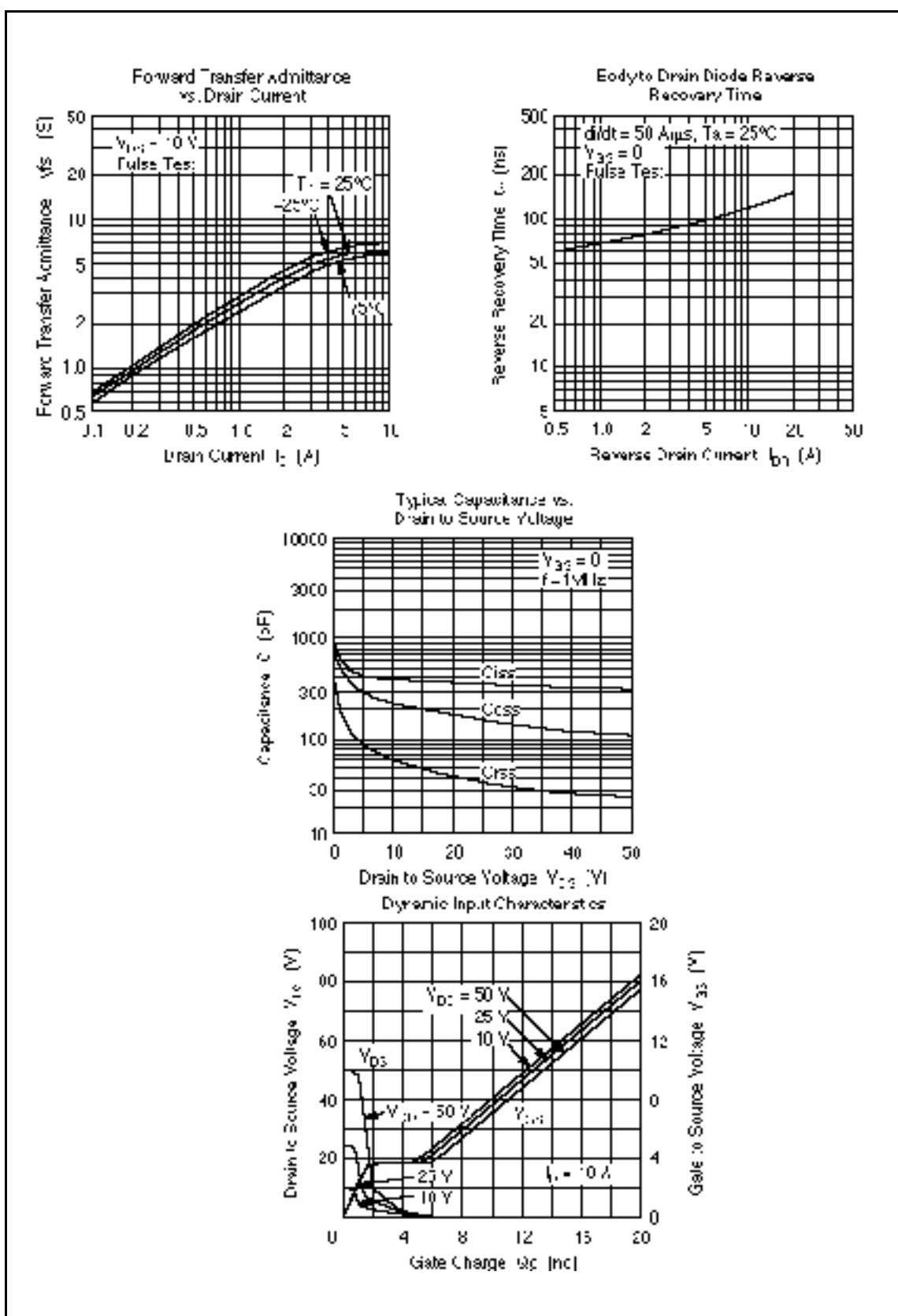
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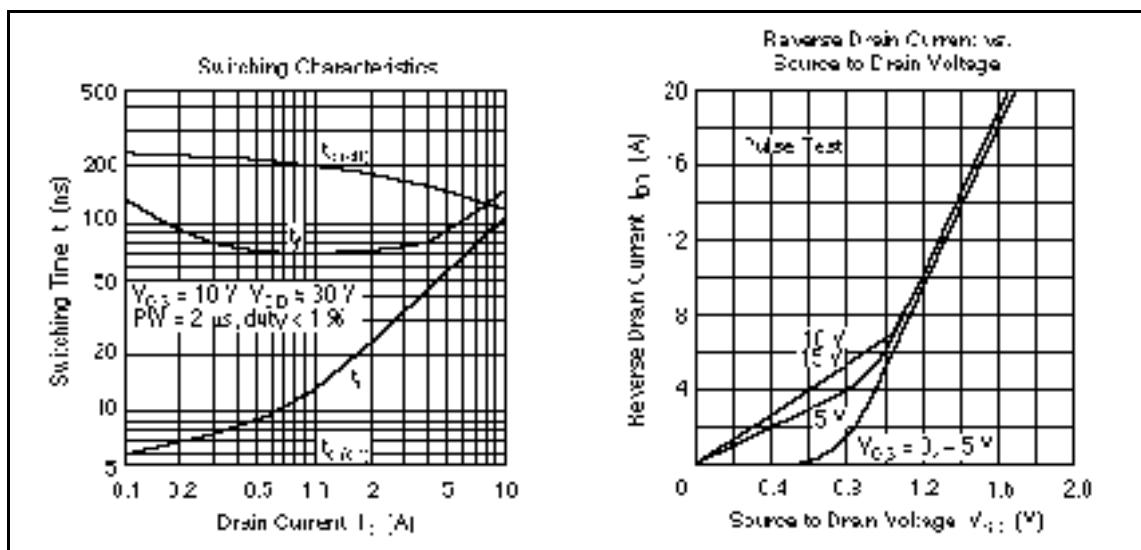
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HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.

Nippon Bldg., 2-6-2, Otemachi, Chiyoda-ku, Tokyo 100, Japan

Tel Tokyo (03) 3270-2411

Fax (03) 3270-5100

For further information write to:

Hitachi America, Ltd.

Semiconductor & IC Div.

2000 Sierra Point Parkway

Brisbane, CA. 94005-4835

U.S.A.

Tel 415-599-8300

Fax 415-599-4207

Hitachi Europe GmbH

Electronic Components Group

Continental Europe

Darmacher Straße 3

D-85522 Fildkirchen

München

Tel 089-9 91 80-0

Fax 089-9 29 30 00

Hitachi Europe Ltd.

Electronic Components Div.

Northern Europe Headquarters

Whitebrook Park

Lower Cookham Road

Maidenhead

Berkshire SL6 8YH

United Kingdom

Tel 0628-585000

Fax 0628-779322

Hitachi Asia Pte. Ltd.

#6 Collyer Quay #20-00

Hitachi Tower

Singapore 0104

Tel 535-2100

Fax 535-1533

Hitachi Asia (Hong Kong) Ltd.

Unit 705, North Tower,

World Finance Centre

Harbour City, Canton Road

Tsim Sha Tsui, Kowloon

Hong Kong

Tel 27359218

Fax 27306074