4532B
8-INPUT PRIORITY ENCODER

OBSOLETE

DESCRIPTION – The 4532B is an 8-Input Priority Encoder with eight active HIGH Priority Inputs (I_0-I_7), three active HIGH Address Outputs (A_0-A_2), an active HIGH Enable Input (E_{In}), an active HIGH Enable Output (E_{Out}) and an active HIGH Group Select Output (GS).

Data is accepted on the eight Priority Inputs (I_0-I_7). The binary code corresponding to the highest Priority Input (I_0-I_7) which is HIGH is generated on the Address Outputs (A_0-A_2) if the Enable Input (E_{In}) is HIGH. Priority Input I_7 is assigned the highest priority. The Group Select output (GS) is HIGH when one or more Priority Inputs (I_0-I_7) and the Enable Input (E_{In}) are HIGH. The Enable Output (E_{Out}) is HIGH when all the Priority Inputs (I_0-I_7) are LOW and the Enable Input (E_{In}) is HIGH. The Enable Input (E_{In}) when LOW, forces all Outputs (A_0-A_2, GS, E_{Out}) LOW.

- **ACTIVE HIGH PRIORITY INPUTS**
- **CASCADABLE**

PIN NAMES

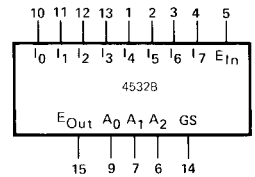
I_0-I_7	Priority Inputs
E_{In}	Enable Input
E_{Out}	Enable Output
GS	Group Select Output
A_0-A_2	Address Outputs

TRUTH TABLE

INPUTS									OUTPUTS				
E_{In}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	A_2	A_1	A_0	E_{Out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

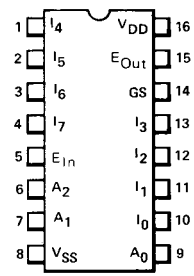
X = Don't Care (Either HIGH or LOW)
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



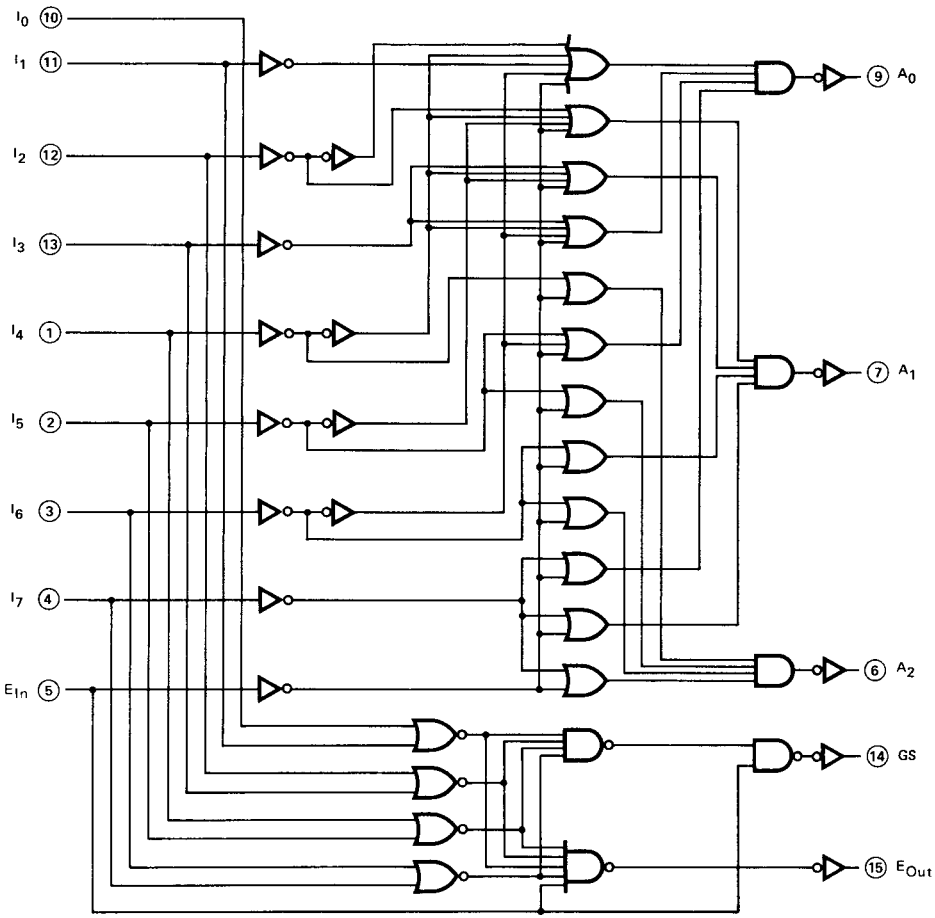
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMIT									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, E_{In} to E_{Out}		85	200		45	90		35	70	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ≤ 20 ns
t_{PHL}			85	200		45	90		35	70		
t_{PLH}	Propagation Delay, E_{In} to GS		65	150		35	70		25	56	ns	
t_{PHL}			65	150		35	70		25	56		
t_{PLH}	Propagation Delay, E_{In} to A_n		70	200		35	90		30	70	ns	
t_{PHL}			70	200		35	90		30	70		
t_{PLH}	Propagation Delay, I_n to A_n		70	200		35	90		30	70	ns	
t_{PHL}			70	200		35	90		30	70		
t_{PLH}	Propagation Delay, I_n to GS		75	200		40	90		31	70	ns	
t_{PHL}			70	200		35	90		28	70		
t_{TLH}	Output Transition Time		65	135		35	75		15	45	ns	
t_{THL}			65	135		35	75		15	45		

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characterisitcs.