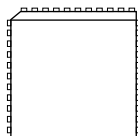


# 3935

## 3-PHASE POWER MOSFET CONTROLLER — For Automotive Applications

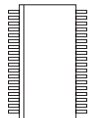
Package ED, 44-Pin PLCC



Package JP, 48-Pin LQFP



Package LQ, 36-Pin SOIC



### ABSOLUTE MAXIMUM RATINGS

Load Supply Voltages, VBAT, VDRAIN, VBOOST, BOOSTD ... **-0.6 V to 40 V**

Output Voltage Ranges,

GHA/GHB/GHC, V<sub>GHX</sub> .. **-4 V to 55 V**

SA/SB/SC, V<sub>SX</sub> ..... **-4 V to 40 V**

GLA/GLB/GLC, V<sub>GLX</sub> .... **-4 V to 16 V**

CA/CB/CC, V<sub>CX</sub> ..... **-0.6 V to 55 V**

Sense Circuit Voltages,

CSP, CSN, LSS ..... **-4 V to 6.5 V**

Logic Supply Voltage,

V<sub>DD</sub> ..... **-0.3 V to +6.5 V**

Logic Input/Outputs and OVSET, BOOSTS,

CSOUT, VDSTH ..... **-0.3 V to 6.5 V**

Operating Temperature Range,

T<sub>A</sub> ..... **-40°C to +135°C**

Junction Temperature, T<sub>J</sub> ..... **+150°C**

Storage Temperature Range,

T<sub>S</sub> ..... **-55°C to +150°C**

\* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

The A3935 is designed specifically for automotive applications that require high-power motors. Each provides six high-current gate drive outputs capable of driving a wide range of n-channel power MOSFETs.

A requirement of automotive systems is steady operation over a varying battery input range. The A3935 integrates a pulse-frequency modulated boost converter to create a constant supply voltage for driving the external MOSFETs. Bootstrap capacitors are utilized to provide the above battery supply voltage required for n-channel FETs.

Direct control of each gate output is possible via six TTL-compatible inputs. A differential amplifier is integrated to allow accurate measurement of the current in the three-phase bridge.

Diagnostic outputs can be continuously monitored to protect the driver from short-to-battery, short-to-supply, bridge-open, and battery under/overvoltage conditions. Additional protection features include dead-time, VDD undervoltage, and thermal shutdown.

The A3935 is supplied in a choice of three packages, a 44-lead PLCC with copper batwing tabs (suffix ED), a 48-lead low profile QFP with exposed thermal pad (suffix JP), and a 36-lead 0.8 mm pitch SOIC (suffix LQ).

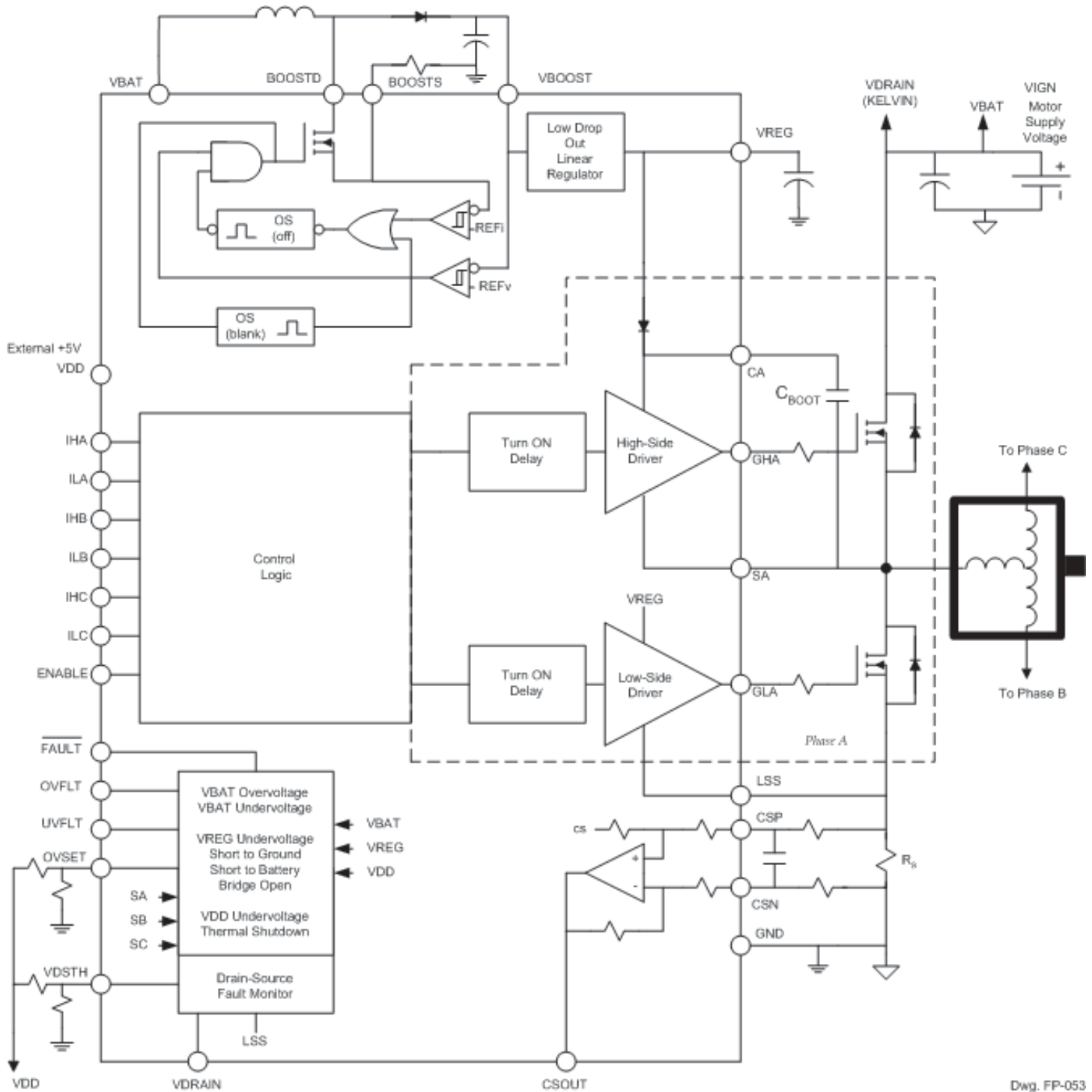
### FEATURES

- Drives wide range of n-channel MOSFETs in 3-phase bridges
- PFM boost converter for use with low-voltage battery supplies
- Internal LDO regulator for gate-driver supply
- Bootstrap circuits for high-side gate drivers
- Current monitor output
- Adjustable battery overvoltage detection.
- Diagnostic outputs
- Motor lead short-to-battery, short-to-ground, and bridge-open protection
- Undervoltage protection
- -40 °C to +150 °C, T<sub>J</sub> operation
- Thermal shutdown

Always order by complete part number, e.g., **A3935KLQ**.

# 3935 THREE-PHASE POWER MOSFET CONTROLLER

## Functional Block Diagram



Dwg. FP-053

See pages 8 and 9 for terminal assignments and descriptions.

# 3935 THREE-PHASE POWER MOSFET CONTROLLER

**A3935KED (PLCC)**

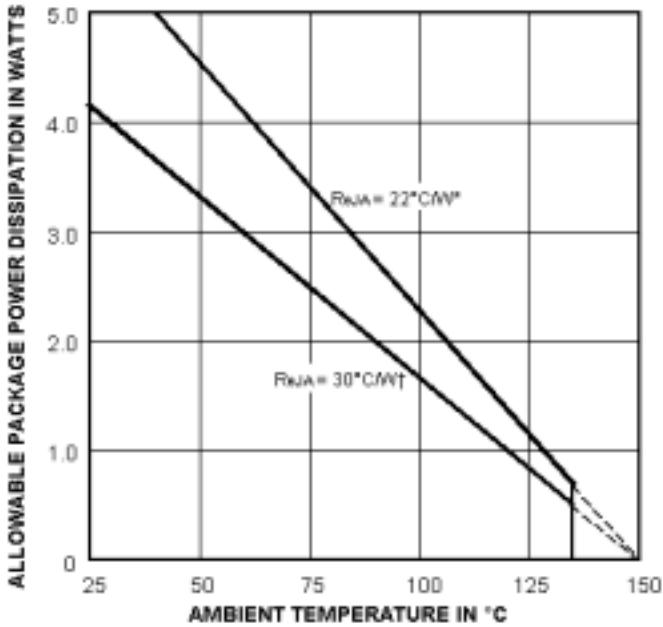


Fig. GP-019-4

**A3935KLQ (SOIC)**

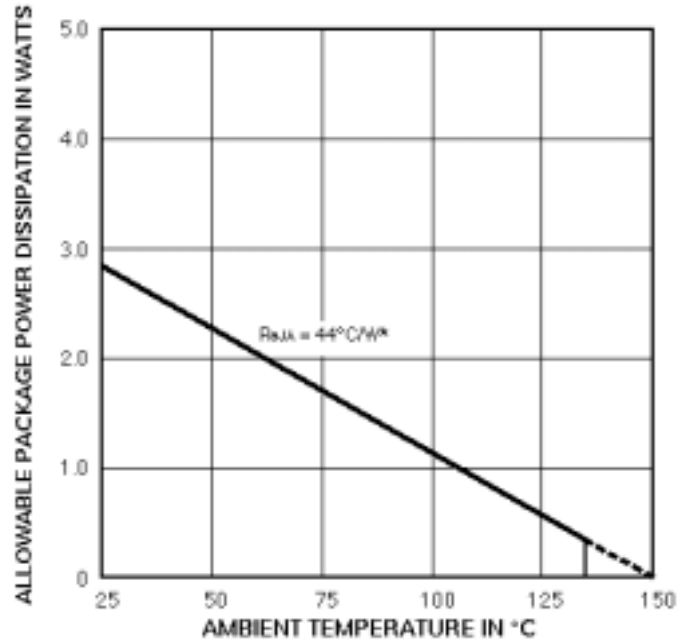


Fig. GP-018-5

\* Measured on “High-K” multi-layer PWB per JEDEC Standard JESD51-7.

† Measured on typical two-sided PWB with power tabs (terminals 1, 2, 11, 12, 22, 23, 34, and 35) connected to copper foil with an area of 3.8 square inches (2452 mm<sup>2</sup>) on each side. See Application Note 29501.5, *Improving Batwing Power Dissipation*, for additional information.

# 3935

## THREE-PHASE POWER MOSFET CONTROLLER

**ELECTRICAL CHARACTERISTICS:** unless otherwise noted at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{\text{BAT}} = 7\text{ V}$  to  $16\text{ V}$ ,  $V_{\text{DD}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ,  $\text{ENABLE} = 22.5\text{ kHz}$ ,  $50\%$  Duty Cycle, Two Phases Active.

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
<b>Power Supply</b>						
$V_{\text{DD}}$ Supply Current	$I_{\text{DD}}$	All logic inputs = 0 V	–	–	7.0	mA
$V_{\text{BAT}}$ Supply Current	$I_{\text{BAT}}$	All logic inputs = 0 V	–	–	3.0	mA
Battery Voltage Operating Range	$V_{\text{BAT}}$		7.0	–	40	V
Bootstrap Diode Forward Voltage	$V_{\text{DBOOT}}$	$I_{\text{DBOOT}} = -I_{\text{CX}} = 10\text{ mA}$ , $V_{\text{DBOOT}} = V_{\text{REG}} - V_{\text{CX}}$	0.8	–	2.0	V
		$I_{\text{DBOOT}} = -I_{\text{CX}} = 100\text{ mA}$	1.5	–	2.3	V
Bootstrap Diode Resistance	$r_{\text{DBOOT}}$	$r_{\text{D}}(100\text{ mA}) = [V_{\text{D}}(150\text{ mA}) - V_{\text{D}}(50\text{ mA})]/100\text{ mA}$	2.5	–	7.5	$\Omega$
Bootstrap Diode Current Limit	$I_{\text{DM}}$	$3\text{ V} < [V_{\text{REG}} - V_{\text{CX}}] < 12\text{ V}$	-150	–	-1150	mA
Bootstrap Quiescent Current	$I_{\text{CX}}$	$V_{\text{CX}} = 40\text{ V}$ , $\text{GHX} = \text{ON}$	10	–	30	$\mu\text{A}$
Bootstrap Refresh Time	$t_{\text{refresh}}$	$V_{\text{SX}} = \text{low}$ to guarantee $\Delta V = +0.5\text{ V}$ refresh of $0.47\text{ }\mu\text{F}$ Boot Cap at $V_{\text{CX}} - V_{\text{SX}} = +10\text{ V}$	–	–	2.0	$\mu\text{s}$
VREG Output Voltage <sup>1</sup>	$V_{\text{REG}}$	$V_{\text{BAT}} = 7\text{ V}$ to $40\text{ V}$ , $V_{\text{BOOST}}$ from Boost Reg	12.7	–	14	V
VREG Dropout Voltage <sup>2</sup>	$V_{\text{REGDO}}$	$V_{\text{REGDO}} = V_{\text{boost}} - V_{\text{reg}}$ , $I_{\text{reg}} = 40\text{ mA}$	–	0.9	–	V
Gate Drive Avg. Supply Current	$I_{\text{REG}}$	No external dc load at VREG, $C_{\text{REG}} = 10\text{ }\mu\text{F}$	–	–	40	mA
VREG Input Bias Current	$I_{\text{REGBIAS}}$	Current into $V_{\text{BOOST}}$ , $\text{ENABLE} = 0$	–	–	4.0	mA
<b>Boost Supply</b>						
$V_{\text{BOOST}}$ Output Voltage Limit	$V_{\text{BOOSTM}}$	$V_{\text{BAT}} = 7\text{ V}$	14.9	–	16.3	V
$V_{\text{BOOST}}$ Output Volt. Limit Hyst.	$\Delta V_{\text{BOOSTM}}$		35	–	180	mV
Boost Switch ON Resistance	$r_{\text{DS(on)}}$	$I_{\text{BOOSTD}} < 300\text{ mA}$	–	1.4	3.3	$\Omega$
Max. Boost Switch Current	$I_{\text{BOOSTSW}}$		–	–	300	mA
Boost Current Limit Threshold Volt.	$V_{\text{BI(th)}}$	Increasing $V_{\text{BOOSTS}}$	0.45	–	0.55	V
OFF Time	$t_{\text{off}}$		3.0	–	8.0	$\mu\text{s}$
Blanking Time	$t_{\text{blank}}$		100	–	220	ns

NOTES: Typical Data and Typical Characteristics are for design information only.

Negative current is defined as coming out of (sourcing) the specified device terminal.

1. For  $V_{\text{BOOSTM}} < V_{\text{BOOST}} < 40\text{ V}$  power dissipation in the  $V_{\text{REG}}$  LDO increases. Observe  $T_J < 150^\circ\text{C}$  limit.

2. With  $V_{\text{BOOST}}$  decreasing Dropout Voltage measured at  $V_{\text{REG}} = V_{\text{REGref}} - 200\text{ mV}$  where  $V_{\text{REG(ref)}} = V_{\text{REG}}$  at  $V_{\text{BOOST}} = 16\text{ V}$ .

# 3935 THREE-PHASE POWER MOSFET CONTROLLER

**ELECTRICAL CHARACTERISTICS:** unless otherwise noted at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{\text{BAT}} = 7\text{ V}$  to  $16\text{ V}$ ,  $V_{\text{DD}} = 4.75\text{ V}$  to  $5.25\text{ V}$ , **ENABLE = 22.5 kHz, 50% Duty Cycle, Two Phases Active.**

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
<b>Control Logic</b>						
Logic Input Voltages	$V_{I(1)}$	Minimum high level input for logical "one"	2.0	–	–	V
	$V_{I(0)}$	Maximum low level input for logical "zero"	–	–	0.8	V
Logic Input Currents	$I_{I(1)}$	$V_I = V_{\text{DD}}$	–	–	500	$\mu\text{A}$
	$I_{I(0)}$	$V_I = 0.8\text{ V}$	50	–	–	$\mu\text{A}$
Input Hysteresis	$V_{\text{hys}}$		100	–	300	mV
Logic Output High Voltage	$V_{O(H)}$	$I_{O(H)} = -800\text{ uA}$	$V_{\text{DD}}-0.8$	–	–	V
Logic Output Low Voltage	$V_{I(L)}$	$I_{O(L)} = 1.6\text{ mA}$	–	–	0.4	V
<b>Gate Drives, GHx ( internal SOURCE or upper switch stages)</b>						
Output High Voltage	$V_{\text{DSL(H)}}$	GHx: $I_{\text{xU}} = -10\text{ mA}$ , $V_{\text{sx}} = 0$	$V_{\text{REG}}-2.26$	–	$V_{\text{REG}}$	V
		GLx: $I_{\text{xU}} = -10\text{ mA}$ , $V_{\text{lss}} = 0$	$V_{\text{REG}}-0.26$	–	$V_{\text{REG}}$	V
Source Current (pulsed)	$I_{\text{xU}}$	$V_{\text{SDU}} = 10\text{ V}$ , $T_J = 25^\circ\text{C}$	–	800	–	mA
		$V_{\text{SDU}} = 10\text{ V}$ , $T_J = 135^\circ\text{C}$	400	–	–	mA
Source ON Resistance	$r_{\text{SDU(on)}}$	$I_{\text{xU}} = -150\text{ mA}$ , $T_J = 25^\circ\text{C}$	4.0	–	10	$\Omega$
		$I_{\text{xU}} = -150\text{ mA}$ , $T_J = 135^\circ\text{C}$	7.0	–	15	$\Omega$
<b>Gate Drives, GLx ( internal SINK or lower switch stages)</b>						
Sink Current (pulsed)	$I_{\text{xL}}$	$V_{\text{DSL}} = 10\text{ V}$ , $T_J = 25^\circ\text{C}$	–	850	–	mA
		$V_{\text{DSL}} = 10\text{ V}$ , $T_J = 135^\circ\text{C}$	550	–	–	mA
Sink ON Resistance	$r_{\text{DSL(on)}}$	$I_{\text{xL}} = +150\text{ mA}$ , $T_J = 25^\circ\text{C}$	1.8	–	6.0	$\Omega$
		$I_{\text{xL}} = +150\text{ mA}$ , $T_J = 135^\circ\text{C}$	3.0	–	7.5	$\Omega$
<b>Gate Drives, GHx, GLx (General)</b>						
Propagation Delay, Logic only	$t_{\text{pd}}$	Logic input to unloaded GHx, GLx	–	–	150	ns
Output Skew Time	$t_{\text{sk(o)}}$	Grouped by edge, phase-to-phase	–	–	50	ns
Dead Time (Shoot-Through Prevention)	$t_{\text{dead}}$	Between GHx, GLx transitions of same phase	75	–	180	ns

NOTES: Typical Data and Typical Characteristics are for design information only.  
 Negative current is defined as coming out of (sourcing) the specified device terminal.  
 For GHx:  $V_{\text{SDU}} = V_{\text{CX}} - V_{\text{GHx}}$ ,  $V_{\text{DSL}} = V_{\text{GHx}} - V_{\text{SX}}$ ,  $V_{\text{DSL(H)}} = V_{\text{CX}} - V_{\text{SDU}} - V_{\text{SX}}$ .  
 For GLx:  $V_{\text{SDU}} = V_{\text{REG}} - V_{\text{GLx}}$ ,  $V_{\text{DSL}} = V_{\text{GLx}} - V_{\text{LSS}}$ ,  $V_{\text{DSL(H)}} = V_{\text{REG}} - V_{\text{SDU}} - V_{\text{LSS}}$ .

# 3935

## THREE-PHASE POWER MOSFET CONTROLLER

**ELECTRICAL CHARACTERISTICS:** unless otherwise noted at  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 7\text{ V}$  to  $16\text{ V}$ ,  $V_{\text{DD}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ,  $\text{ENABLE} = 22.5\text{ kHz}$ , 50% Duty Cycle, Two Phases Active.

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
<b>Sense Amplifier</b>						
Input Bias Current	$I_{\text{bias}}$	$\text{CSP} = \text{CSN} = 0\text{ V}$	-180	–	-360	$\mu\text{A}$
Input Offset Current	$I_{\text{IO}}$	$\text{CSP} = \text{CSN} = 0\text{ V}$	–	–	$\pm 35$	$\mu\text{A}$
Input Resistance	$r_i$	CSP with respect to GND	–	80	–	$\text{k}\Omega$
		CSN with respect to GND	–	4.0	–	$\text{k}\Omega$
Diff. Input Operating Voltage	$V_{\text{ID}}$	$V_{\text{ID}} = \text{CSP} - \text{CSN}$ , $-1.3\text{V} < \text{CSP}, \text{N} < 4\text{V}$	–	–	$\pm 200$	mV
Output Offset Voltage	$V_{\text{OO}}$	$\text{CSP} = \text{CSN} = 0\text{ V}$	77	250	450	mV
Output Offset Voltage Drift	$\Delta V_{\text{OO}}$	$\text{CSP} = \text{CSN} = 0\text{ V}$	–	100	–	$\mu\text{V}/^{\circ}\text{C}$
Input Com-Mode Oper. Range	$V_{\text{IC}}$	$\text{CSP} = \text{CSN}$	-1.5	–	4.0	V
Voltage Gain	$A_V$	$V_{\text{ID}} = 40\text{ mV}$ to $200\text{ mV}$	18.6	19.2	19.8	V/V
Low Output Voltage Error	$E_V$	$V_{\text{id}} = 0$ to $40\text{ mV}$ , $V_o = (19.2 \times V_{\text{ID}}) + V_o + E_V$	–	–	$\pm 25$	mV
DC Common-Mode Attenuation	$A_{\text{VC}}$	$\text{CSP} = \text{CSN} = 200\text{ mV}$	28	–	–	dB
Output Resistance	$r_o$	$V_{\text{CSOUT}} = 2.0\text{ V}$	–	8.0	–	$\Omega$
Output Dynamic Range	$V_{\text{CSOUT}}$	$I_{\text{CSOUT}} = -100\ \mu\text{A}$ at top rail, $100\ \mu\text{A}$ at bottom rail	0.075	–	$V_{\text{DD}} - 0.25$	V
Output Current, Sink	$I_{\text{sink}}$	$V_{\text{CSOUT}} = 2.5\text{ V}$	20	–	–	mA
Output Current, Source	$I_{\text{source}}$	$V_{\text{CSOUT}} = 2.5\text{ V}$	-1.0	–	–	mA
VDD Supply Ripple Rejection	PSRR	$\text{CSP} = \text{CSN} = \text{GND}$ , freq. = 0 to 1 MHz	20	–	–	dB
VREG Supply Ripple Rejection	PSRR	$\text{CSP} = \text{CSN} = \text{GND}$ , freq. = 0 to 300 kHz	45	–	–	dB
Small Signal 3-dB Bandwidth	$f_{3\text{dB}}$	10 mV input	–	1.6	–	MHz
AC Common-Mode Attenuation	$A_{\text{VC}}$	$V_{\text{cm}} = 250\text{ mV/pp}$ , freq. = 0 to 800 kHz	26	–	–	dB
Output Slew Rate (positive or negative)	SR	200 mV step input, meas. 10/90% points	10	–	–	V/ $\mu\text{s}$

NOTES: Typical Data and Typical Characteristics are for design information only.  
Negative current is defined as coming out of (sourcing) the specified device terminal.

# 3935 THREE-PHASE POWER MOSFET CONTROLLER

**ELECTRICAL CHARACTERISTICS:** unless otherwise noted at  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{\text{BAT}} = 7\text{ V}$  to  $16\text{ V}$ ,  $V_{\text{DD}} = 4.75\text{ V}$  to  $5.25\text{ V}$ ,  $\text{ENABLE} = 22.5\text{ kHz}$ ,  $50\%$  Duty Cycle, Two Phases Active.

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
<b>Fault Logic</b>						
VDD Undervoltage	$V_{\text{DD(}uv)}$	Decreasing $V_{\text{DD}}$	3.8	–	4.3	V
VDD Undervoltage Hysteresis	$\Delta V_{\text{DD(}uv)}$	$V_{\text{DD(recovery)}} - V_{\text{DD(}uv)}$	100	–	300	mV
OVSET Operating Volt. Range	$V_{\text{SET(}ov)}$		0	–	$V_{\text{DD}}$	V
OVSET Calibrated Volt. Range	$V_{\text{SET(}ov)}$		0	–	2.5	V
OVSET Input Current Range	$I_{\text{SET(}ov)}$		-1.0	–	+1.0	$\mu\text{A}$
VBAT Overvoltage Range	$V_{\text{BAT(}ov)}$	$0\text{ V} < V_{\text{SET(}ov)} < 2.5\text{ V}$	19.4	–	40	V
VBAT Overvoltage	$V_{\text{BAT(}ov)}$	Increasing $V_{\text{BAT}}$ , $V_{\text{SET(}ov)} = 0\text{ V}$	19.4	22.4	25.4	V
VBAT Overvoltage Hysteresis	$\Delta V_{\text{BAT(}ov)}$	Percent of $V_{\text{BAT(}ov)}$ value set by $V_{\text{SET(}ov)}$	9.0	–	15	%
VBAT Overvoltage Gain Constant	$K_{\text{BAT(}ov)}$	$V_{\text{BAT(}ov)} = (K_{\text{BAT(}ov)} \times V_{\text{SET(}ov)}) + V_{\text{BAT(}ov)}[0]$	–	12	–	V/V
VBAT Undervoltage	$V_{\text{BAT(}uv)}$	Decreasing $V_{\text{BAT}}$	5.0	5.25	5.5	V
VBAT Undervoltage Hysteresis	$\Delta V_{\text{BAT(}uv)}$	Percent of $V_{\text{BAT(}uv)}$	8.0	–	12	%
VREG Undervoltage	$V_{\text{REG(}uv)}$	Decreasing $V_{\text{REG}}$	9.9	–	11.1	V
VDSTH Input Range	$V_{\text{DSTH}}$		0.5	–	3.0	V
VDSTH Input Current	$I_{\text{DSTH}}$	$V_{\text{DSTH}} > 0.8\text{ V}$	40	–	100	$\mu\text{A}$
Short-to-Ground Threshold	$V_{\text{STG(th)}}$	With a high-side driver “on”, as $V_{\text{SX}}$ decreases, $V_{\text{DRAIN}} - V_{\text{SX}} > V_{\text{STG}}$ causes a fault	$V_{\text{DSTH}}-0.3$	–	$V_{\text{DSTH}}+0.2$	V
Short-to-Battery Threshold	$V_{\text{STB(th)}}$	With a low-side driver “on”, as $V_{\text{SX}}$ increases, $V_{\text{SX}} - V_{\text{LSS}} > V_{\text{STB}}$ causes a fault	$V_{\text{DSTH}}-0.3$	–	$V_{\text{DSTH}}+0.2$	V
$V_{\text{DRAIN}}$ /Open Bridge Oper. Range	$V_{\text{DRAIN}}$	$7\text{ V} < V_{\text{BAT}} < 40\text{ V}$	-0.3	–	$V_{\text{BAT}}+2.0$	V
$V_{\text{DRAIN}}$ /Open Bridge Current	$I_{\text{VDRAIN}}$	$7\text{ V} < V_{\text{BAT}} < 40\text{ V}$	0	–	1.0	mA
$V_{\text{DRAIN}}$ /Open Bridge Threshold Volt.	$V_{\text{BDGO(th)}}$	If $V_{\text{DRAIN}} < V_{\text{BDGO(th)}}$ then a bridge fault occurs	1.0	–	3.0	V
Thermal Shutdown Temp.	$T_J$		160	170	180	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$\Delta T_J$		7.0	10	13	$^\circ\text{C}$

NOTES: Typical Data and Typical Characteristics are for design information only.  
Negative current is defined as coming out of (sourcing) the specified device terminal.

# 3935

## THREE-PHASE POWER MOSFET CONTROLLER

### Terminal Functions

Terminal Name	Function	A3935KED (PLCC)	A3935KJP (QLFP)	A3935KLQ (SOIC)
CSP	Current-sense input, positive-side	31	19	1
VDSTH	DC input, drain-to-source monitor threshold voltage	32	20	2
LSS	Gate-drive source return, low-side	33	21	3
GLC	Gate-drive C output, low-side	36	22	4
SC	Load phase C input	37	26	5
GHC	Gate-drive C output, high-side	38	27	6
CC	Bootstrap capacitor C	39	28	7
GLB	Gate-drive B output, low-side	40	29	8
SB	Load phase B input	41	30	9
GHB	Gate-drive B output, high-side	42	31	10
CB	Bootstrap capacitor B	43	32	11
GLA	Gate-drive A output, low-side	44	33	12
SA	Load phase A input	3	34	13
GHA	Gate-drive A output, high-side	4	38	14
CA	Bootstrap capacitor A	5	39	15
VREG	Gate drive supply, positive	6	40	16
VDRAIN	Kelvin connection to MOSFET high-side drains	7	41	17
VBOOST	Boost supply output	8	42	18
BOOSTS	Boost switch, source	9	43	19
BOOSTD	Boost switch, drain	10	44	20
VBAT	Battery supply, positive	13	46	22
UVFLT	VBAT undervoltage fault output	14	3	23
OVFLT	VBAT overvoltage fault output	15	4	24
$\overline{\text{FAULT}}$	Active-low fault output, primary	16	5	25
ALO	Gate control input A, low-side	17	6	26
AHI	Gate control input A, high-side	18	7	27
BHI	Gate control input B, high-side	19	8	28
BLO	Gate control input B, low-side	20	9	29
CLO	Gate control input C, low-side	21	10	30
CHI	Gate control input C, high-side	24	11	31
ENABLE	Gate output enable	25	12	32
OVSET	DC input, overvoltage threshold setting for VBAT	26	15	33
NC	Not connected, no external connection allowed	27	1,2,13,14,23,24, 25,35,36,37,47,48	–
CSOUT	Current-sense amplifier output	28	16	34
VDD	Logic supply, nominally +5 V	29	17	35
CSN	Current-sense input, negative-side	30	18	36
GND	Ground, dc supply returns, negative, and (for ED package) heat sink tab	1, 2, 11, 12, 22, 23, 34, 35	45	21



## Terminal Descriptions

**AHI/BHI/CHI.** Direct control of high-side gate outputs GHA/GHB/GHC. Logic “1” drives the gate “on”. Logic “0” pulls the gate down, turning off the external power MOSFET. Internally pulled down when terminal is open.

**ALO/BLO/CLO.** Direct control of low-side gate outputs GLA/GLB/GLC. Logic “1” drives the gate “on”. Logic “0” pulls the gate down, turning off the external power MOSFET. Internally pulled down when terminal is open.

**BOOSTD.** Boost converter switch drain connection.

**BOOSTS.** Boost converter switch source connection.

**CA/CB/CC.** High-side connection for bootstrap capacitor, positive supply for high-side gate drive. The bootstrap capacitor is charged to VREG when the output Sx terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for n-channel power MOSFETs.

**CSN.** Input for current-sense, differential amplifier, inverting, negative side. Kelvin connection for ground side of current-sense resistor.

**CSOUT.** Amplifier output voltage proportional to current sensed across an external low-value resistor placed in the ground-side of the power FET bridge.

**CSP.** Input for current-sense differential amplifier, non-inverting, positive side. Connected to positive side of sense resistor.

**ENABLE.** Logic “0” disables the gate control signals and switches off all the gate drivers “low” causing a “coast”. Can be used in conjunction with the gate inputs to PWM the load current. Internally pulled down when terminal is open.

**FAULT.** Diagnostic logic output signal, when “low” indicates that one or more fault condition have occurred.

**GHA/GHB/GHC.** High-side gate-drive outputs for n-channel MOSFET drivers. External series gate resistors can control slew rate seen at the power driver gate; thereby, controlling the di/dt and dv/dt of Sx outputs.

**GLA/GLB/GLC.** Low-side gate drive outputs for external, n-channel MOSFET drivers. External series gate resistors can control slew rate.

**GND.** Ground or negative side of VDD and VBAT supplies.

**LSS.** Low-side gate driver returns. Connects to the common sources in the low-side of the power MOSFET bridge.

**OVFLT.** Logic “1” means that the VBAT exceeded the VBAT overvoltage trip point set by OVSET level. It will recover after a hysteresis below that maximum value. Normally has a high-impedance state.

**OVSET.** A positive, dc level that controls the VBAT overvoltage trip point. Usually, provided from precision resistor divider network between  $V_{DD}$  and GND, but can be held grounded for a preset value. When terminal is open, sets unspecified but high overvoltage trip point.

**SA/SB/SC.** Directly connected to the motor terminals, these terminals sense the voltages switched across the load and are connected to the negative side of the bootstrap capacitors. Also, are the negative supply connection for the floating, high-side drivers.

**UVFLT.** Logic “1” means that VBAT is below its minimum value and will recover after a hysteresis above that minimum value. Has a high-impedance state. [If UVFLT and OVFLT are both in high-impedance state; then, at least, a thermal shutdown or VDD undervoltage has occurred.]

**VBAT.** Battery voltage, positive input and is usually connected to the motor voltage supply.

**VBOOST.** Boost converter output, nominally 16 V, is also input to regulator for VREG. Has internal boost current and boost voltage control loops. In high-voltage systems is approximately one diode drop below  $V_{BAT}$ .

**VDD.** Logic supply, nominally +5 V.

**VDRAIN.** Kelvin connection for drain-to-source voltage monitor and is connected to high-side drains of MOSFET bridge. High impedance when terminal is open and registers as a short-to-ground fault on all motor phases.

**VDSTH.** A positive, dc level that sets the drain-to-source monitor threshold voltage. Internally pulled down when terminal is open.

**VREG.** High-side, gate-driver supply, nominally, 13.5 V. Has low-voltage dropout (LDO) feature.

## Functional Description

**Motor Lead Protection.** A fault detection circuit monitors the voltage across the drain to source of the external MOSFETs. A fault is asserted “low” on the output terminal,  $\overline{\text{FAULT}}$ , if the drain-to-source voltage of any MOSFET that is instructed to turn on is greater than the voltage applied to the  $V_{\text{DSTH}}$  input terminal. When a high-side switch is turned on, the voltage from  $V_{\text{DRAIN}}$  to the appropriate motor phase output,  $V_{\text{SX}}$ , is examined. If the motor lead is shorted to ground before the high side is turned on, the measured voltage will exceed the threshold and the  $\overline{\text{FAULT}}$  terminal will go “low”. Similarly, when a low-side MOSFET is turned on, the differential voltage between the motor phase (drain) and the LSS terminal (source) is monitored.  $V_{\text{DSTH}}$  is set by a resistor divider to  $V_{\text{DD}}$ .

The  $V_{\text{DRAIN}}$  is intended to be a Kelvin connection for the high-side, drain-source monitor circuit. Voltage drops across the power bus are eliminated by connecting an isolated PCB trace from the  $V_{\text{DRAIN}}$  terminal to the drain of the MOSFET bridge. This allows improved accuracy in setting the  $V_{\text{DSTH}}$  threshold voltage. The low-side, drain-source monitor uses the LSS terminal, rather than  $V_{\text{DRAIN}}$ , in comparing against  $V_{\text{DSTH}}$ . The A3935 merely reports these motor faults.

**Fault Outputs.** Transient faults on any of the fault outputs are to be expected during switching and will not disable the gate drive outputs. External circuitry or controller logic must determine if the faults represent a hazardous condition.

**FAULT.** This terminal will go active “low” when any of the following conditions occur:

- $V_{\text{BAT}}$  overvoltage,
- $V_{\text{BAT}}$  undervoltage,
- $V_{\text{REG}}$  undervoltage,
- Motor lead short-to-ground,
- Motor lead short-to-supply (or battery),
- Bridge (or  $V_{\text{DRAIN}}$ ) open,
- $V_{\text{DD}}$  undervoltage, or
- Thermal shutdown.

**OVFLT.** Asserts “high” when a  $V_{\text{BAT}}$  overvoltage fault occurs and resets “low” after a recovery hysteresis. It has a high-impedance state when a thermal shutdown or  $V_{\text{DD}}$  undervoltage occurs. The voltage at the OVSET terminal,  $V_{\text{OVSET}}$ , controls the  $V_{\text{BAT}}$  overvoltage set point  $V_{\text{BAT(ov)}}$ , i.e.,

$$V_{\text{BAT(ov)}} = (K_{\text{BAT(ov)}} \times V_{\text{SET(ov)}}) + V_{\text{BAT(ov)}(0)},$$

where  $K_{\text{BAT(ov)}}$  is the gain (12) and  $V_{\text{BAT(ov)}(0)}$  is the value of  $V_{\text{BAT(ov)}}$  when  $V_{\text{SET(ov)}}$  is zero (~22.4). For valid formula, all variables must be in range and below maximum operating specification.

**UVFLT.** Asserts “high” when a  $V_{\text{BAT}}$  undervoltage fault occurs and resets “low” after a recovery hysteresis. It has a high-impedance state when a thermal shutdown or  $V_{\text{DD}}$  undervoltage occurs. OVFLT and UVFLT are mutually exclusive by definition.

**Current Sensing.** A current-sense amplifier is provided to allow system monitoring of the load current. The differential amplifier inputs are intended to be Kelvin connected across a low-value sense resistor or current shunt. The output voltage is represented by:

$$V_{\text{CSOUT}} = (I_{\text{LOAD}} \times A_V \times R_S) + V_{\text{OS}}$$

where  $V_{\text{OS}}$  is the output voltage calibrated at zero load current and  $A_V$  is the differential amplifier gain of about 19.2.

**Shutdown.** If a fault occurs because of excessive junction temperature or undervoltage on  $V_{\text{DD}}$  or  $V_{\text{BAT}}$ , all gate driver outputs are driven “low” until the fault condition is removed. In addition, the boost supply switch and the VREG are turned “off” until those undervoltages and junction temperatures recover.

**Boost Supply.**  $V_{\text{BOOST}}$  is controlled by an inner current-control loop, and by an outer voltage-feedback loop. The current-control loop turns “off” the boost switch for 5  $\mu\text{s}$  whenever the voltage across the boost current-sense resistor exceeds 500 mV. A diode reverse-recovery current flows through the sense resistor whenever the boost switch turns “on”, which could turn it “off” again if not for the “blanking time” circuit. Adjustment of this external sense resistor determines the maximum current in the inductor. Whenever  $V_{\text{BOOST}}$  exceeds the predefined threshold, nominally 16 V, the boost switch is inhibited.

### Functional Description (cont'd)

#### Input Logic

ENABLE	xLO	xHI	GLx	GHx	Mode of Operation
0	X	X	0	0	All gate drive outputs low
1	0	0	0	0	Both gate drive outputs low
1	0	1	0	1	High side on
1	1	0	1	0	Low side on
1	1	1	0	0	XOR circuitry prevents shoot-through

#### Fault Responses

Fault Mode	ENABLE Input	FAULT	OVFLT	UVFLT	Boost Reg.	V <sub>REG</sub> Reg.	GHx	GLx
No Fault	X	1	0	0	ON	ON	①	①
Short-to-Battery	1②	0	0	0	ON	ON	①	①
Short-to-Ground	1③	0	0	0	ON	ON	①	①
Bridge (V <sub>DRAIN</sub> ) Fault	1④	0	0	0	ON	ON	①	①
V <sub>REG</sub> Undervoltage	X	0	0	0	ON	ON	①	①
V <sub>BAT</sub> Overvoltage	X	0	1	0	OFF⑤	ON	①	①
V <sub>BAT</sub> Undervoltage⑥	X	0	0	1	OFF	OFF	0	0
V <sub>DD</sub> Undervoltage⑥	X	0	Z	Z	OFF	OFF	0	0
Thermal Shutdown⑥	X	0	Z	Z	OFF	OFF	0	0

NOTES: x = "Little x "indicates A, B, or C phase.

X = "Capital X " indicates a "don't care".

Z = High-impedance state.

① = Depends on xLO input, xHI input, and ENABLE. See Input Logic table.

② = Short-to-battery can only be detected when the corresponding GLx = 1. This fault is not detected when ENABLE = 0.

③ = Short-to-ground can only be detected when the corresponding GHx = 1. This fault is not detected when ENABLE = 0.

④ = Bridge fault appears as a short-to-ground fault on all motor phases. This fault is not detected when ENABLE = 0.

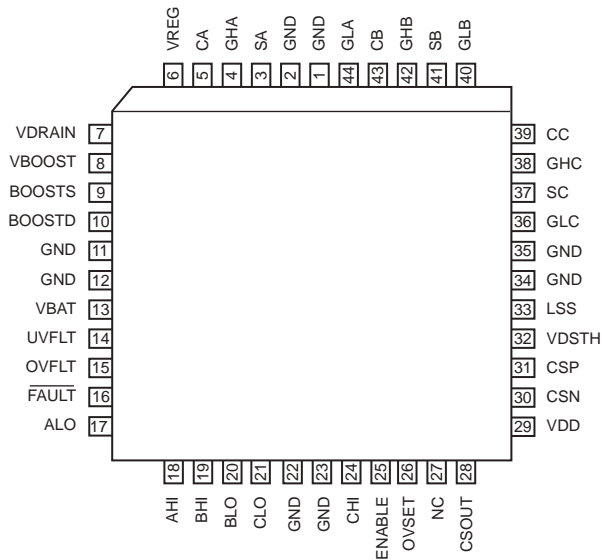
⑤ = Off, only because V<sub>BOOST</sub> ≈ V<sub>BAT</sub> is above the voltage threshold of the regulator's voltage control loop.

⑥ = These faults are not only reported but action is taken by the internal logic to protect the A3935 and the system.

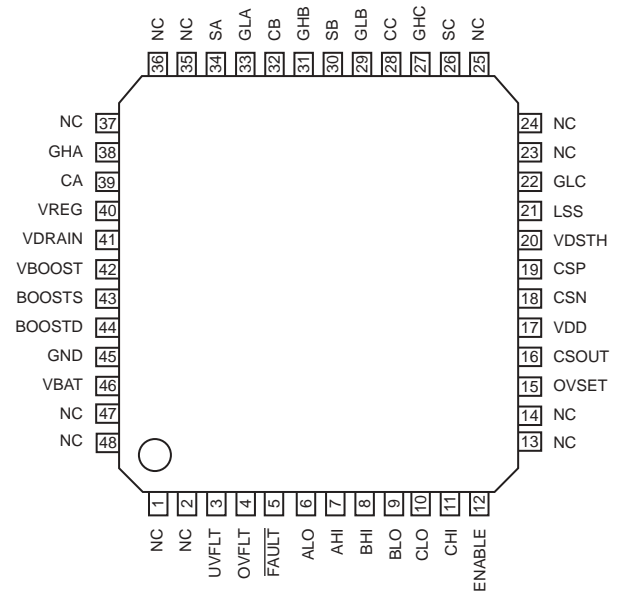
# 3935

## THREE-PHASE POWER MOSFET CONTROLLER

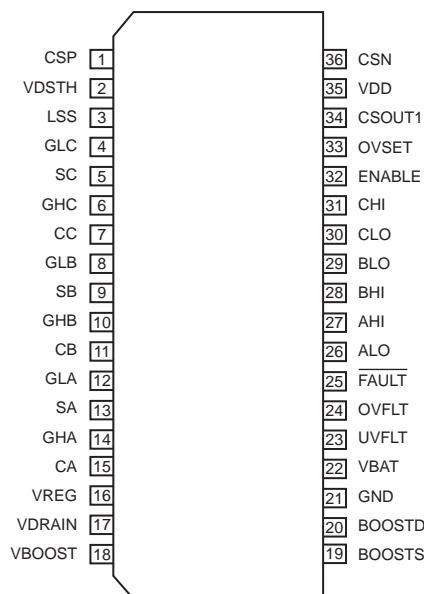
Package ED, 44-Pin PLCC



Package JP, 48-Pin LQFP

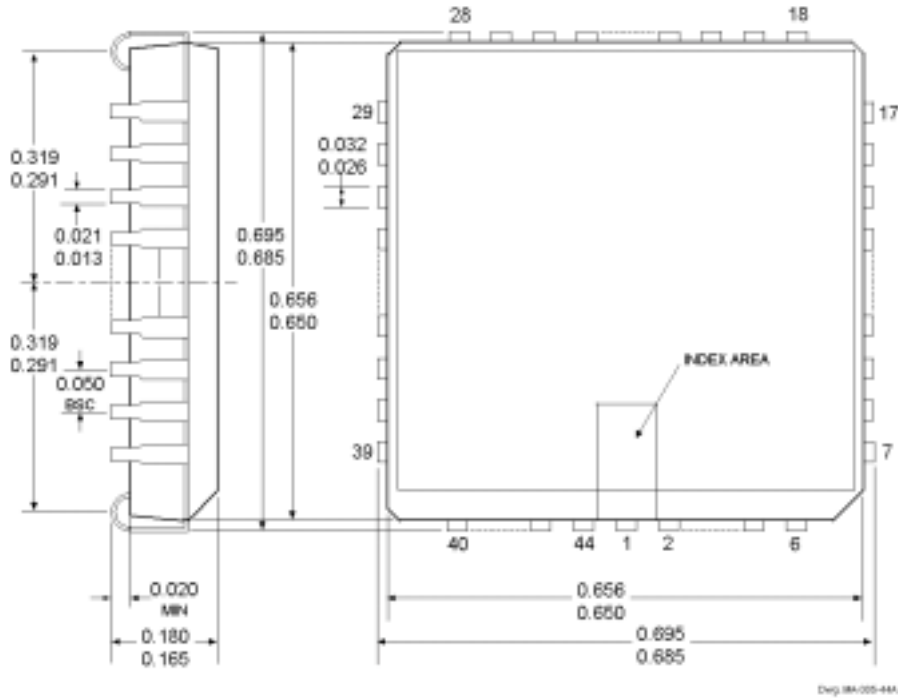


Package LQ, 36-Pin SOIC

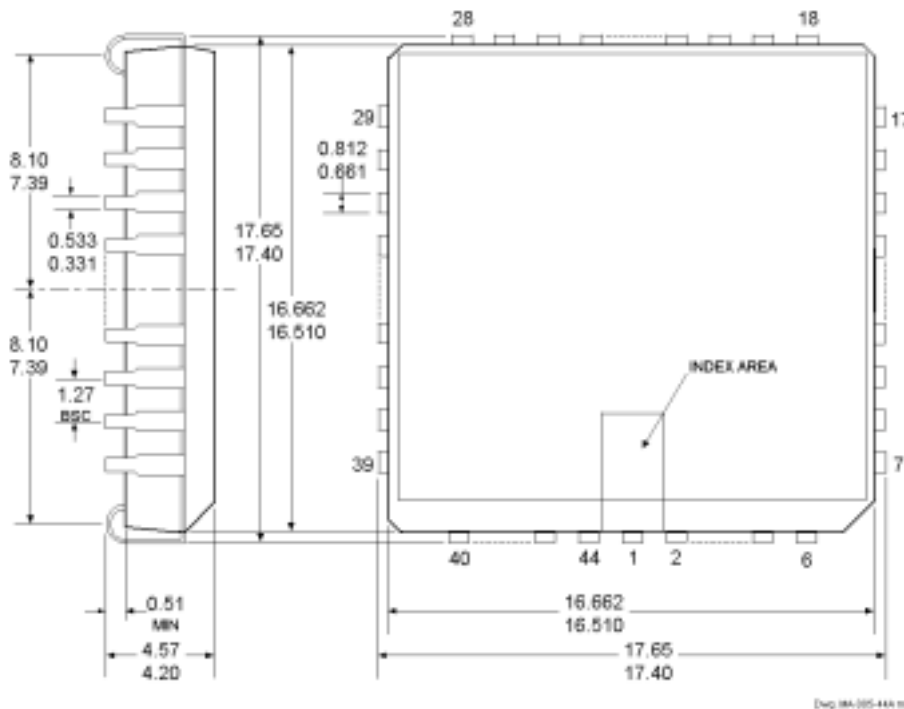


# 3935 THREE-PHASE POWER MOSFET CONTROLLER

## A3935KED (PLCC)



**Dimensions in Inches**  
(for reference only)

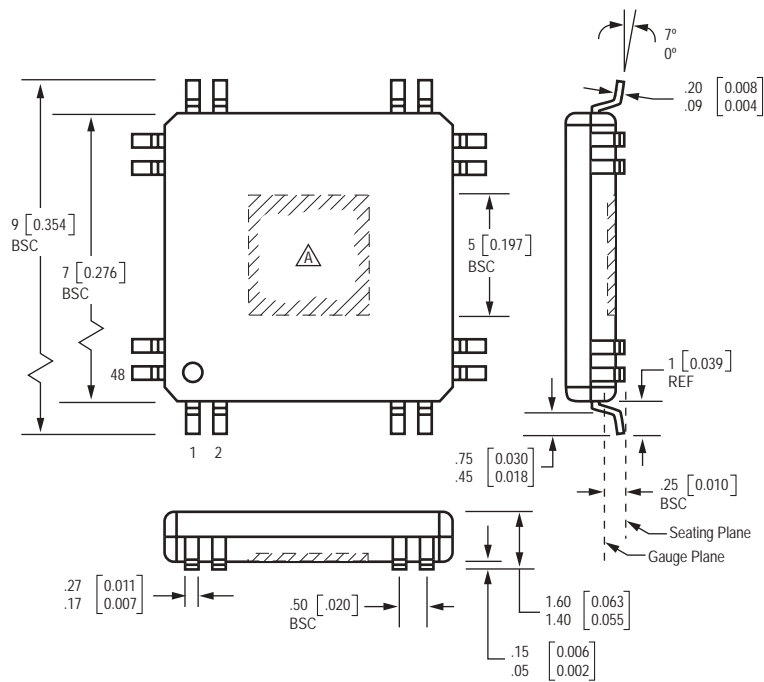


**Dimensions in Millimeters**  
(controlling dimensions)

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.  
 2. Lead spacing tolerance is non-cumulative.  
 3. Webbed lead frame. Terminals 1, 2, 11, 12, 22, 23, 34, and 35 are internally one piece.  
 4. Supplied in standard sticks/tubes of 27 devices or add "TR" to part number for tape and reel.

# 3935 THREE-PHASE POWER MOSFET CONTROLLER

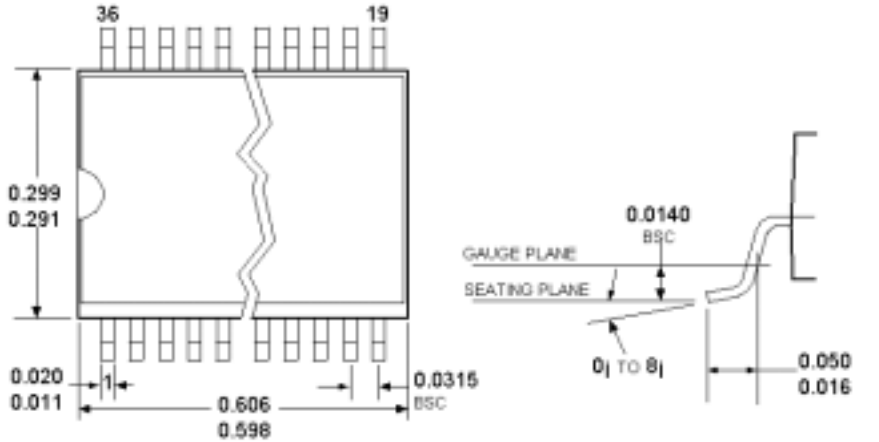
## A3935KJP (LQFP)



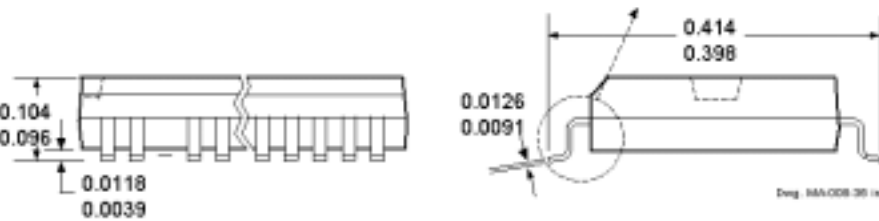
Dimensions in millimeters  
 U.S. Customary dimensions (in.) in brackets, for reference only  
 ⚠ Exposed thermal pad (bottom surface)

# 3935 THREE-PHASE POWER MOSFET CONTROLLER

## A3935KLQ (SOIC)



**Dimensions in Inches**  
(for reference only)



**Dimensions in Millimeters**  
(controlling dimensions)

- NOTES: 1. Lead spacing tolerance is non-cumulative.  
 2. Exact body and lead configuration at vendor's option within limits shown.  
 3. Supplied in standard sticks/tubes of 31 devices or add "TR" to part number for tape and reel.

**3935**

***THREE-PHASE POWER  
MOSFET CONTROLLER***

*The products described here are manufactured under one or more U.S. patents or U.S. patents pending.*

*Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.*

*Allegro products are not authorized for use as critical components in life-support devices or systems without express written approval.*

*The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.*