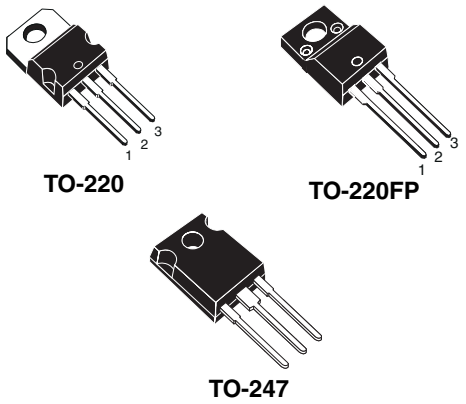
STP10NK80ZFP
STP10NK80Z - STW10NK80Z

N-channel 800V - 0.78Ω - 9A - TO-220/FP-TO-247
Zener-protected superMESH™ MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP10NK80Z	800V	<0.90Ω	9A	160 W
STW10NK80Z	800V	<0.90Ω	9A	160 w
STP10NK80ZFP	800V	<0.90Ω	9A	40 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeability



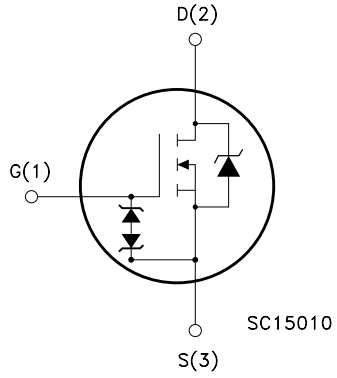
Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STP10NK80Z	P10NK80Z	TO-220	Tube
STP10NK80ZFP	P10NK80ZFP	TO-220FP	Tube
STW10NK80Z	W10NK80Z	TO-247	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/ TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	800		V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	800		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	9	9(1)	A
I_D	Drain current (continuous) at T_C=100°C	6	6(1)	A
I_{DM}(2)	Drain current (pulsed)	36	36(1)	A
P_{TOT}	Total dissipation at T_C = 25°C	160	40	W
	Derating Factor	1.28	0.32	W/°C
Vesd(G-S)	G-S ESD (HBM C=100pF, R=1.5kΩ)	4		KV
dv/dt(3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (DC)	--	2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤9A, di/dt ≤200A/µs,V_{DD} ≤$V_{(BR)DSS}$, T_j ≤T_{JMAX}

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-220FP	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	0.78	3.1	0.78	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	62.5		50	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	9	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	290	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±10	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 100µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 4.5A		0.78	0.9	Ω

Table 5. Dynamic

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 4.5A		9.6		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		2180 205 38		pF pF pF
$C_{oss\ eq}$ (2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 640V		105		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=640V, I_D = 9A V_{GS} =10V (see Figure 19)		72 12.5 37		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}=400 V, I_D=4.5A, R_G=4.7Ω, V_{GS}=10V (see Figure 20)		30 20		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=400 V, I_D=4.5A, R_G=4.7Ω, V_{GS}=10V (see Figure 20)		65 17		ns ns

Table 7. Gate-source zener diode

Symbol	Parameter	Test condictions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-Source Breakdown Voltage	Igs=±1mA (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Table 8. Source drain diode

Symbol	Parameter	Test condictions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				9	A
I_{SDM}(1)	Source-drain current (pulsed)				36	A
V_{SD}(2)	Forward on voltage	I_{SD}=9A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=9A, di/dt = 100A/µs, V_{DD}=45V, Tj=150°C		645 6.4 20		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

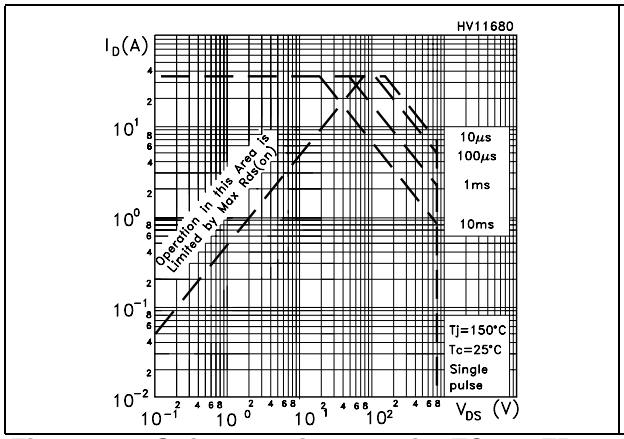


Figure 2. Thermal impedance for TO-220

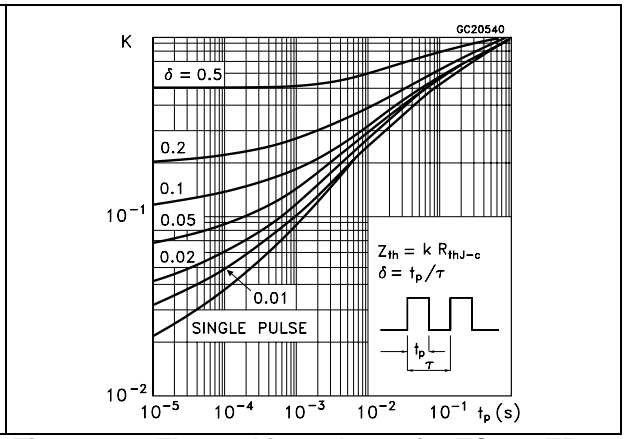


Figure 3. Safe operating area for TO-220FP

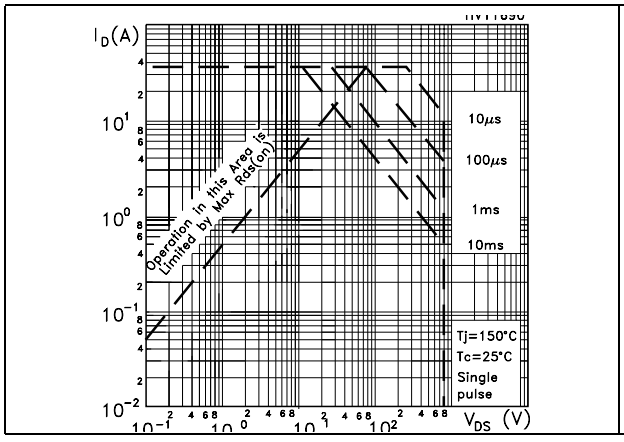


Figure 4. Thermal impedance for TO-220FP

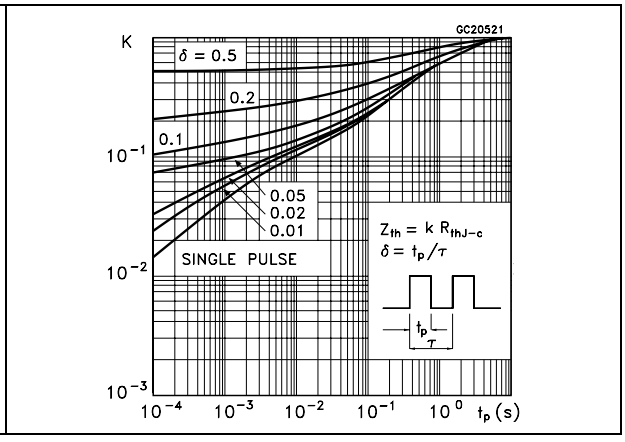


Figure 5. Safe operating area for TO-247

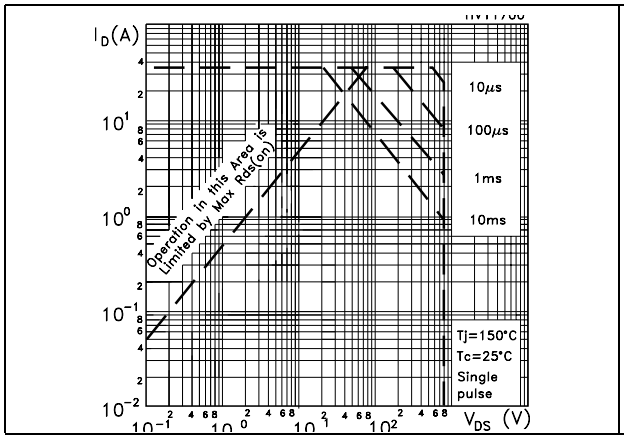


Figure 6. Thermal impedance for TO-247

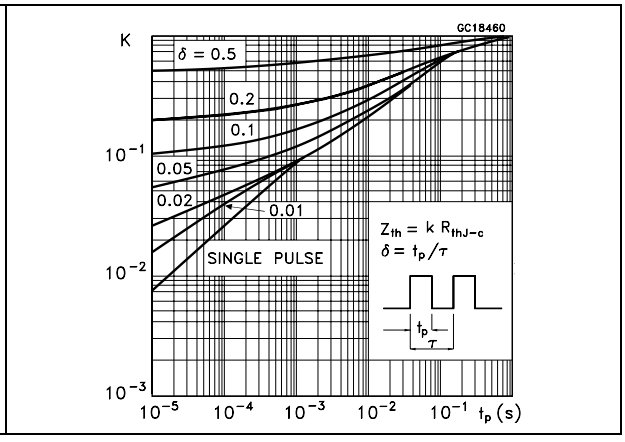


Figure 7. Output characterisics

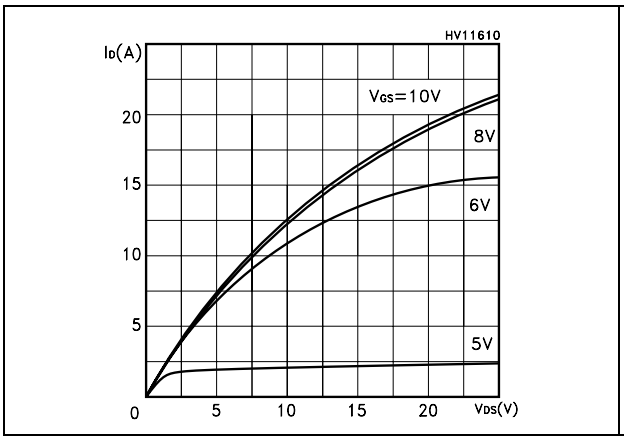


Figure 8. Transfer characteristics

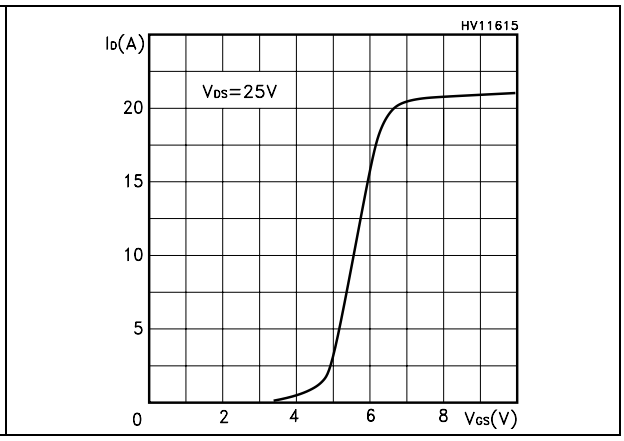


Figure 9. Transconductance

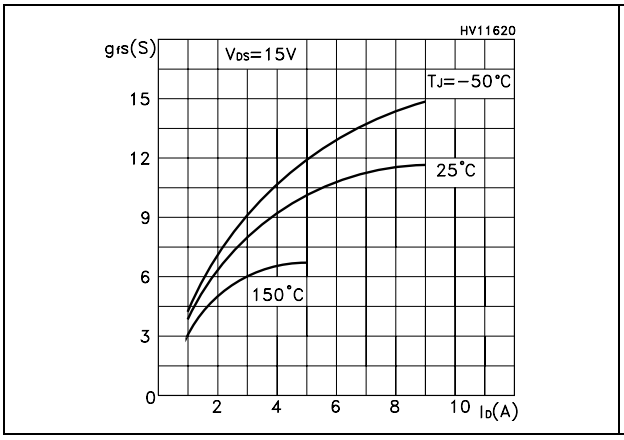


Figure 10. Static drain-source on resistance

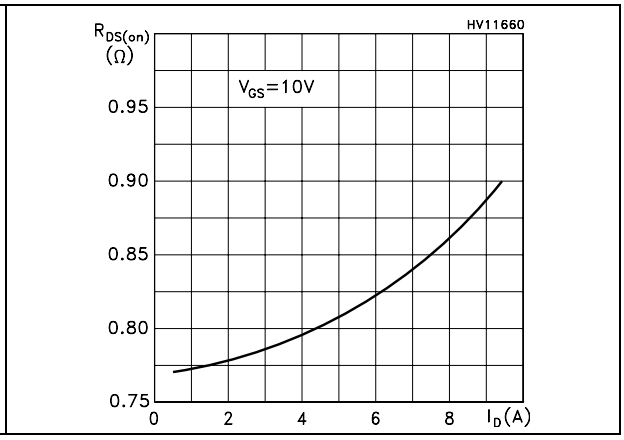


Figure 11. Gate charge vs gate-source voltage

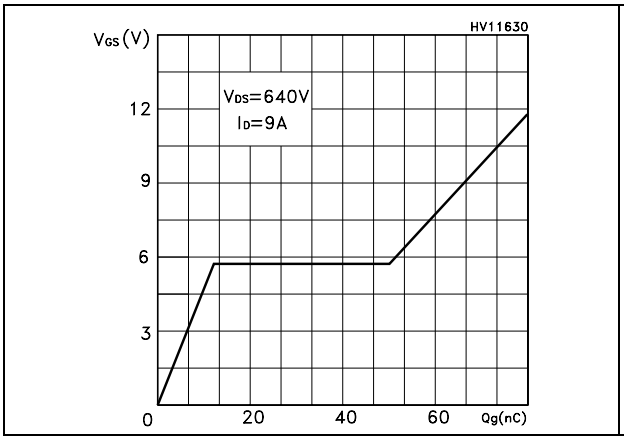


Figure 12. Capacitance variations

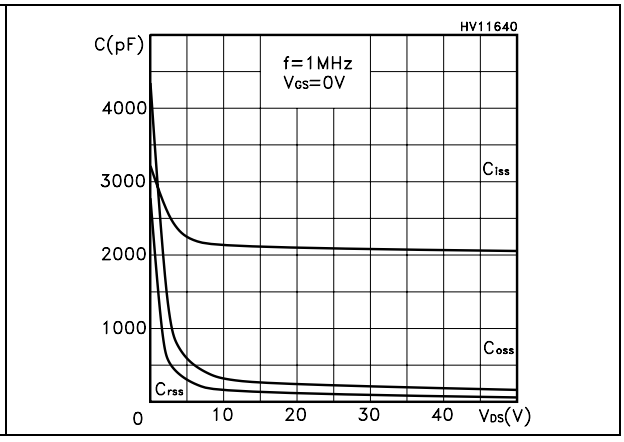


Figure 13. Normalized gate threshold voltage vs temperature

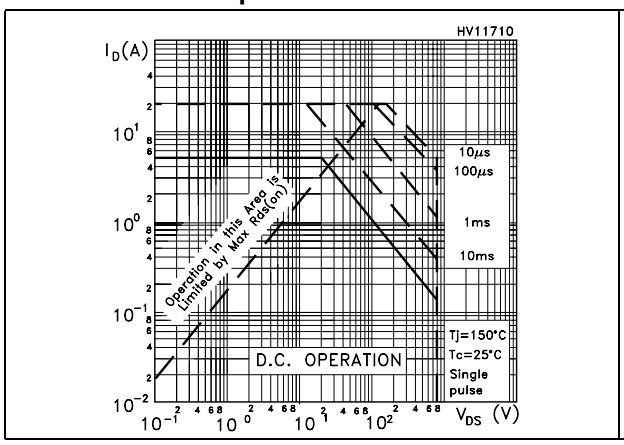


Figure 14. Normalized on resistance vs temperature

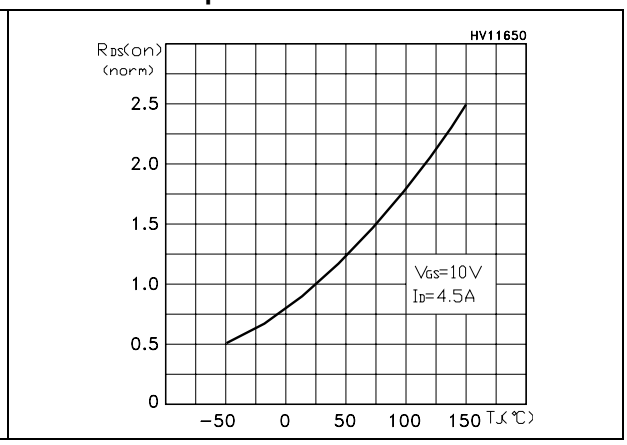


Figure 15. Source-drain diode forward characteristics

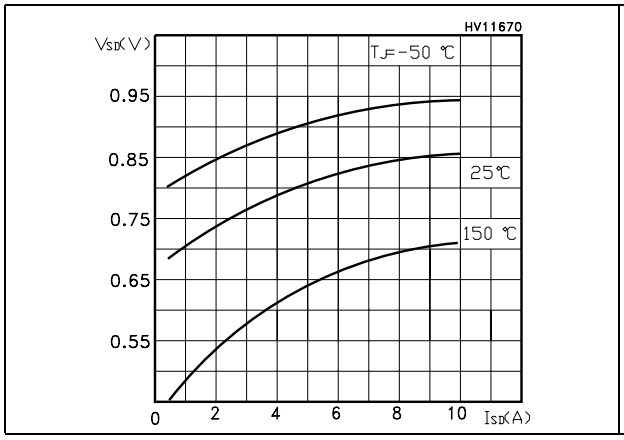


Figure 16. Normalized B_{VDSS} vs temperature

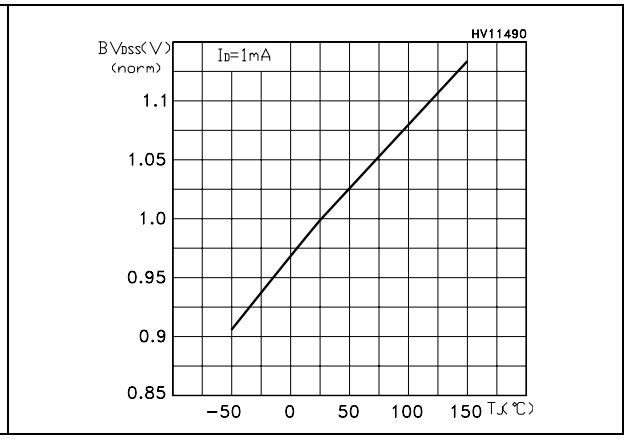
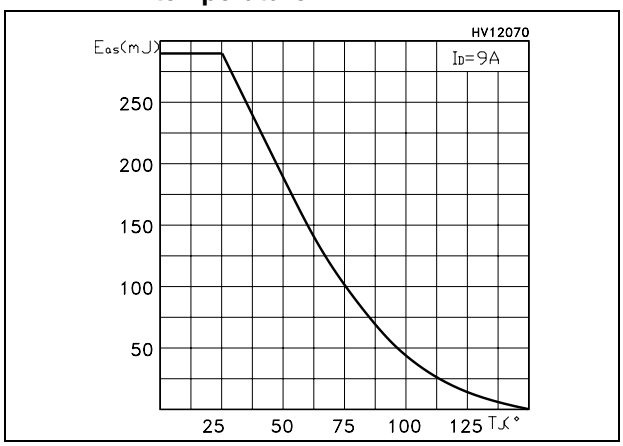


Figure 17. Maximum avalanche energy vs temperature



3 Test circuit

Figure 18. Switching times test circuit for resistive load

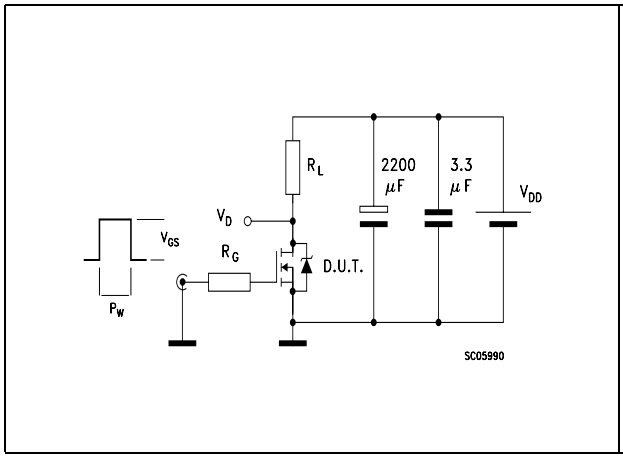


Figure 19. Gate charge test circuit

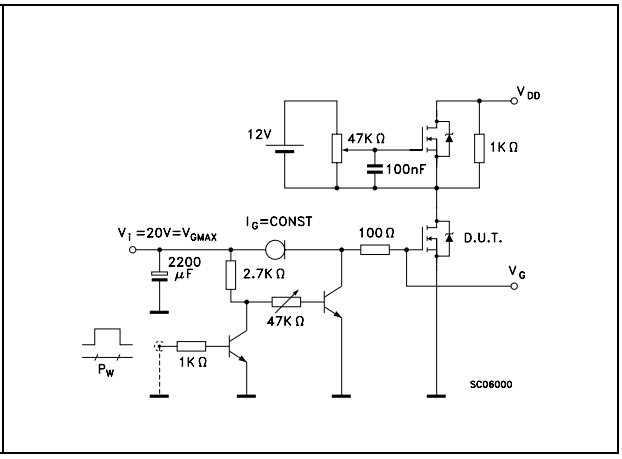


Figure 20. Test circuit for inductive load switching and diode recovery times

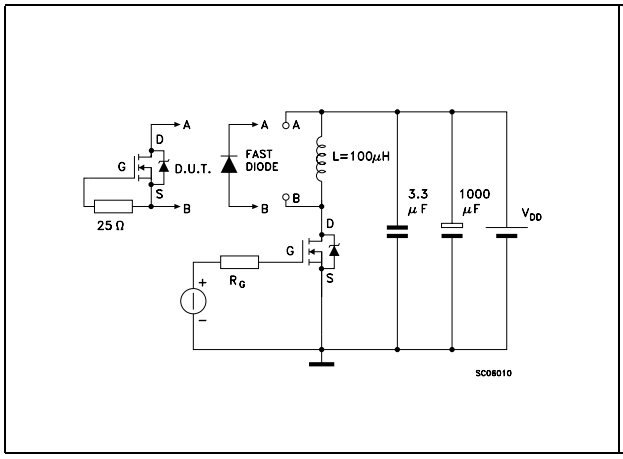


Figure 21. Unclamped Inductive load test circuit

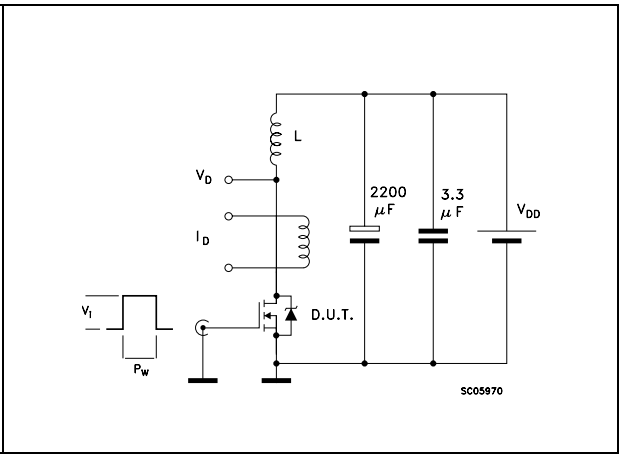


Figure 22. Unclamped inductive waveform

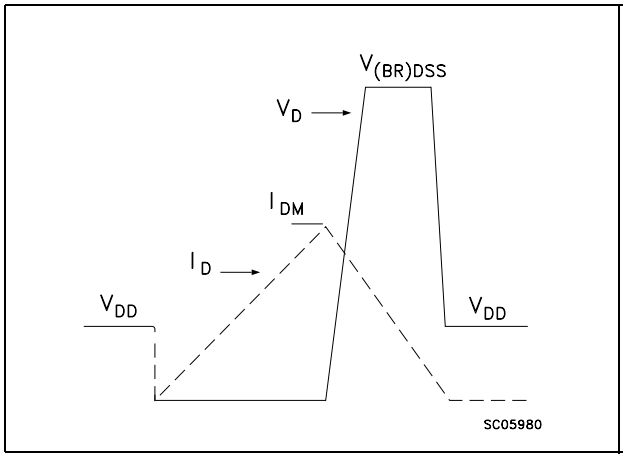
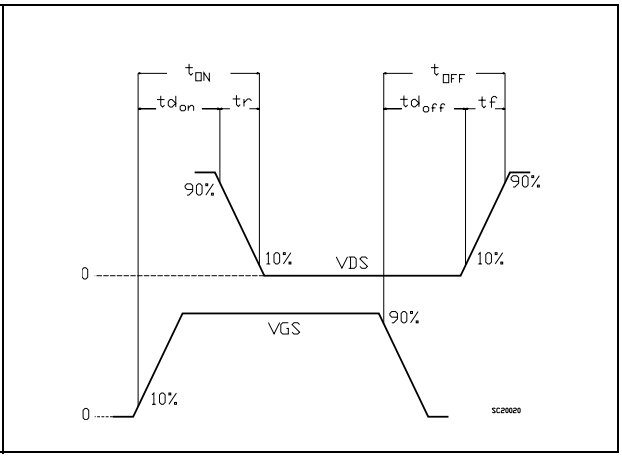


Figure 23. Switching time waveform

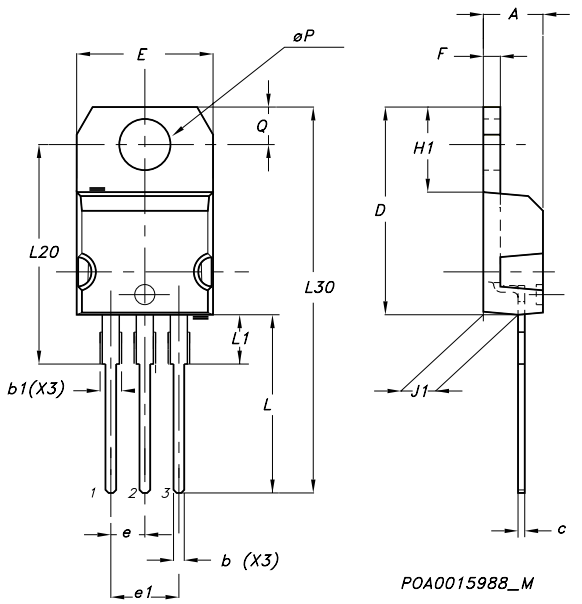


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

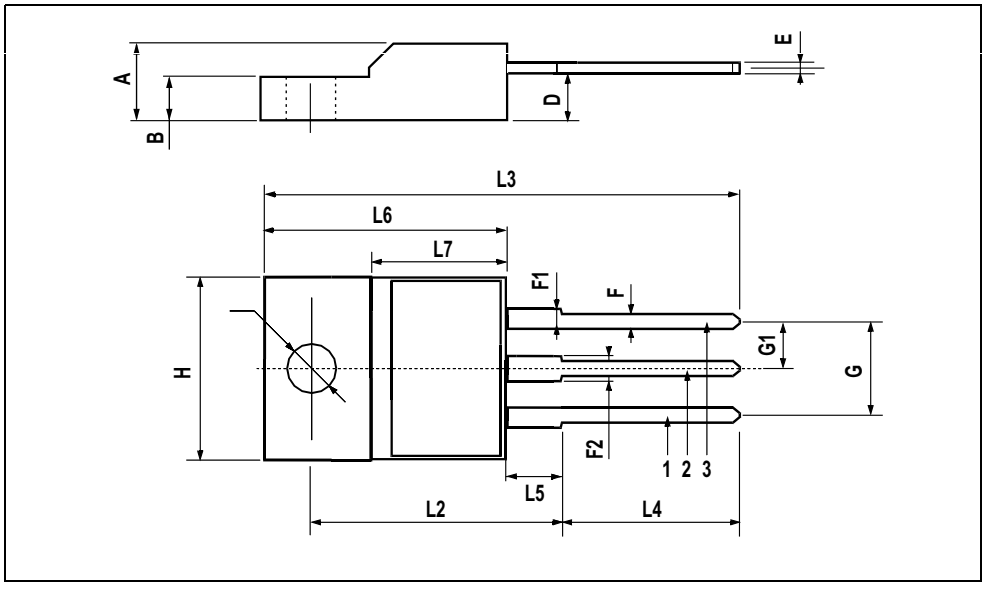
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



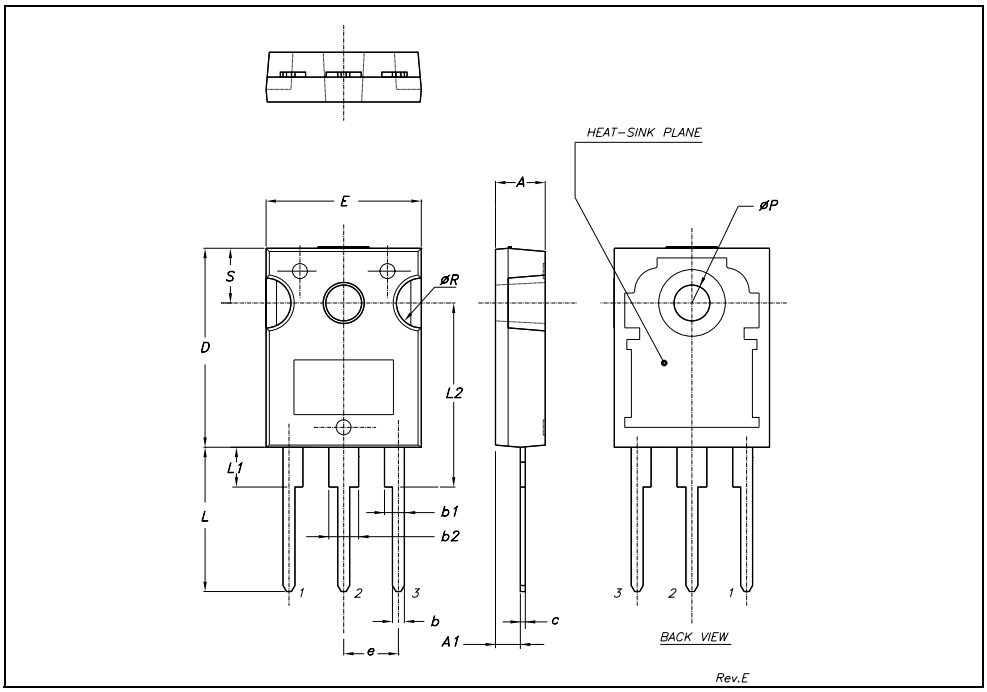
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
08-Sep-2005	4	Complete document
10-Mar-2006	5	Inserted ecopack indication
28-Sep-2005	6	New template, no content change

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