



BU931Z

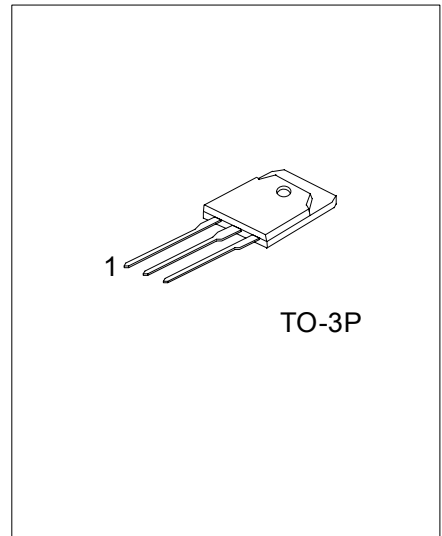
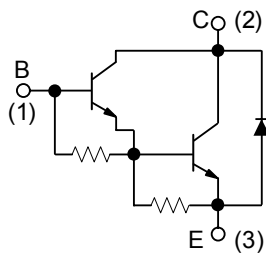
NPN SILICON TRANSISTOR

NPN POWER DARLINGTON

■ FEATURES

- * High operating junction temperature
- * High voltage ignition coil driver
- * Very rugged bipolar technology

■ INTERNAL SCHEMATIC DIAGRAM



*Pb-free plating product number: BU931L

■ ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | Packing |
|-----------------|-------------------|---------|----------------|---|---|---------|
| Normal | Lead Free Plating | | 1 | 2 | 3 | |
| BU931-T3P-T | BU931L-T3P-T | TO-3P | B | C | E | Tube |

| | |
|--|--|
| <p>BU931L-T3P-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Plating</p> | <p>(1) T: Tube</p> <p>(2) T3P: TO-3P</p> <p>(3) L: Lead Free Plating, Blank: Pb/Sn</p> |
|--|--|

■ ABSOLUTE MAXIMUM RATINGS (Ta=25)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|------------------------------|------------|------------|------|
| Collector-Emitter Voltage | BV_{CEO} | 350 | V |
| Emitter-Base Voltage | BV_{EBO} | 5 | V |
| Collector Current (DC) | I_C | 10 | A |
| Collector Peak Current | I_{CM} | 15 | A |
| Base Current | I_B | 1 | A |
| Base Peak Current | I_{BM} | 5 | A |
| Total Dissipation (Tc = 25) | P_D | 125 | W |
| Junction Temperature | T_J | +175 | |
| Storage Temperature | T_{STG} | -65 ~ +175 | |

■ ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------------|---|-----|-----|-----|---------------|
| Collector Cut-off Current | I_{CEO} | $V_{CE} = 300\text{ V}$ | | | 100 | μA |
| Emitter Cut-off Current | I_{EBO} | $V_{EB} = 5\text{ V}$ | | | 20 | mA |
| | V_{CL} | $I_C = 100\text{mA}$ | 350 | | 500 | V |
| Collector-Emitter Saturation Voltage | $V_{CE(SAT)1}$ | $I_C = 7\text{ A}, I_B = 70\text{ mA}$ | | | 1.6 | V |
| | $V_{CE(SAT)2}$ | $I_C = 8\text{ A}, I_B = 100\text{ mA}$ | | | 1.8 | V |
| Base-Emitter Saturation Voltage | $V_{BE(SAT)1}$ | $I_C = 7\text{ A}, I_B = 70\text{ mA}$ | | | 2.2 | V |
| | $V_{BE(SAT)2}$ | $I_C = 8\text{ A}, I_B = 100\text{ mA}$ | | | 2.4 | V |
| DC Current Gain | h_{FE} | $V_{CE} = 10\text{ V}, I_C = 5\text{ A}$ | 300 | | | |
| Diode Forward Voltage | V_F | $I_F = 8\text{ A}$ | | | 2.5 | V |
| Inductive Load Storage Time / Fall Time | t_s | $V_{CC} = 12\text{ V}, V_{clamp} = 300\text{ V}$ $L = 7\text{ mH}$ | | 15 | | μs |
| | t_f | $I_C = 7\text{ A}, I_B = 70\text{ mA}$ $V_{BE} = 0, R_{BE} = 47\Omega$ | | 0.5 | | μs |

Note: 1. Wafer area should be than 50%

2.The quantity of cracked wafers should be less than 10% per shipment.

3.Average yield should be more than 50% per wafer, 80% per shipment.

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