3 CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT

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GENERAL DESCRIPTION

The XRT73L03 is a 3-Channel, E3/DS3/STS-1 Line Interface Unit designed for E3, DS3 or SONET STS-1 applications and consists of three independent line transmitters and receivers integrated on a single chip.

Each channel of the XRT73L03 can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channels.

In the transmit direction, each channel in the XRT73L03 encodes input data to either B3ZS or HDB3 format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT73L03 can perform Equalization on incoming signals, perform Clock Recovery, decode data from either B3ZS or HDB3 format, convert the receive data into TTL/CMOS format, check for LOS or LOL conditions and detect and declare the occurrence of Line Code Violations.

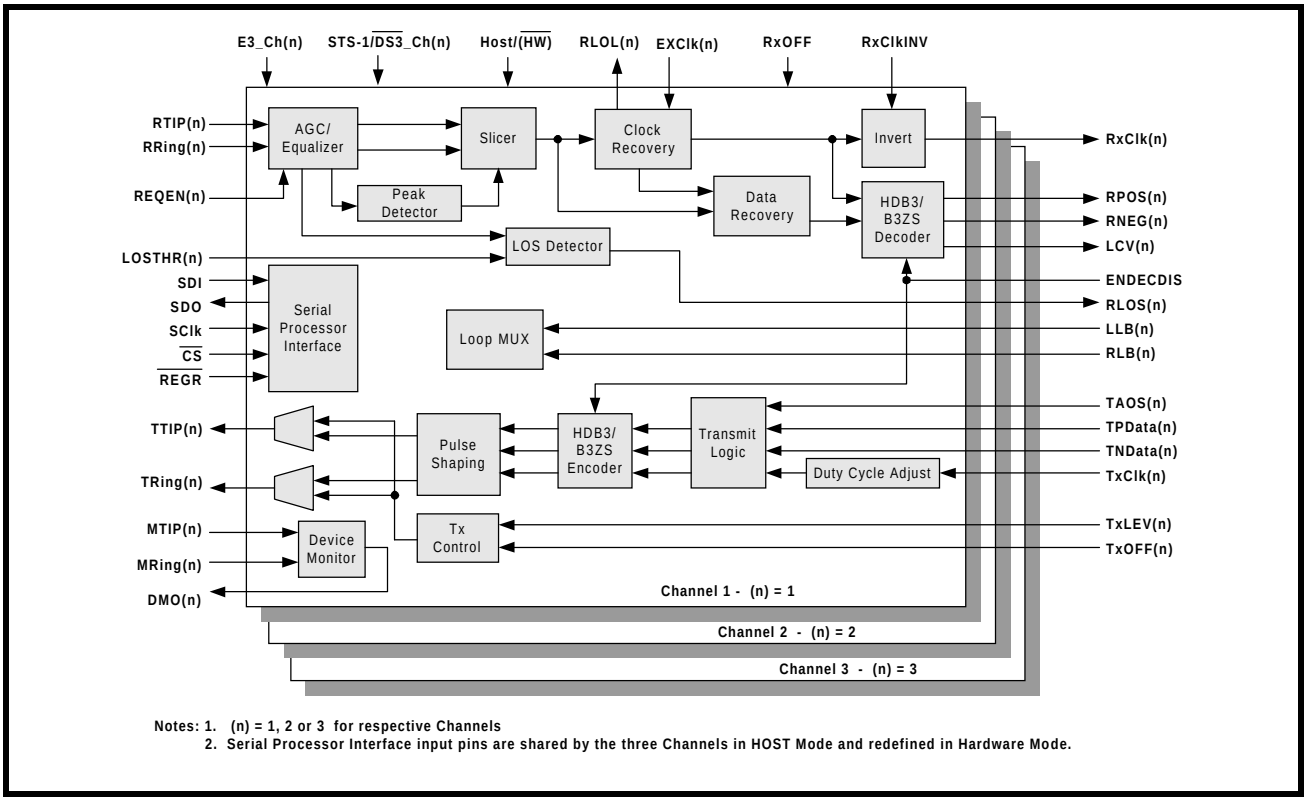
APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

FEATURES

- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Full Loop-Back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Contains a 4-Wire Microprocessor Serial Interface
- Uses Minimum External components
- Single +3.3V Power Supply
- 5V tolerant I/O
- -40°C to +85°C Operating Temperature Range
- Available in a Thermally Enhanced 120 pin TQFP package

FIGURE 1. XRT73L03 BLOCK DIAGRAM



Notes: 1. (n) = 1, 2 or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the three Channels in HOST Mode and redefined in Hardware Mode.

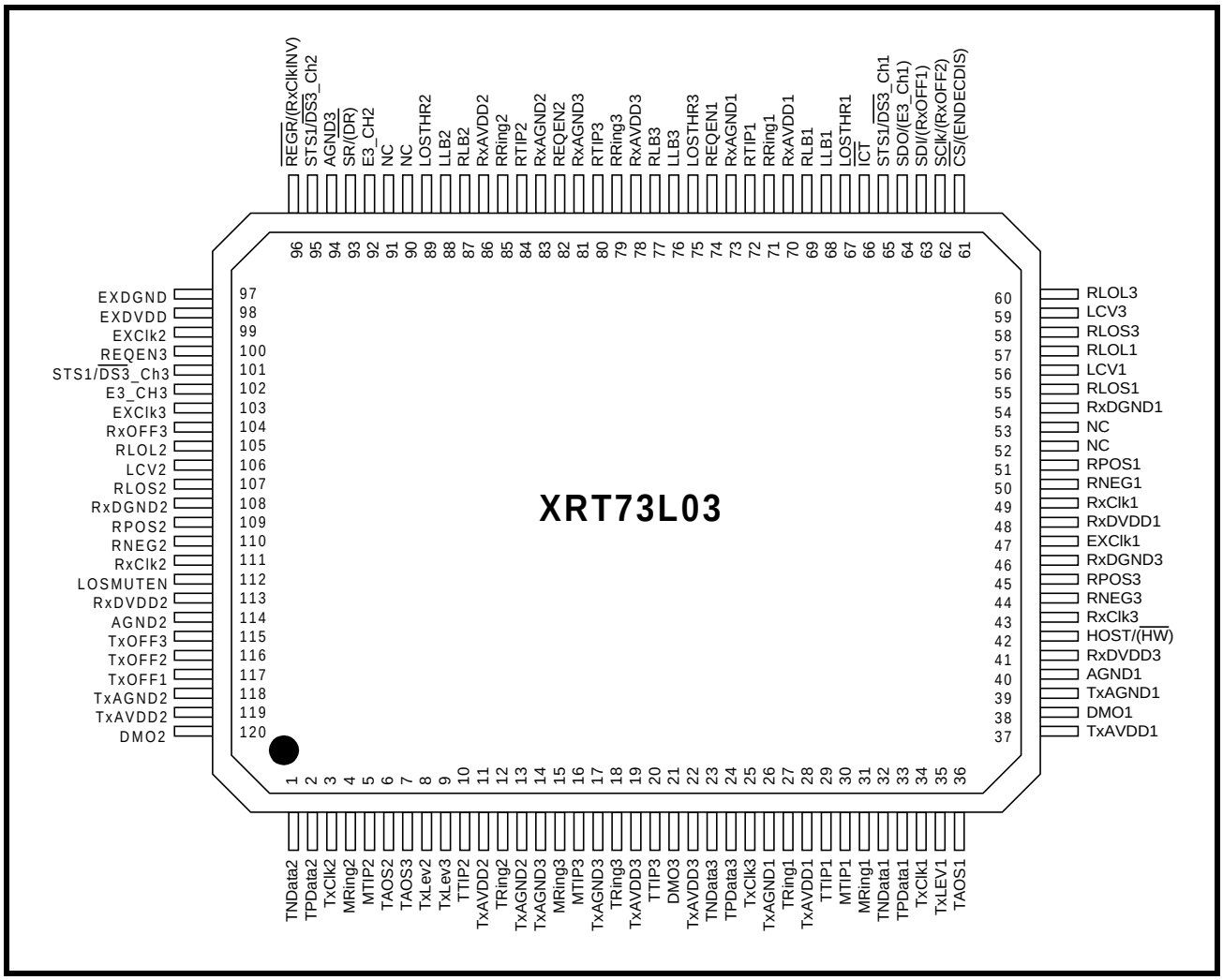
TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal from the line
- Integrated Pulse Shaping Circuit.
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Contains Transmit Clock Duty Cycle Correction Circuit on-chip
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) and Timing Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment
- Receiver can be powered down in order to conserve power in redundancy designs

FIGURE 2. PIN OUT OF THE XRT73L03 IN THE 14 X 20MM, 0.5MM PITCH TQFP



ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73L03IV	120 Pin TQFP 14mm X 20mm	-40^{o}C to +85^{o}C

PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
1	TNData2	I	**Transmit Negative Data Input - Channel 2:** Refer to the description of pin 32 TNData1
2	TPData2	I	**Transmit Positive Data Input - Channel 2:** Refer to the description of pin 33 TPData1
3	TxClk2	I	**Transmit Clock Input for TPData and TNData - Channel 2:** Refer to the description of pin 34 TxClk1
4	MRing2	I	**Monitor Ring Input - Channel 2:** Refer to the description of pin 31 MRing1
5	MTIP2	I	**Monitor Tip Input - Channel 2:** Refer to the description of pin 30 MTIP1
6	TAOS2	I	**Transmit All Ones Select - Channel 2:** Refer to description of pin 36 TAOS1
7	TAOS3	I	**Transmit All Ones Select - Channel 3:** Refer to description of pin 36 TAOS1
8	TxLEV2	I	**Transmit Line Build-Out Enable/Disable Select - Channel 2:** Refer to the description of 35 TxLEV1
9	TxLEV3	I	**Transmit Line Build-Out Enable/Disable Select - Channel 3:** Refer to the description of 35 TxLEV1
10	TTIP2	O	**Transmit TTIP Output - Channel 2:** Refer to the description of pin 29 TTIP1
11	TxAVDD2	****	**Transmitter Analog 3.3V+ 5% VDD - Transmitter 2**
12	TRing2	O	**Transmit Ring Output - Channel 2:** Refer to the description of pin 27 TRing1
13	TxAGND2	****	**Transmitter Analog GND - Transmitter 2**
14	TxAGND3	****	**Transmitter Analog GND - Channel 3**
15	MRing3	I	**Monitor Ring Input - Channel 3:** Refer to the description of pin 31 MRing1
16	MTIP3	I	**Monitor Tip Input - Channel 3:** Refer to the description of pin 30 MTIP1
17	TxAGND3	****	**Transmitter Analog GND - Transmitter 3**
18	TRing3	O	**Transmit Ring Output - Channel 3:** Refer to the description of pin 27 TRing1
19	TxAVDD3	****	**Transmitter Analog 3.3V+ 5% VDD - Transmitter 3**
20	TTIP3	O	**Transmit TTIP Output - Channel 3:** Refer to the description of pin 29 TTIP1
21	DMO3	O	**Drive Monitor Output - Channel 3:** Refer to the description of pin 38 DMO1

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
22	TxAVDD3	****	**Transmitter Analog 3.3V+ 5% VDD - Transmitter 3**
23	TNData3	I	**Transmit Negative Data Input - Channel 3:** Refer to the description of pin 32 TnData1
24	TPData3	I	**Transmit Positive Data Input - Channel 3:** Refer to the description of pin 33 TPData1
25	TxClk3	I	**Transmit Clock Input for TPData and TNData - Channel 3:** Refer to the description of pin 34 TxClk1
26	TxAGND1	****	**Transmitter Analog GND - Transmitter 1:**
27	TRing1	O	**Transmit Ring Output - Channel 1:** The XRT73L03 uses this pin with TTIP1 to transmit a bipolar line signal via a 1:1 transformer.
28	TxAVDD1	****	**Transmitter Analog 3.3V+ 5% VDD - Transmitter 1:**
29	TTIP1	O	**Transmit TTIP Output - Channel 1:** The XRT73L03 uses this pin with TRing1 to transmit a bipolar line signal via a 1:1 transformer.
30	MTIP1	I	**Monitor Tip Input - Channel 1:** The bipolar line output signal from TTIP1 is connected to this pin via a 270-ohm resistor to check for line driver failure. This pin is internally pulled "High".
31	MRing1	I	**Monitor Ring Input - Channel 1:** The bipolar line output signal from TRing1 is connected to this pin via a 270-ohm resistor to check for line driver failure. This pin is internally pulled "High".
32	TNData1	I	**Transmit Negative Data Input - Channel 1:** The XRT73L03 samples this pin on the falling edge of TxClk1. If it samples a "1", then it generates and transmits a negative polarity pulse to the line. ***NOTES:*** *1. This input pin is ignored and tied to GND if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If operating in the HOST Mode, it can be configured to sample the TNData1 pin on either the rising or falling edge of TxClk1.*
33	TPData1	I	**Transmit Positive Data Input - Channel 1:** The XRT73L03 samples this pin on the falling edge of TxClk. If it samples a "1", then it generates and transmits a positive polarity pulse to the line. ***NOTES:*** *1. The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If the XRT73L03 is operating in the HOST Mode it can be configured to sample the TPData1 pin on either the rising or falling edge of TxClk1.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
34	TxClk1	I	**Transmit Clock Input for TPData and TNData - Channel 1:** This input pin must be driven at 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications or 51.84 MHz for SONET STS-1 applications. The XRT73L03 uses this signal to sample the TPData1 and TNData1 input pins. By default, the XRT73L03 is configured to sample these two pins on the falling edge of this signal. If operating in the HOST Mode, the XRT73L03 can be configured to sample the TPData1 and TNData1 input pins on either the rising or falling edge of TxClk1.
35	TxLEV1	I	**Transmit Line Build-Out Enable/Disable Select - Channel 1:** This input pin is used to enable or disable the Transmit Line Build-Out circuit of Channel 1. Setting this pin to "High" disables the Line Build-Out circuit of Channel 1. In this mode, Channel 1 outputs partially-shaped pulses onto the line via the TTIP1 and TRing1 output pins. Setting this pin to "Low" enables the Line Build-Out circuit of Channel 1. In this mode, Channel 1 outputs shaped pulses onto the line via the TTIP1 and TRing1 output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set this input pin to "1" if the cable length between the Cross-Connect and the transmit output of Channel 1 is greater than 225 feet. 2. Set this input pin to "0" if the cable length between the Cross-Connect and the transmit output of Channel 1 is less than 225 feet. This pin is active only if the following two conditions are true: a. The XRT73L03 is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT73L03 is configured to operate in the Hardware Mode. ***NOTE:*** *If the XRT73L03 is going to be operating in the HOST Mode, this pin should be tied to GND.*
36	TAOS1	I	**Transmit All Ones Select - Channel 1:** A “High" on this pin causes the Transmit Section of Channel 1 to generate and transmit a continuous AMI all “1’s" pattern onto the line. The frequency of this "1’s" pattern is determined by TxClk1. ***NOTES:*** 1. *This input pin is ignored if the XRT73L03 is operating in the HOST Mode.* 2. *if the XRT73L03 is going to be operating in the HOST Mode, this pin should tie tied to GND..*
37	TxAVDD1	****	**Transmitter Analog 3.3V+ 5% VDD - Transmitter 1**
38	DMO1	O	**Drive Monitor Output - Channel 1:** If no transmitted AMI signal is present on MTIP1 and MRing1 input pins for 128±32 TxClk periods, then DMO1 toggles and remains "High" until the next AMI signal is detected.
39	TxAGND1	****	**Transmitter Analog GND - Transmitter 1**
40	AGND1	****	**Analog GND (Substrate Connection) - Channel 1:**

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
41	RxDVDD3	****	**Receive Digital 3.3V+ 5% VDD (for Receiver 3):**
42	HOST/($\overline{HW}$)	I	**HOST/Hardware Mode Select:** This input pin is used to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SClk, and $\overline{CS}$ pins). Setting this input pin "High" enables the Microprocessor Serial Interface (e.g. configures the XRT73L03 to operate in the HOST Mode). In this mode, configure the XRT73L03 via the Microprocessor Serial Interface. When the XRT73L03 is operating in the HOST Mode, then it ignores the states of many of the discrete input pins. Setting this input pin "Low" disables the Microprocessor Serial Interface (e.g., configures the XRT73L03 to operate in the Hardware Mode). In this mode, many of the external input control pins are functional.
43	RxClk3	O	**Receive Clock Output pin - Channel 3:** This output pin is the Recovered Clock signal from the incoming line signal for Channel 3. The receive section of Channel 3 outputs data via the RPOS3 and RNEG3 output pins on the rising edge of this clock signal. ***NOTE:*** *The Receive Section of Channel 3 is configured to update the data on the RPOS3 and RNEG3 output pins on the falling edge of RxClk3 by doing one of the following:* **a. Operating in the Hardware Mode** Pull the RxClkINV pin (pin 62) to "High". **b. Operating in the HOST Mode** Write a "1" into the RxClkINV bit-field of the Command Register.
44	RNEG3	O	**Receive Negative Data Output - Channel 3:** This output pin pulses "High" whenever Channel 3 of the XRT73L03 has received a Negative Polarity pulse in the incoming line signal at the RTIP3/ RRing3 inputs. ***NOTE:*** *If the Channel 3 B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
45	RPOS3	O	**Receive Positive Data Output - Channel 3:** This output pin pulses “High" whenever Channel 3 of the XRT73L03 has received a Positive Polarity pulse in the incoming line signal at the RTIP3/ RRing3 inputs. ***NOTE:*** *If the Channel 3 B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
46	RxDGND3	****	**Receive Digital GND - Channel 3:**

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
47	EXClk1	I	**External Reference Clock Input - Channel 1:** Apply a 34.368 MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications. The Clock Recovery PLL in Channel 1 uses this signal as a Reference Signal for Declaring and Clearing the Receive Loss of Lock Alarm. ***NOTES:*** 1. *It is permissible to use the same clock which is also driving the TxClk input pin.* 2. *It is permissible to operate the three Channels at different data rates.*
48	RxDVDD1	****	**Receive Digital 3.3V+ 5% VDD (for Receiver 1):**
49	RxClk1	O	**Receive Clock Output - Channel 1:** Refer to the description of pin 43, RxClk3
50	RNEG1	O	**Receive Negative Data Output - Channel 1:** Refer to the description of pin 44, RNEG3
51	RPOS1	O	**Receive Positive Data Output - Channel 1:** Refer to the description of pin 45, RPOS3
52	NC		**No Connection**
53	NC		**No Connection**
54	RxDGND1	****	**Receive Digital GND - Channel 1:**
55	RLOS1	O	**Receive Loss of Signal Output Indicator - Channel 1:** This output pin toggles "High" if Channel 1 in the XRT73L03 has detected a Loss of Signal Condition in the incoming line signal. The criteria the XRT73L03 uses to declare an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode.
56	LCV1	O	**Line Code Violation Indicator - Channel 1:** Whenever the Receive Section of Channel 1 detects a Line Code Violation, it pulses this output pin "High". This output pin remains "Low" at all other times. ***NOTE:*** *The XRT73L03 outputs an NRZ pulse via this output pin. It is advisable to sample this output pin via the RxClk1 clock output signal.*
57	RLOL1	O	**Receive Loss of Lock Output Indicator - Channel 1:** This output pin toggles "High" if Channel 1 of the XRT73L03 has detected a Loss of Lock Condition. Channel 1 declares an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXClk(n) input pin) by more than 0.5%.
58	RLOS3	O	**Receive Loss of Signal Output Indicator - Channel 3:** Refer to the description of pin 55, RLOS1
59	LCV3	O	**Line Code Violation Indicator - Channel 3:** Refer to the description of pin 56, LCV1
60	RLOL3	O	**Receive Loss of Lock Output Indicator - Channel 3:** Refer to the description of pin 57, RLOL1

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
61	$\overline{CS}$/(ENDECDIS)	I	**Microprocessor Serial Interface - Chip Select Input/Encoder-Decoder Disable Input:** This pin's functionality depends on whether the XRT73L03 is operating in the HOST or Hardware Mode. **HOST Mode - Chip Select Input** The Local Microprocessor must assert this pin (set it to "0") in order to enable communication with the XRT73L03 via the Microprocessor Serial Interface. ***NOTE:*** *This pin is internally pulled "High".* **Hardware Mode - Encoder/Decoder Disable Input** Setting this input pin "High" disables the B3ZS/HDB3 Encoder & Decoder blocks in the XRT73L03 and configures it to transmit and receive the line signal in an AMI format. Setting this input pin "Low" enables the B3ZS/HDB3 Encoder & Decoder blocks and configures it transmit and receive the line signal in the B3ZS format for STS-1/DS3 operation or in the HDB3 format for E3 operation. ***NOTE:*** *If the XRT73L03 is operating in the Hardware Mode, this pin setting configures the B3ZS/HDB3 Encoder and Decoder Blocks for all Channels.*
62	SClk/(RxOFF2)	I	**Microprocessor Serial Interface Clock Signal/Channel 2 Receiver Shut OFF Input:** The function of this pin depends on whether the XRT73L03 is operating in the HOST Mode or in the Hardware Mode. **HOST Mode - Microprocessor Serial Interface Clock Signal:** This signal is used to sample the data on the SDI pin on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. **Hardware Mode - Channel 2 Receiver Shut OFF input pin:** Setting this input pin "High" shuts off the Channel 2 receiver. Setting this input pin "Low" enables the Receive Section for full operation.
63	SDI/(RxOFF1)	I	**Serial Data Input for the Microprocessor Serial Interface/Channel 1 - Receiver Shut OFF Input pin:** The function of this input depends on whether the XRT73L03 is operating in the HOST Mode or in the Hardware Mode. **HOST Mode - Serial Data Input for the Microprocessor Serial Interface:** To read or write data into the Command Registers over the Microprocessor Serial Interface, apply the Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations to this pin. This input is sampled on the rising edge of the SClk pin (pin 18). **Hardware Mode - Channel 1 Receiver Shut OFF Input pin:** Setting this input pin "High" shuts off the Channel 1 receiver. Setting this input pin "Low" enables the Receive Section for full operation.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
64	SDO/(E3_Ch1)	I/O	**Serial Data Output from the Microprocessor Serial Interface/E3_Mode Select - Channel 1:** The function of this pin depends on whether the XRT73L03 is operating in the HOST Mode or in the Hardware Mode. **HOST Mode Operation - Serial Data Output for the Microprocessor Serial Interface:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SClk input signal and tri-stated upon completion of data transfer. **Hardware Mode Operation - E3 Mode Select - Channel 1:** This input pin is used to configure Channel 1 in the XRT73L03 to operate in the E3 or STS/DS3 Modes. Setting this input pin to "High" configures Channel 1 to operate in the E3 Mode. Setting this input pin to "Low" configures Channel 1 to operate in either the DS3 or STS-1 Modes, depending upon the state of the STS-1/$\overline{DS3}$_Ch1 input pin (pin 31). ***NOTE:*** *This pin is internally pulled "Low" when XRT73L03 is in the Hardware Mode.*
65	STS1/$\overline{DS3}$_Ch1	I	**STS-1/DS3 Select Input - Channel 1:** "High" for STS-1 and "Low" for DS3 Operation. The XRT73L03 ignores this pin if the E3_Ch1 pin (pin 28) is set to "1". This input pin is ignored if the XRT73L03 is operating in the HOST Mode. If the XRT73L03 is operating in the HOST Mode, the pin should be tied to GND.
66	$\overline{ICT}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, set this pin "High". ***NOTE:*** *This pin is internally pulled "High".*
67	LOSTHR1	I	**Loss of Signal Threshold Control - Channel 1:** The voltage forced on this pin controls the input loss of signal threshold for Channel 1. Forcing the LOSTHR1 pin to GND or VDD provides two settings. This pin must be set to the desired level upon power up and should not be changed during operation. ***NOTE:*** *This pin is only applicable during DS3 or STS-1 operations.*
68	LLB1	I	**Local Loop-back - Channel 1:** This input pin along with RLB1 dictates the Loop-Back mode in which Channel 1 in the XRT73L03 is operating. A "High" on this pin with RLB1 set to "Low" configures Channel 1 of the XRT73L03 to operate in the Analog Local Loop-back Mode. A "High" on this pin with RLB1 set to "High" configures Channel 1 of the XRT73L03 to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L03 is operating in the HOST Mode.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	RLB1	I	**Remote Loop-back - Channel 1:** This input pin along with LLB1 dictates the Loop-Back mode in which Channel 1 in the XRT73L03 is operating. A "High" on this pin with LLB1 being set to "Low" configures Channel 1 of the XRT73L03 to operate in the Remote Loop-back Mode. A "High" on this pin with LLB1 also being set to "High" configures Channel 1 of the XRT73L03 to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L03 is operating in the HOST Mode.*
70	RxAVDD1	****	**Receive Analog 3.3V+ 5% VDD - Channel 1**
71	RRing1	I	**Receive Ring Input - Channel 1:** This input pin along with RTIP1 is used to receive the bipolar line signal from the Remote DS3/E3 Terminal.
72	RTIP1	I	**Receive TIP Input - Channel 1:** This input pin along with RRing1 is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
73	RxAGND1	****	**Receive Analog GND - Channel 1**
74	REQEN1	I	**Receive Equalization Enable Input - Channel 1:** Setting this input pin "High" enables the Internal Receive Equalizer of Channel 1. Setting this pin "Low" disables the Internal Receive Equalizer. The guide-lines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L03 is operating in the HOST Mode.*
75	LOSTHR3	I	**Loss of Signal Threshold Control - Channel 3:** Refer to the description of pin 67, LOSTHR1
76	LLB3	I	**Local Loop-back - Channel 3:** Refer to the description of pin 68, LLB1
77	RLB3	I	**Remote Loop-back - Channel 3:** Refer to the description of pin 69, RLB1
78	RxAVDD3	****	**Receive Analog 3.3V+ 5% VDD - Channel 3**
79	RRing3	I	**Receive Ring Input - Channel 3:** Refer to the description of pin 71, RRing1
80	RTIP3	I	**Receive TIP Input - Channel 3:** Refer to the description of pin 72, RTIP1
81	RxAGND3	****	**Receive Analog GND - Channel 3**
82	REQEN2	I	**Receive Equalization Enable Input - Channel 2:** Refer to the description of pin 74, REQEN1
83	RxAGND2	****	**Receive Analog GND - Channel 2**
84	RTIP2	I	**Receive TIP Input - Channel 2:** Refer to the description of pin 72, RTIP 1

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
85	RRing2	I	**Receive Ring Input - Channel 2:** Refer to the description of pin 71, RRing 1
86	RxAVDD2	****	**Receive Analog 3.3V+ 5% VDD - Channel 2**
87	RLB2	I	**Remote Loop-back - Channel 2:** Refer to the description of pin 69, RLB1
88	LLB2	I	**Local Loop-back - Channel 2:** Refer to the description of pin 68, LLB1
89	LOSTHR2	I	**Loss of Signal Threshold Control - Channel 2:** Refer to the description of pin 67, LOSTHR1
90	NC		**No Connection**
91	NC		**No Connection**
92	E3_Ch2	I	**E3 Select Input - Channel 2:** A "High" on this pin configures Channel 2 of the XRT73L03 to operate in the E3 Mode. A "Low" on this pin configures Channel 2 of the XRT73L03 to check the state of the STS-1/$\overline{DS3}$_Ch2 input pin ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L03 is operating in the HOST Mode.*
93	SR/($\overline{DR}$)	I	**Receive Output Single-Rail/Dual-Rail Select:** Setting this pin "High" configures the Receive Sections of all Channels to output data in a Single-Rail Mode to the Terminal Equipment. Setting this pin "Low" configures the Receive Section of all Channels to output data in a Dual-Rail Mode to the Terminal Equipment.
94	AGND3	****	**Analog Ground (Substrate Connection) - Channel 3**
95	STS1/$\overline{DS3}$_Ch2	I	**STS-1/DS3 Select Input - Channel 2:** Refer to the description of pin 65, STS1/DS3_Ch1
96	$\overline{REGR}$/(RxClk-INV)	I	**Register Reset Input pin (Invert RxClk(n)) Output - Select):** The function of this pin depends upon whether the XRT73L03 is operating in the HOST Mode or in the Hardware Mode. ***NOTE:*** *This pin is internally pulled "High".* **In the HOST-Mode - Register Reset Input pin:** Setting this input pin "Low" causes the XRT73L03 to reset the contents of the Command Registers to their default settings and default operating configuration. **In the Hardware Mode - Invert RxClk Output Select:** Setting this input pin "High" configures the Receive Section of all Channels in the XRT73L03 to invert their RxClk(n) clock output signals and configures Channel (n) to output the recovered data via the RPOS(n) and RNEG(n) output pins on the falling edge of RxClk(n). Setting this pin "Low" configures Channel (n) to output the recovered data via the RPOS(n) and RNEG(n) output pins on the rising edge of RxClk(n).
97	EXDGND	****	**External Reference Clock GND**

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
98	EXDVDD	****	**External Reference Clock Power Supply**
99	EXClk2	I	**External Reference Clock Input - Channel 2:** Refer to the description of pin 49, EXCLK1
100	REQEN3	I	**Receive Equalization Enable Input - Channel 3:** Refer to the description of pin 74, REQEN1
101	STS1/$\overline{DS3}$_Ch3	I	**STS-1/DS3 Select Input - Channel 3:** Refer to the description of pin 65, STS1/DS3_Ch1
102	E3_CH3	I	**E3 Select Input - Channel 3:** Refer to the description of pin 92, E3_Ch2
103	EXClk3	I	**External Reference Clock Input - Channel 3:** Refer to the description of pin 49, EXCLK1
104	RxOFF3		**Channel 3 Receiver Shut OFF Input:** **Hardware Mode - Channel 3 Receiver Shut OFF Input pin:** Setting this input pin "High" shuts off the Receive Section in Channel 3. Setting this input pin "Low" enables the Receive Section for full operation.
105	RLOL2	O	**Receive Loss of Lock Output Indicator - Channel 2:** Refer to the description of pin 57, RLOL1
106	LCV2	O	**Line Code Violation Indicator - Channel 2:** Refer to the description of pin 56, LCV1
107	RLOS2	O	**Receive Loss of Signal Output Indicator - Channel 2:** Refer to description of pin 55, RLOS1
108	RxDGND2	****	**Receive Digital Ground - Channel 2**
109	RPOS2	O	**Receive Positive Pulse Output - Channel 2:** Refer to the description of pin 45, RPOS3
110	RNEG2	O	**Receive Negative Pulse Output - Channel 2:** Refer to the description of pin 44, RNEG3
111	RxClk2	O	**Receive Clock Output pin - Channel 2:** Refer to the description of pin 43, RxClk3
112	LOSMUTEN	I	**MUTE-upon-LOS Enable Input (Hardware Mode):** This input pin is used to configure the XRT73L03 while it is operating in the Hardware Mode to MUTE the recovered data via the RPOS(n), RNEG(n) output pins whenever one of the Channels declares an LOS condition. Setting this input pin "High" configures all Channels to automatically pull the RPOS(n) and RNEG(n) output pins to GND whenever it is declaring an LOS condition, MUTing the data being output to the Terminal Equipment. Setting this input pin "Low" configures all Channels to NOT automatically MUTE the recovered data whenever an LOS condition is declared. ***NOTES:*** *1. This input pin is ignored and should be connected to GND if the XRT73L03 is operating in the HOST Mode.* *2. This pin is internally pulled "High".*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
113	RxDVDD2	****	**Receive Digital 3.3V+ 5% VDD - Channel 2**
114	AGND2	****	**Analog Ground (Substrate Connection) - Channel 2**
115	TxOFF3	I	**Transmitter OFF Input - Channel 3:** Refer to the description of pin 117, TxOFF1
116	TxOFF2	I	**Transmitter OFF Input - Channel 2:** Refer to the description of pin 117, TxOFF1
117	TxOFF1	I	**Transmitter OFF Input - Channel 1:** Setting this input pin "High" configures the XRT73L03 to turn off the Transmit Section of Channel 1. In this mode, the TTIP1 and TRing1 outputs is tri-stated. ***NOTES:*** 1. *This input pin controls the TTIP1 and TRing1 outputs even when the XRT73L03 is operating in the HOST Mode.* 2. *For HOST Mode Operation, tie this pin to GND if the Transmitter is intended to be turned off via the Microprocessor Serial Interface.*
118	TxAGND2	****	**Transmitter Analog GND - Transmitter 2**
119	TxAVDD2	****	**Transmitter Analog 3.3V+ 5% VDD - Transmitter 2**
120	DMO2	O	**Drive Monitor Output - Channel 2:** Refer to the description of pin 38, DMO1

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (T_A = 25^{0}C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DC Electrical Characteristics					
DV_{DD}	Digital DC Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog DC Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all "1's")		TBD	TBD	mA
V_{IL}	Input Low Voltage *			0.8	V
V_{IH}	Input High Voltage *	2.0		VDD	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA *	0		0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA *	2.8		VDD	V
I_L	Input Leakage Current *			±10	µA

NOTE: ** Not applicable to pins with pull-down resistors.*

ELECTRICAL CHARACTERISTICS (CONTINUED) (T_A = 25^{0}C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

AC Electrical Characteristics (Figure 3)					
Terminal Side Timing Parameters (see Figure 4 and Figure 5) -- {(n) =1, 2 or 3}					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
	TxClk(n) Clock Duty Cycle STS-1/DS3)	30	50	70	%
	TxClk(n) Clock Duty Cycle (E3)	30	50	70	%
	TxClk(n) Frequency (SONET STS-1)		51.84		MHz
	TxClk(n) Frequency (DS3)		44.736		MHz
	TxClk(n) Frequency (E3)		34.368		MHz
t_{RTX}	TxClk(n) Clock Rise Time (10% to 90%)		3	5	ns
t_{FTX}	TxClk(n) Clock Fall Time (90% to 10%)		3	5	ns
t_{TSU}	TPData(n)/TNData(n) to TxClk(n) Falling Set up time	3	1.5		ns
t_{THO}	TPData(n)/TNData(n) to TxClk(n) Falling Hold time	3	1.5		ns
t_{LCVO}	RxClk(n) to rising edge of LCV1(n) output delay		2.5		ns
t_{TDY}	TTIP(n)/TRing(n) to TxClk(n) Rising Propagation Delay time		8		ns
	RxClk(n) Clock Duty Cycle		50		%
	RxClk(n) Frequency (SONET STS-1)		51.84		MHz
	RxClk(n) Frequency (DS3)		44.736		MHz
	RxClk(n) Frequency (E3)		34.368		MHz
t_{CO}	RxClk(n) to RPOS(n)/RNEG(n) Delay Time	0	2.5		ns
t_{RRX}	RxClk(n) Clock Rise Time (10% to 90%)		1.5		ns
t_{FRX}	RxClk(n) Clock Fall Time (10% to 90%)		1.5		ns
C_I	Input Capacitance		5	TBD	pF
C_L	Load Capacitance		5	TBD	pF

NOTES:

1. *All XRT73L03 digital inputs are designed to be TTL 5V compliant.*
2. *All XRT73L03 digital outputs are also TTL 5V compliant. However these outputs will not drive to 5V nor will they accept external 5V pullups.*

FIGURE 3. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES (TYPICAL CHANNEL)

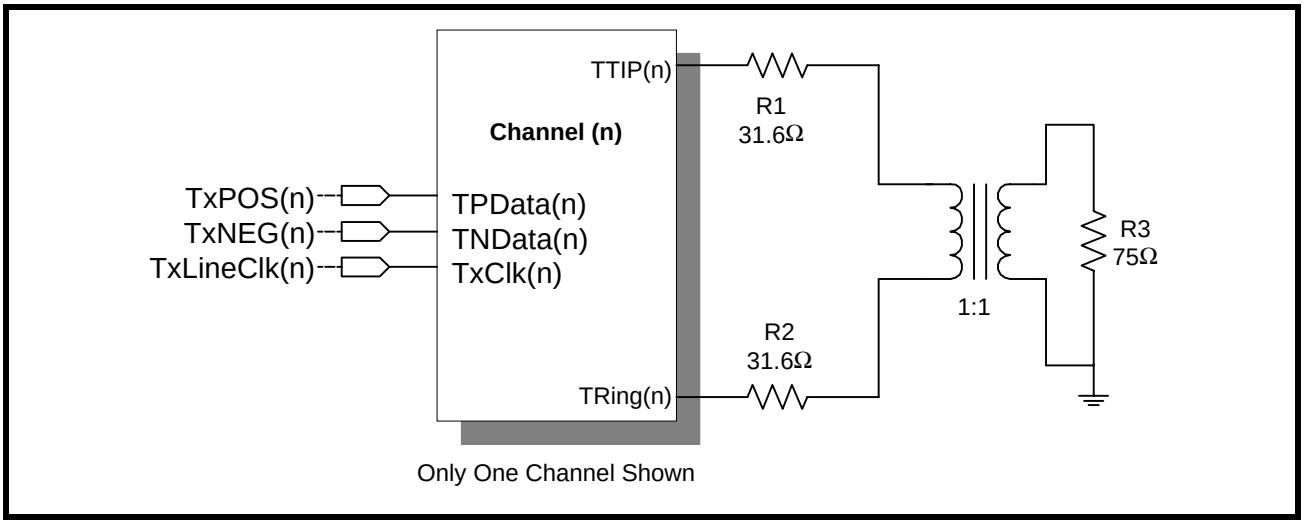


FIGURE 4. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE

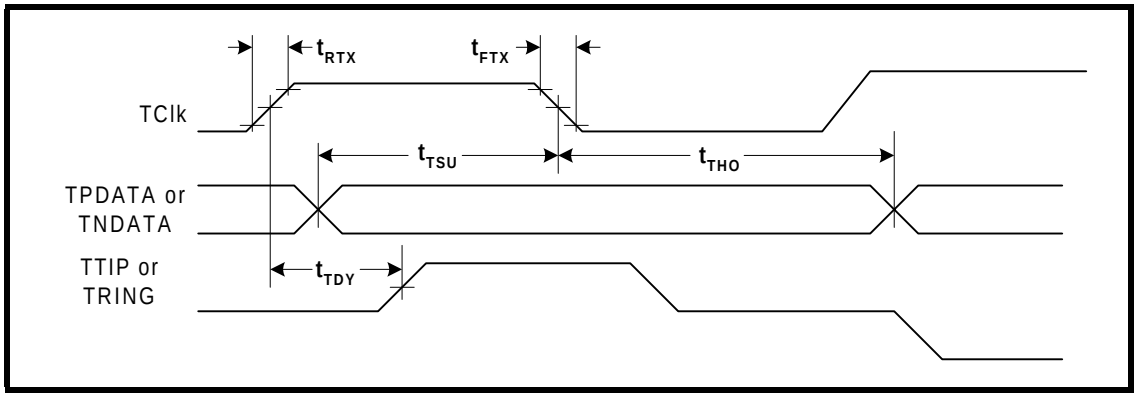
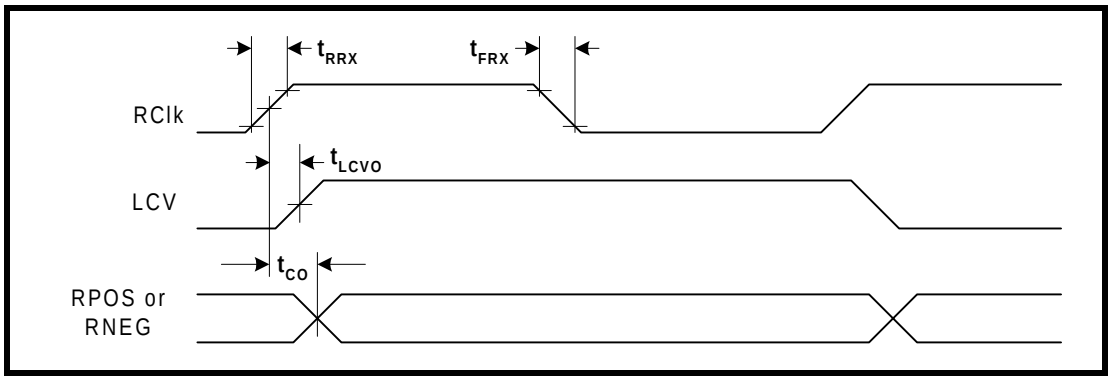


FIGURE 5. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE



ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25^{0}C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
Line Side Parameters E3 Application					
Transmit Characteristics (see Figure 3)					
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer, see Figure 1)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input @ TxClk(n)		0.02	0.05	UIpp
Receive Line Characteristics (See Figure 5)					
	Receive Sensitivity (Length of cable)		1200		feet
	Interference Margin		TBD		dB
	Signal Level to Declare Loss of Signal	-35			dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10		255	UI
	Termination of LOS to LOS Clearance Time	10		255	UI
	Intrinsic Jitter (As Measured in the RxClk(n) signal)		TBD		UI
	Jitter Transfer Function, -3dB Frequency		TBD		kHz
	Jitter Transfer Function, Peak Gain		TBD		dB
	Jitter Tolerance @ Jitter Frequency = 100Hz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 1kHz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 10kHz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 800kHz		TBD		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25^{0}C, V_{DD} = 3.3 ± 5%, UNLESS OTHERWISE SPECIFIED)

Line Side Parameters Sonet STS-1 Application					
Transmit Characteristics (See Figure 4)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
	Transmit Output Pulse Amplitude (Measured with TxLEV=0, see Figure 1)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured with TxLEV=1, see Figure 1)	0.93	0.98	1.08	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input @ TxClk(n)		0.02	0.05	UI
Receive Line Characteristics (See Figure 5)					
	Receive Sensitivity (Length of Table)		1000		feet
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 1)		90		mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 1)		240		mV
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 1)		35		mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 1)		90		mV
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 0)		70		mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 0)		190		mV
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 0)		35	90	mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 0)		65		mV
	Intrinsic Jitter (As Measured at the RxClk(n) Output Pin)		TBD		UI
	Jitter Transfer Function, -3dB Frequency		TBD		kHz
	Jitter Transfer Function, Peak Gain		TBD		dB
	Jitter Tolerance @ Jitter Frequency = 100Hz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 1kHz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 10kHz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 800kHz		TBD		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25^{0}C, V_{DD} = 3.3 ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
Line Side Parameters DS3 Application					
Transmit Characteristics (see Figure 4)					
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=0, see Figure 3)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=1, see Figure 3)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input @ TxClk(n)		0.02	0.05	UI
Receive Line Characteristics (See Figure 5)					
	Receive Sensitivity (Length of Table)		1000		feet
	Receive Intrinsic Jitter (All One's Pattern)		TBD		UI
	Receive Intrinsic Jitter (Using PRBS 2^23-1 Pattern)		TBD		UI
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 1)		70		mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 1)		200		mV
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 1)		35		mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 1)		80		mV
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 0)		50		mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 0, REQEN(n) = 0)	155	130		mV
	Signal Level to Declare Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 0)		25		mV
	Signal Level to Clear Loss of Signal (LOSTHR(n) = 1, REQEN(n) = 0)		55		mV
	Intrinsic Jitter (As Measured at the RxClk(n) Output Pin)		TBD		UI
	Jitter Transfer Function, -3dB Frequency		TBD		kHz
	Jitter Transfer Function, Peak Gain		TBD		dB
	Jitter Tolerance @ Jitter Frequency = 100Hz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 1kHz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 10kHz		TBD		UI
	Jitter Tolerance @ Jitter Frequency = 800kHz		TBD		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25^{0}C, V_{DD} = 3.3 ± 5%, UNLESS OTHERWISE SPECIFIED)

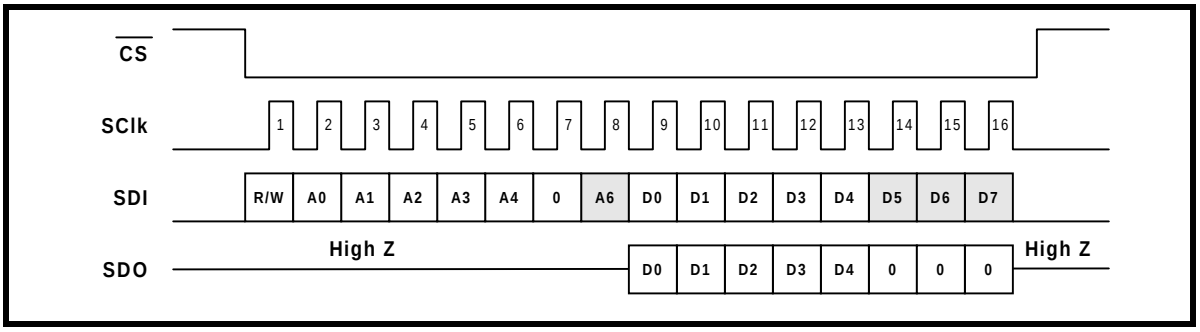
Microprocessor Serial Interface Timing (See Figure 6)					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk Setup Time	50			ns
t_{22}	$\overline{CS}$ High to Rising Edge of SClk Hold Time	20			ns
t_{23}	SDI to Rising Edge of SClk Setup Time	50			ns
t_{24}	SDI to Rising Edge of SClk Hold Time	50			ns
t_{25}	SClk "Low" Time	240			ns
t_{26}	SClk "High" Time	240			ns
t_{27}	SClk Period	500			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SClk Hold Time	50			ns
t_{29}	$\overline{CS}$ "Inactive" Time	250			ns
t_{30}	Falling Edge of SClk to SDO Valid Time			200	ns
t_{31}	Falling Edge of SClk to SDO Invalid Time			100	ns
t_{32}	Falling Edge of SClk, or rising edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			40	ns

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	- 65^{0}C to + 150^{0}C
Operating Temperature	- 40^{0}C to + 85^{0}C
Supply Voltage Range	-0.5V to +3.465V
Theta-JA	23° C/W
Theta-JC	7° C/W

NOTE: *The XRT73L03 is assembled in a thermally enhanced package with an intergral Copper Heat Slug. The Heat Slug is solder plated and is exposed on the bottom of the package and is electrically connected to the Ground connections of the device. This Heat Slug can be soldered to the mounting board if desired, but must be isolated from any V_{DD} connections.*

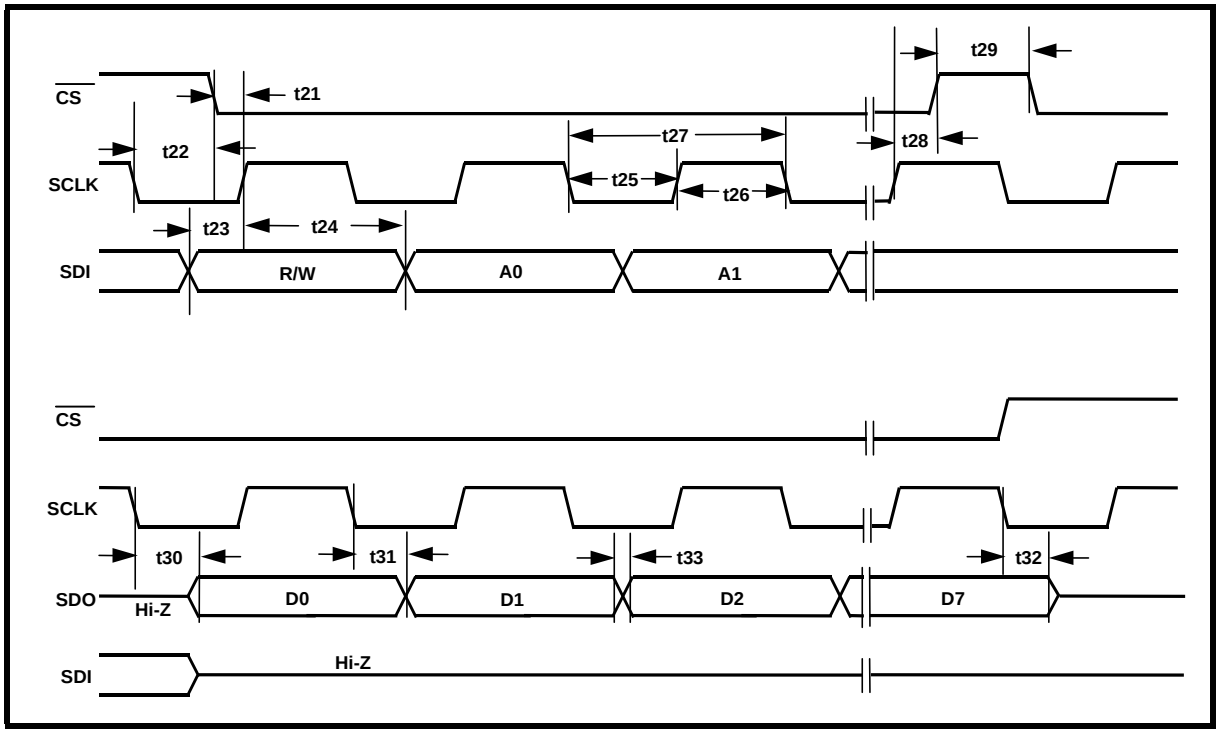
FIGURE 6. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



NOTES:

1. *A5 is always "0".*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*
4. *A shaded pulse denotes a "don't care" value.*

FIGURE 7. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



SYSTEM DESCRIPTION

A functional block diagram of the XRT73L03 E3/DS3/STS-1 Transceiver IC is presented in Figure 8. The XRT73L03 contains three independent transmitter and receiver sections and a common microprocessor interface section.

THE TRANSMIT SECTION - CHANNELS 1, 2 AND 3

The Transmit Section of each Channel accepts TTL/CMOS level signals from the Terminal Equipment in either a Single-Rail or Dual-Rail format. The Transmit Section takes this data and does the following:

- Encode this data into the B3ZS format if the DS3 or SONET STS-1 Modes have been selected, or into the HDB3 format if the E3 Mode has been selected.
- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements.
- Drive these pulses onto the line via the TTIP(n) and TRing(n) output pins across a 1:1 Transformer.

NOTE: *The Transmit Section drives a "1" (or a Mark) onto the line by driving either a positive or negative polarity pulse across the 1:1 Transformer in a given bit period. The Transmit Section drives a "0" (or a Space) onto the line by driving no pulse onto the line.*

THE RECEIVE SECTION - CHANNELS 1, 2 AND 3

The Receive Section of each Channel receives a bipolar signal from the line via the RTIP and RRing signals across a 1:1 Transformer or a 0.01µF Capacitor.

The recovered clock and data outputs to the Local Terminal Equipment in the form of CMOS level signals via the RPOS(n), RNEG(n) and RxClk(n) output pins.

THE MICROPROCESSOR SERIAL INTERFACE

The XRT73L03 contains three identical channels. The Microprocessor Interface Inputs are common to all channels. The descriptions that follow refer to Channel(n) where (n) represents Channel1, Channel2 or Channel3.

The XRT73L03 can be configured to operate in either the Hardware Mode or the HOST Mode.

a. Operating in the Hardware Mode

The XRT73L03 can be configured to operate in the Hardware Mode by tying the HOST/($\overline{HW}$) input pin (pin 8) to GND.

When the XRT73L03 is operating in the Hardware Mode, the following is true:

1. The Microprocessor Serial Interface block is disabled.
2. The XRT73L03 is configured via input pin settings.

Each of the pins associated with the Microprocessor Serial Interface takes on their alternative role as defined in Table 1.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT73L03 IS OPERATING IN THE HARDWARE MODE

PIN #	PIN NAME	FUNCTION WHILE IN HARDWARE MODE
61	$\overline{CS}$/(ENDECDIS)	ENDECDIS
62	SClk/(RxOFF2)	RxOFF2
63	SDI/(RxOFF1)	RxOFF1
64	SDO/(E3_Ch1)	E3_Ch1
96	$\overline{REGR}$/(RxClkINV)	RxCKlkINV

When the XRT73L03 is operating in the Hardware Mode, all of the remaining input pins become active.

b. Operating in the HOST Mode

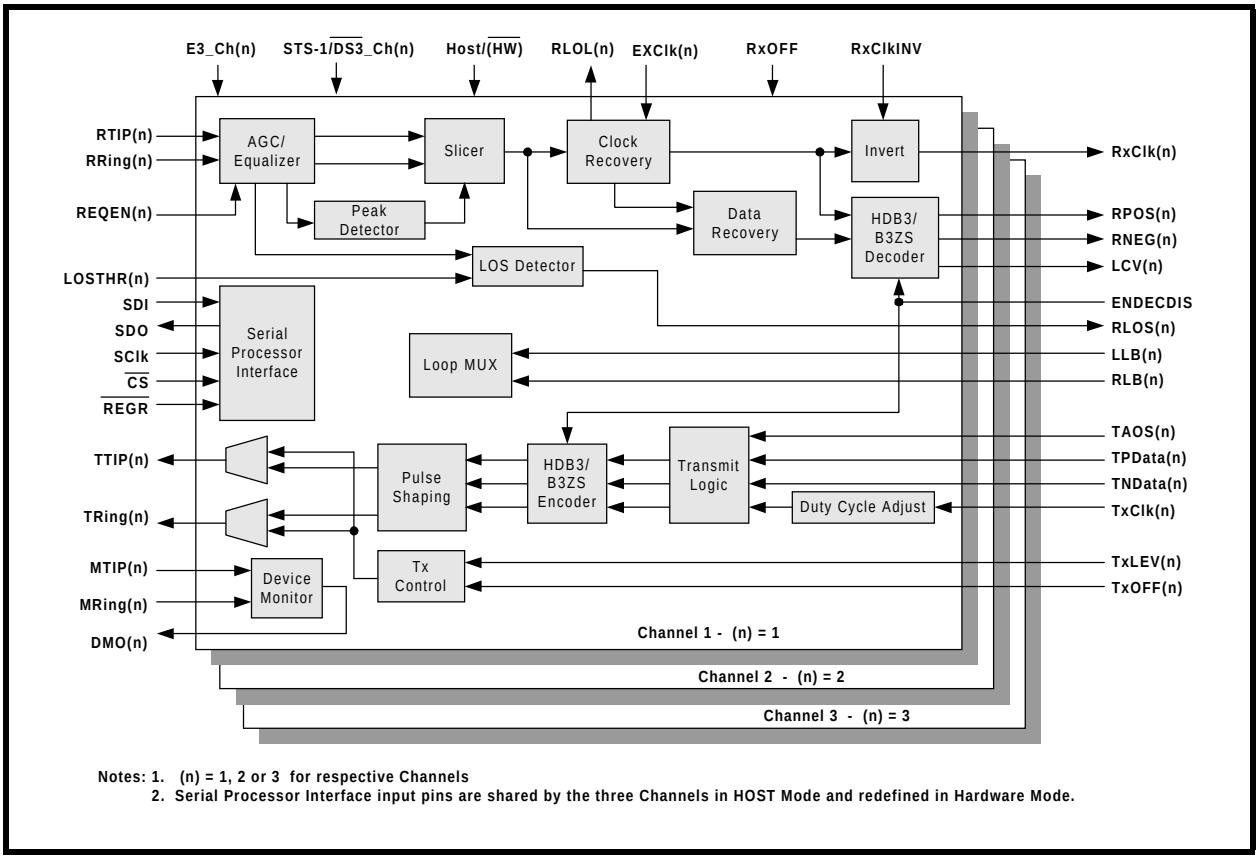
The XRT73L03 can be configured to operate in the HOST Mode by tying the HOST/($\overline{HW}$) input pin (pin 8) to VDD.

When the XRT73L03 is operating in the HOST Mode, the following is true:

1. The Microprocessor Serial Interface block is enabled. Writing the appropriate data into the on-chip Command Registers makes many configuration selections.
2. All of the following input pins are disabled and should be connected to GND.
   - Pins 8, 9 & 35 - TxLEV(n)
   - Pins 6, 7 & 36 - TAOS(n)
   - Pin 74, 82 & 100 - REQEN(n)
   - Pin 69, 77 & 87 - RLB(n)
   - Pin 68, 76 & 88 - LLB(n)
   - Pin 92 & 102 - E3_Ch(n)
   - Pin 65, 95 & 101 - STS1/$\overline{DS3}$_Ch(n)

In HOST Mode Operation, the TxOFF(n) input pins can still be used to turn on or turn off the Transmit Output Drivers in Channels 1, 2 and 3, respectively. The intent behind this feature is to permit a system designed for redundancy to quickly switch out a defective line card and switch-in the back-up line card.

FIGURE 8. FUNCTIONAL BLOCK DIAGRAM OF THE XRT73L03



Notes: 1. (n) = 1, 2 or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the three Channels in HOST Mode and redefined in Hardware Mode.

1.0 SELECTING THE DATA RATE

Each channel in the XRT73L03 can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or SONET STS-1 (51.84 Mbps) rates and to operate in a mode/data rate that is independent of the other channels.

Two methods are available to select the data rate for each channel of the XRT73L03.

1.1 CONFIGURING CHANNEL(N)

Refer to Table 2 to determine the appropriate Address for each Command Register of each channel in the XRT73L03. The Command Register description refers to CR(m)-(n), where (m) = 0 to 7 and (n) refers to a particular channel of the XRT73L03.

TABLE 2: ADDRESSES AND BIT FORMATS OF XRT73L03 COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	**COMMAND REGISTER**	**TYPE**	**D4**	**D3**	**D2**	**D1**	**D0**
CHANNEL1							
0x00	CR0-1	RO	RLOL1	RLOS1	ALOS1	DLOS1	DMO1
0x01	CR1-1	R/W	TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
0x02	CR2-1	R/W	Reserved	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
0x03	CR3-1	R/W	SR/(DR)_1	LOSMUT1	RxOFF1	RxClk1INV	Reserved
0x04	CR4-1	R/W	Reserved	STS-1/DS3_Ch1	E3_Ch1	LLB1	RLB1

TABLE 2: ADDRESSES AND BIT FORMATS OF XRT73L03 COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	TYPE	D4	D3	D2	D1	D0
0x05	CR5-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL2							
0x08	CR0-2	RO	RLOL2	RLOS2	ALOS2	DLOS2	DMO2
0x09	CR1-2	R/W	TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
0x0A	CR2-2	R/W	Reserved	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
0x0B	CR3-2	R/W	SR/($\overline{DR}$)_2	LOSMUT2	RxOFF2	RxClk2INV	Reserved
0x0C	CR4-2	R/W	Reserved	STS-1/$\overline{DS3}$_Ch2	E3_Ch2	LLB2	RLB2
0x0D	CR5-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0E	CR6-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0F	CR7-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL3							
0x10	CR0-3	RO	RLOL3	RLOS3	ALOS3	DLOS3	DMO3
0x11	CR1-3	R/W	TxOFF3	TAOS3	TxClkINV3	TxLEV3	TxBIN3
0x12	CR2-3	R/W	Reserved	ENDECDIS3	ALOSDIS3	DLOSDIS3	REQEN3
0x13	CR3-3	R/W	SR/($\overline{DR}$)_3	LOSMUT3	RxOFF3	RxClk3INV	Reserved
0x14	CR4-3	R/W	Reserved	STS-1/$\overline{DS3}$_Ch3	E3_Ch3	LLB3	RLB3
0x15	CR5-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x16	CR6-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x17	CR7-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Address:

The register addresses presented in the **Hexadecimal** format.

Type:

The Command Registers are either Read-Only (RO) or Read/Write (R/W) type of registers.

The default value for each of the bit-fields in these registers is "0".

a. Operating in the Hardware Mode

To configure individual Channel Data Rate, set the E3_Ch(n) and the STS-1/$\overline{DS3}$_Ch(n) input pins (where n = 1, 2 or 3) to the appropriate logic states referenced in Table 3.

TABLE 3: SELECTING THE DATA RATE FOR CHANNEL(N) OF THE XRT73L03, VIA THE E3_CH(N) AND STS-1/$\overline{\text{DS3}}$_CH(N) INPUT PINS (HARDWARE MODE)

DATA RATE	STATE OF E3_CH(N) PIN (PIN 64, 92, 102)	STATE OF STS-1/$\overline{\text{DS3}}$_CH(N) PIN (PIN 65, 95, 101)	MODE OF B3ZS/HDB3 ENCODER/ DECODER BLOCKS
E3 (34.368 Mbps)	1	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	1	B3ZS

b. Operating in the HOST Mode.

To configure the Data Rate of a Channel, write the appropriate values into the STS-1/$\overline{\text{DS3}}$_Ch(n) and E3_Ch(n) bit-fields in Command Register CR4-(n).

NOTE: *Reference Table 2 for the correct address of each channel.*

COMMAND REGISTER CR4-(N)

D4	D3	D2	D1	D0
X	STS-1/($\overline{\text{DS3}}$)_(n))	E3_Ch(n)	LLB(n)	RLB(n)
x	x	x	x	x

Table 4 relates the values of these two bit-fields to the selected data rates.

TABLE 4: SELECTING THE DATA RATE FOR CHANNEL(N) OF THE XRT73L03 VIA THE STS-1/$\overline{\text{DS3}}$_CH(N) AND THE E3_CH(N) BIT-FIELDS IN THE APPROPRIATE COMMAND REGISTER (HOST MODE)

SELECTED DATA RATE	STS-1/$\overline{\text{DS3}}$_(N) (D3)	E3_CH(N) (D2)
E3	X (Don't Care)	1
DS3	0	0
STS-1	1	0

2.0 THE TRANSMIT SECTION

Figure 8 shows the Transmit Section in each Channel of the XRT73L03 consists of the following blocks:

- Transmit Logic Block
- TxClk(n) Duty Cycle Adjust Block
- HDB3/(B3ZS) Encoder
- Pulse Shaping Block

The purpose of the Transmit Section in each Channel of the XRT73L03 is to take TTL/CMOS level data from the Terminal Equipment and encode it into a format that can:

1. be efficiently transmitted over coaxial cable at E3, DS3 or STS-1 data rates,
2. be reliably received by the Remote Terminal Equipment at the other end of the E3, DS3 or STS-1 data link, and
3. comply with the applicable pulse template requirements.

The circuitry that the Transmit Section in each Channel of the XRT73L03 takes to accomplish this goal is discussed below.

2.1 THE TRANSMIT LOGIC BLOCK

The purpose of the Transmit Logic Block is to accept either Dual-Rail or Single-Rail (binary data stream) TTL/CMOS level data and timing information from the Terminal Equipment.

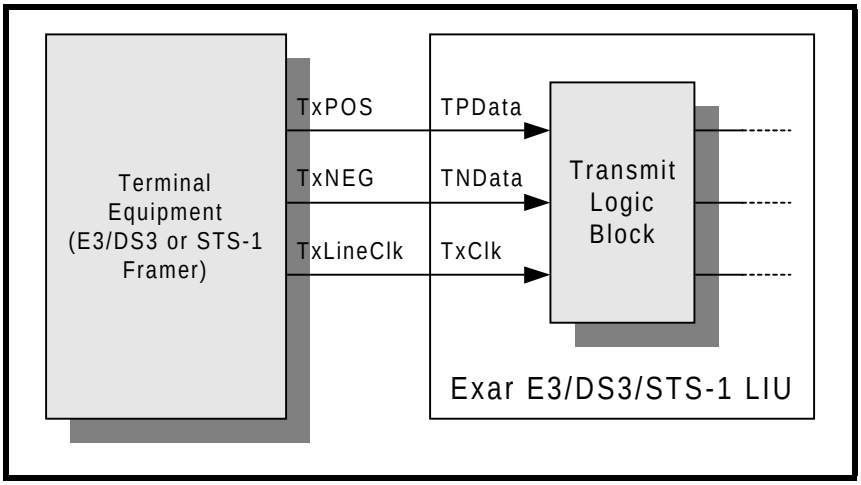
2.1.1 Accepting Dual-Rail Data from the Terminal Equipment

Whenever the XRT73L03 accepts Dual-Rail data from the Terminal Equipment, it does so via the following input signals:

- TPData(n)
- TNData(n)
- TxClk(n)

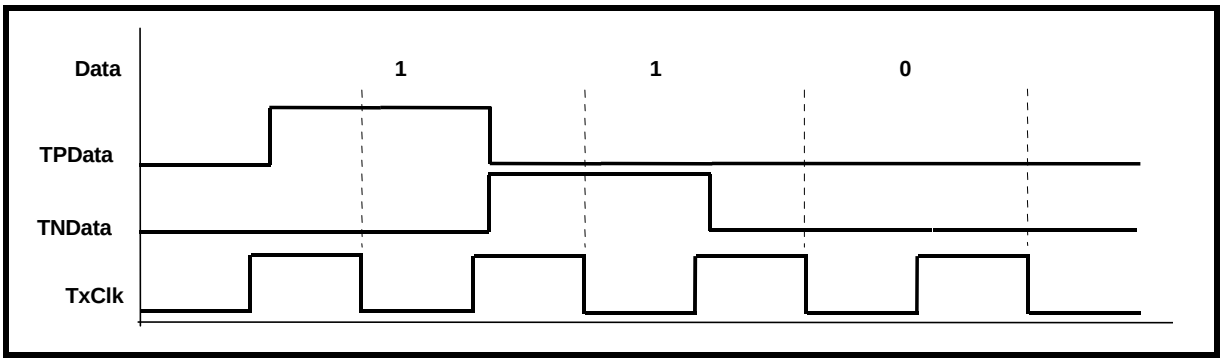
Figure 9 illustrates the typical interface for the transmission of data in a Dual-Rail Format between the Terminal Equipment and the Transmit Section of the XRT73L03.

FIGURE 9. THE TYPICAL INTERFACE FOR DATA TRANSMISSION IN DUAL-RAIL FORMAT FROM THE TRANSMITTING TERMINAL EQUIPMENT TO THE TRANSMIT SECTION OF A CHANNEL OF THE XRT73L03



The manner that the LIU handles Dual-Rail data is described below and illustrated in Figure 10. The Transmit Section of a Channel typically samples the data on the TPData and TNData input pins on the falling edge of TxClk(n).

FIGURE 10. HOW THE XRT73L03 SAMPLES THE DATA ON THE TPDATA AND TNDATA INPUT PINS



TxClk(n) is the clock signal that is of the selected data rate frequency for E3 = 34.368 MHz, DS3 = 44.736 MHz and STS-1 = 51.84 MHz. If the Transmit Section samples a “1" on the TPData input pin, the Transmit Section of the XRT73L03 generates a positive polarity pulse via the TTIP(n) and TRing(n) output pins across a 1:1 transformer. If the Transmit Section samples a "1" on the TNData input pin, then the Transmit Section ultimately generates a negative polarity pulse via the TTIP(n) and TRing(n) output pins across a 1:1 transformer.

2.1.2 Configure Channel(n) to accept Single-Rail Data from the Terminal Equipment

To transmit data in a Single-Rail data from the Terminal Equipment, configure the XRT73L03 in the HOST Mode.

Write a "1" into the TxBin(n) (TRANSMIT BINary) bit-field of Command Register CR1-(n) shown below.

NOTE: *Please refer to Table 2 for the Address of the individual Channel(n).*

COMMAND REGISTER CR1-(N)

D4	D3	D2	D1	D0
TxOFF(n)	TAOS(n)	TxClkINV(n)	TxLEV(n)	TxBin(n)
x	x	x	x	1

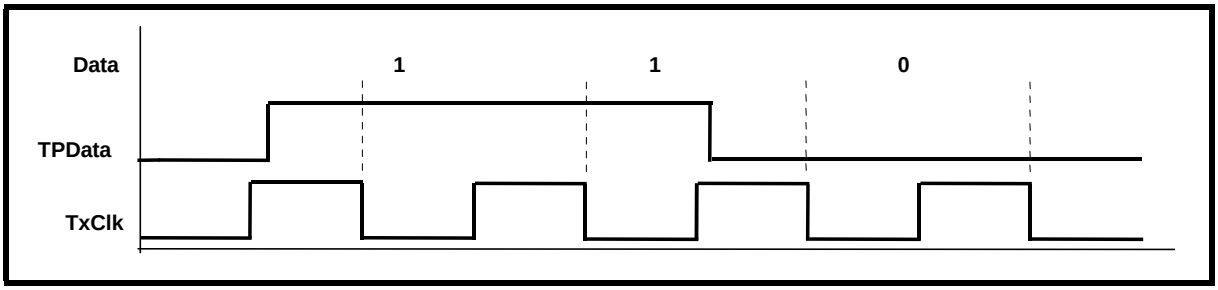
The Transmit Section of each channel samples this input pin on the falling edge of the TxClk(n) clock signal and encodes this data into the appropriate bipolar line signal across the TTIP(n) and TRing(n) output pins.

NOTES:

1. *In this mode the Transmit Logic Block ignores the TNData input pin.*
2. *If the Transmit Section of a given channel is configured to accept Single-Rail data from the Terminal Equipment, the B3ZS/HDB3 Encoder must be enabled.*

Figure 11 illustrates the behavior of the TPData and TxClk(n) signals when the Transmit Logic Block has been configured to accept Single-Rail data from the Terminal Equipment.

FIGURE 11. THE BEHAVIOR OF THE TPDATA AND TXCLK INPUT SIGNALS WHILE THE TRANSMIT LOGIC BLOCK IS ACCEPTING SINGLE-RAIL DATA FROM THE TERMINAL EQUIPMENT



2.2 THE TRANSMIT CLOCK DUTY CYCLE ADJUST CIRCUITRY

The on-chip Pulse-Shaping circuitry in the Transmit Section of each Channel of the XRT73L03 generates pulses of the appropriate shapes and width to meet the applicable pulse template requirements. The widths of these output pulses are defined by the width of the half-period pulses in the TxClk(n) signal.

However, if the widths of the pulses in the TxClk(n) clock signal are allowed to vary significantly, this could jeopardize the chip's ability to generate Transmit Output pulses of the appropriate width, thereby not meeting the Pulse Template requirement specification. Consequently, the chip's ability to generate compliant pulses could depend upon the duty cycle of the clock signal applied to the TxClk(n) input pin.

The Transmit Clock Duty Cycle Adjust Circuitry accepts clock pulses via the TxClk(n) input pin at duty cycles ranging from 30% to 70% and converts them to a 50% duty cycle.

2.3 THE HDB3/B3ZS ENCODER BLOCK

The purpose of the HDB3/B3ZS Encoder Block is to aid in the Clock Recovery process at the Remote Terminal Equipment by ensuring an upper limit on the number of consecutive zeros that can exist in the line signal.

2.3.1 B3ZS Encoding

If the XRT73L03 has been configured to operate in the DS3 or SONET STS-1 Modes, the HDB3/B3ZS Encoder blocks operate in the B3ZS Mode. When the Encoder is operating in this mode it parses through and searches the Transmit Binary Data Stream from the Transmit Logic Block for the occurrence of three (3) consecutive zeros (e.g., "000"). If the B3ZS Encoder finds an occurrence of three consecutive zeros, then it substitutes these three "0's" with either a "00V" or a "B0V" pattern.

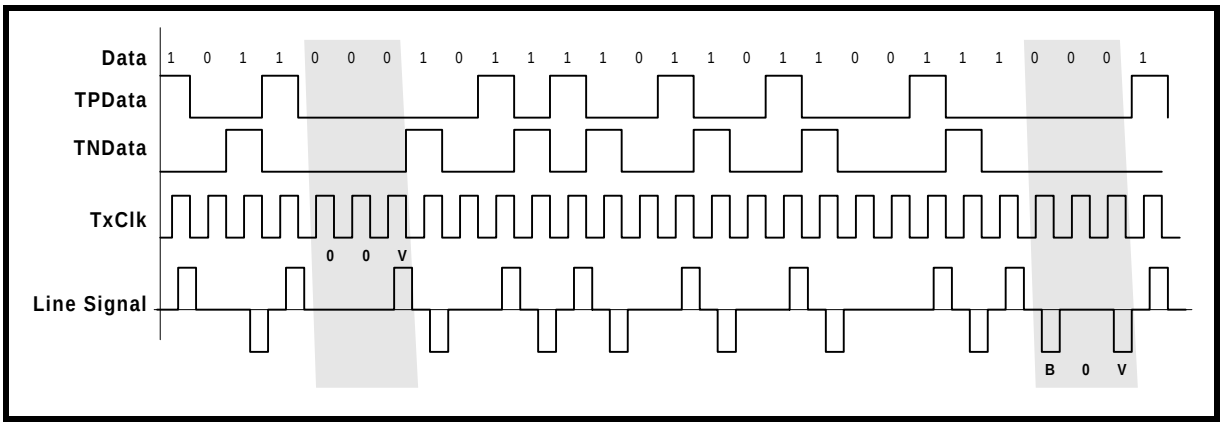
"B" represents a Bipolar pulse that is compliant with the Alternating Polarity requirements of the AMI (Alternate Mark Inversion) line code.

"V" represents a Bipolar Violation (e.g., a Bipolar pulse that violates the Alternating Polarity requirements of the AMI line code).

The B3ZS Encoder decides whether to substitute with either the "00V" or the "B0V" pattern in order to insure that an odd number of Bipolar pulses exist between any two consecutive violation pulses.

Figure 12 illustrates the B3ZS Encoder at work with two separate strings of three or more consecutive zeros.

FIGURE 12. AN EXAMPLE OF B3ZS ENCODING

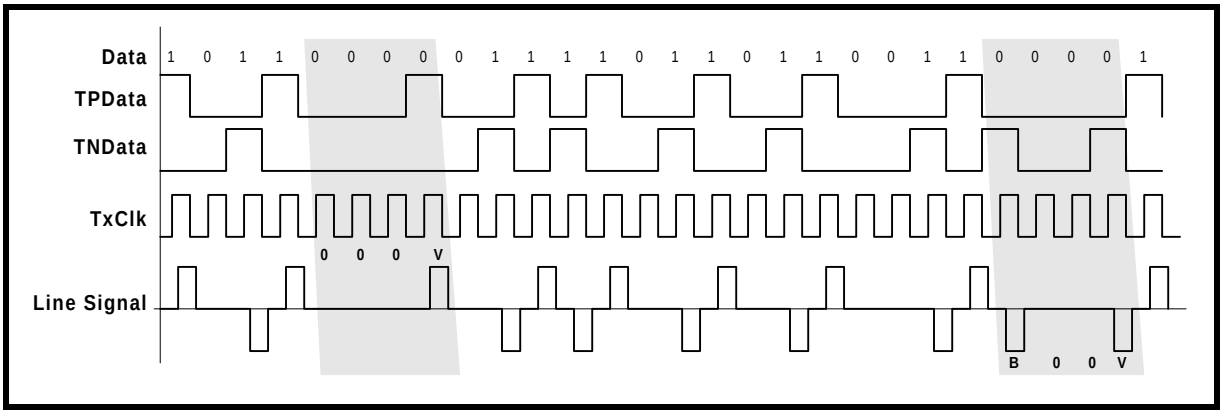


2.3.2 HDB3 Encoding

If the XRT73L03 has been configured to operate in the E3 Mode, the HDB3/B3ZS Encoder blocks operate in the HDB3 Mode. When the Encoder is operating in this mode it parses through and searches the Transmit Data Stream from the Transmit Logic Block for the occurrence of four (4) consecutive zeros ("0000"). If the HDB3 Encoder finds an occurrence of four consecutive zeros then it substitutes these four "0's" with either a "000V" or a "B00V" pattern. The HDB3 Encoder decides whether to substitute with either the "000V" or the "B00V" pattern in order to insure that an odd number of Bipolar pulses exist between any two consecutive violation pulses.

Figure 13 illustrates the HDB3 Encoder at work with two separate strings of four or more consecutive zeros.

FIGURE 13. AN EXAMPLE OF HDB3 ENCODING



2.3.3 Disabling the HDB3/B3ZS Encoder

The XRT73L03 HDB3/B3ZS Encoder can be disabled by two methods.

a. Operating in the Hardware Mode.

The HBD3/B3ZS Encoder blocks of all channels are disabled by setting the ENDECDIS (Encoder/ Decoder Disable) input pin (pin 25) to “0".

NOTE: *By executing this step the HDB3/B3ZS Encoder and Decoder blocks in all channels of the XRT73L03 are globally disabled.*

b. Operating in the HOST Mode.

When the XRT73L03 is operating in the HOST Mode the HDB3/B3ZS Encoders in each channel can be individually enabled or disabled. Disable the HDB3/B3ZS Encoder block in Channel(n) by

setting the ENDECDIS(n) bit-field in Command Register (CR2-(n)), to "1".

COMMAND REGISTER CR2-(N)

D4	D3	D2	D1	D0
Reserved	ENDECDIS(n)	ALOSDIS(n)	DLOSDIS(n)	REQEN(n)
x	1	x	x	x

If either of these two methods is used to disable the HDB3/B3ZS Encoder, the LIU transmits the data as received via the TPData and TNData input pins.

2.4 THE TRANSMIT PULSE SHAPING CIRCUITRY

The Transmit Pulse Shaper Circuitry consists of a Transmit Line Build-Out circuit which can be enabled or disabled by setting the TxLEV(n) input pin or TxLEV(n) bit-field to "High" or "Low". The purpose of the Transmit Line Build-Out circuit is to permit configuration of each channel in the XRT73L03 to transmit an output pulse which is compliant to either of the following pulse template requirements when measured at the Digital Cross Connect System. Each of these Bellcore specifications state that the cable length between the Transmit Output and the Digital Cross Connect system can range anywhere from 0 to 450 feet.

The Isolated DSX-3 Pulse Template Requirement per Bellcore GR-499-CORE is illustrated in Figure 14 and the Isolated STSX-1 Pulse Template Requirement per Bellcore GR-253-CORE is illustrated in Figure 15.

FIGURE 14. THE BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

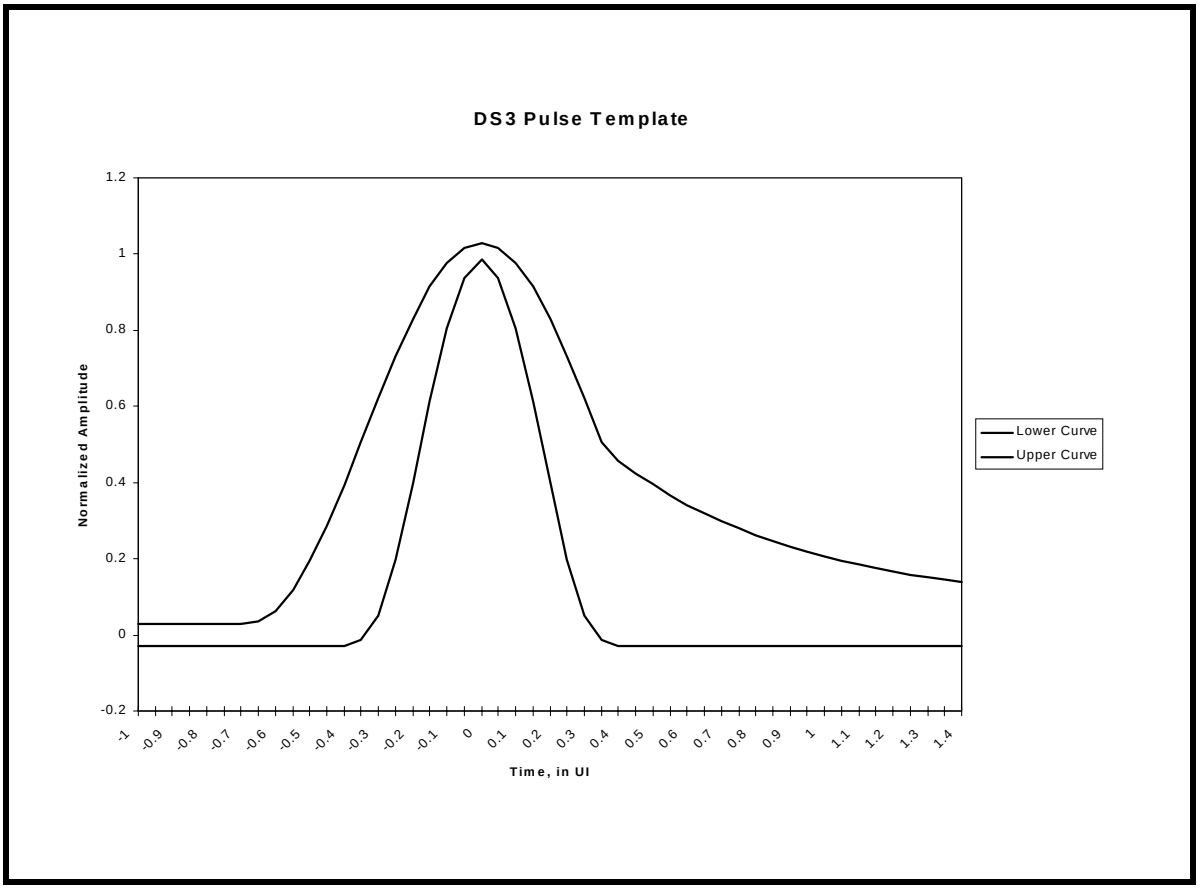
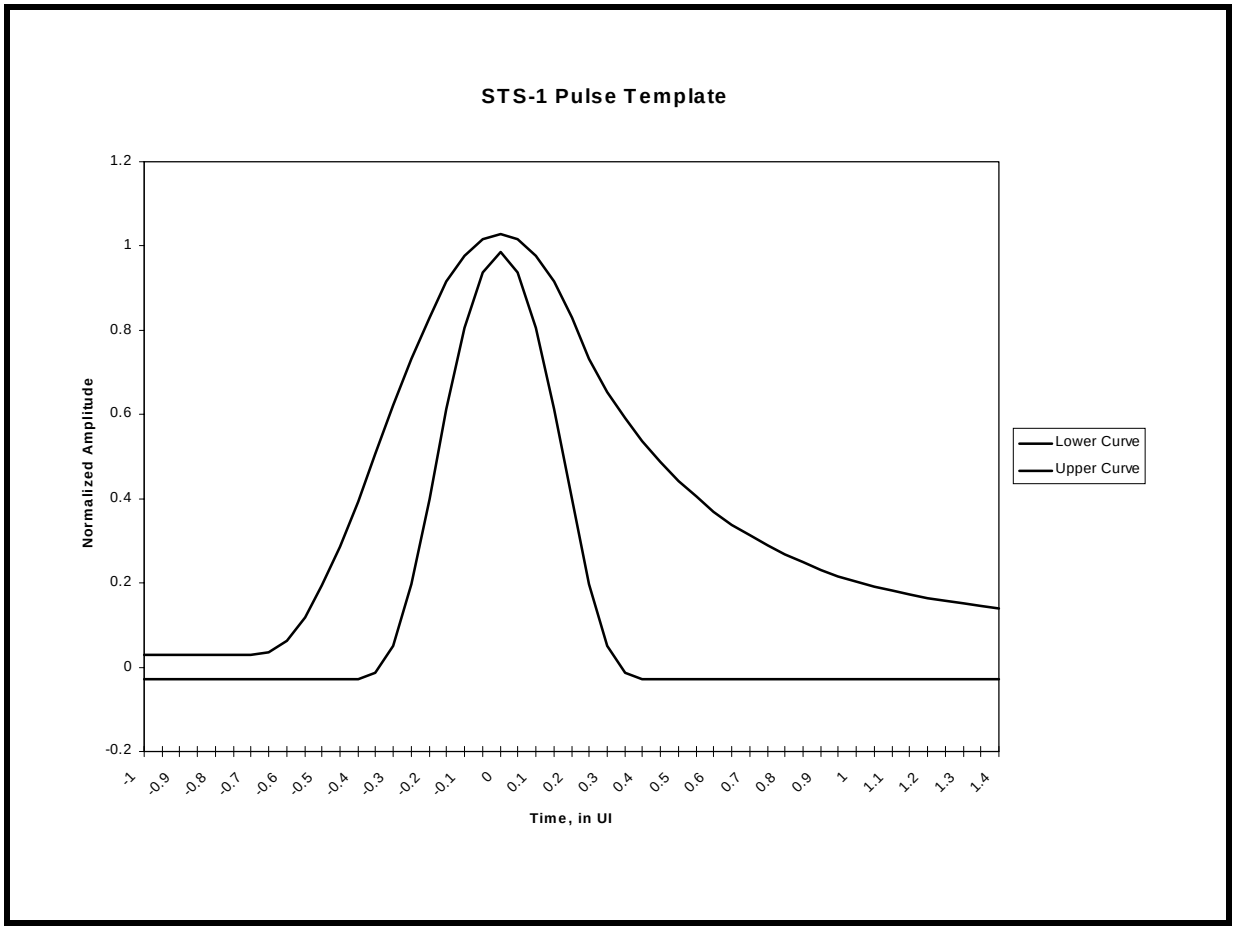


FIGURE 15. THE BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS



2.4.1 Enabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out Circuit is enabled, the Transmit Section of Channel(n) of the XRT73L03 outputs shaped pulses onto the line via the TTIP(n) and TRing(n) output pins.

Enable the Transmit Line Build-Out circuit for each channel in the XRT73L03 by doing the following:

a. Operating in the Hardware Mode

Set the TxLEV(n) input pin to "Low"

b. Operating in the HOST Mode

Set the TxLEV(n) bit-field to "0".

COMMAND REGISTER CR1-(N)

D4	D3	D2	D1	D0
TxOFF(n)	TAOS(n)	TxClkINV(n)	TxLEV(n)	TxBIN(n)
0	X	X	0	X

2.4.2 Disabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out circuit is disabled, the XRT73L03 outputs partially-shaped pulses onto the line via the TTIP(n) and TRing(n) output pins.

To disable the Transmit Line Build-Out circuit, do the following:

a. Operating in the Hardware Mode

Set the TxLEV(n) input pin to "High".

b. Operating in the HOST Mode

Set the TxLEV(n) bit-field to "1" as illustrated below.

COMMAND REGISTER CR1-(N)

D4	D3	D2	D1	D0
TxOFF(n)	TAOS(n)	TxClkINV(n)	TxLEV(n)	TxBin(n)
0	X	X	1	X

2.4.3 Design Guideline for Setting the Transmit Line Build-Out Circuit

The TxLEV(n) input pins or bit-fields should be set based upon the overall cable length between the Transmitting Terminal and the Digital Cross Connect system where the pulse template measurements are made.

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is less than 225 feet, enable the Transmit Line Build-Out circuit by setting the TxLEV(n) input pin or bit-field to "0".

NOTE: *In this case, the configured channel outputs shaped (e.g., not square-wave) pulses onto the line via its TTIP(n) and TRing(n) output pins. The shape of this output pulse is such that it complies with the pulse template requirements even when subjected to cable loss ranging from 0 to 225 feet.*

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is greater than 225 feet, disable the Transmit Line Build-Out circuit by setting the TxLEV(n) input pin or bit-field to "1".

NOTE: *In this case, the configured channel in the XRT73L03 outputs partially-shaped pulses onto the line via the TTIP(n) and TRing(n) output pins. The cable loss that these pulses experience over long cable lengths (e.g., greater than 225 feet) causes these pulses to be properly shaped and comply with the appropriate pulse template requirement.*

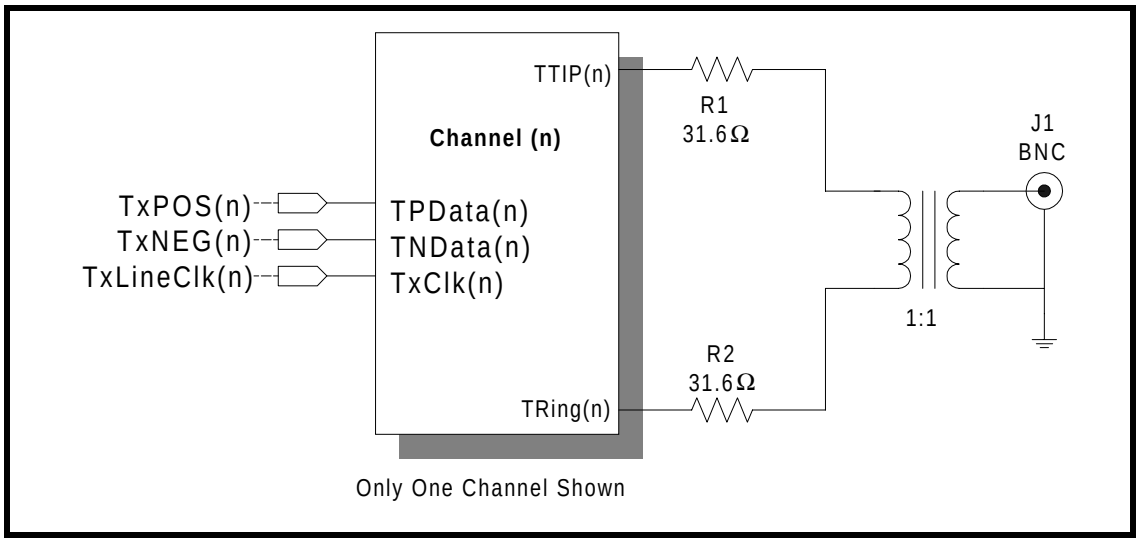
2.4.4 The Transmit Line Build-Out Circuit and E3 Applications

The ITU-T G.703 Pulse Template Requirements for E3 states that the E3 transmit output pulse should be measured at the Secondary Side of the Transmit Output Transformer for Pulse Template compliance. In other words, there is no Digital Cross Connect System pulse template requirement for E3. Consequently, the Transmit Line Build-Out circuit in a given Channel in the XRT73L03 is disabled whenever that channel has been configured to operate in the E3 Mode.

2.5 INTERFACING THE TRANSMIT SECTIONS OF THE XRT73L03 TO THE LINE

The E3, DS3 and SONET STS-1 specification documents all state that line signals transmitted over coaxial cable are to be terminated with 75 Ohm resistor. Interface the Transmit Section of the XRT73L03 in the manner illustrated in Figure 16 to accomplish this.

FIGURE 16. RECOMMENDED SCHEMATIC FOR INTERFACING THE TRANSMIT SECTION OF THE XRT73L03 TO THE LINE



Transformer Recommendations

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	4µH
Isolation Voltage	1500Vrms
Leakage Inductance	0.06µH

PART #	INSULATION	PACKAGE TYPE
PE-68629	3000V	Large Thru-Hole
PE-65966	1500V	Small Thru-Hole
PE-65967	1500V	Small SMT
T3001	1500V	Small SMT

TRANSFORMER VENDOR INFORMATION

Pulse

Corporate Office

12220 World Trade Drive
San Diego, CA 92128
Tel: (619)-674-8100
FAX: (619)-674-8262

Europe

1 & 2 Huxley Road
The Surrey Research Park
Guildford, Surrey GU2 5RE
United Kingdom
Tel: 44-1483-401700
FAX: 44-1483-401701

Asia

150 Kampong Ampat
#07-01/02
KA Centre
Singapore 368324
Tel: 65-287-8998
FAX: 65-280-0080

3.0 THE RECEIVE SECTION

Figure 8 indicates that the Receive Section in the XRT73L03 consists of the following blocks:

- AGC/Equalizer
- Peak Detector
- Slicer
- Clock Recovery PLL
- Data Recovery
- HDB3/B3ZS Decoder

The purpose of each Receive Section of the XRT73L03 is to take an incoming attenuated/distorted bipolar signal from the line and encode it back into the TTL/CMOS format where it can be received and processed by the Terminal Equipment.

3.1 INTERFACING THE RECEIVE SECTIONS OF THE XRT73L03 TO THE LINE

The design of the Receive Circuitry in the XRT73L03 allows for transformer-coupling or capacitive-coupling of the Receive Section to the line. As mentioned earlier, the specification documents for E3, DS3 and STS-1 all specify 75 Ohm termination loads when transmitting over coaxial cable. The recommended method of Transformer-Coupling the Receive Section of the XRT73L03 to the line is shown in Figure 17 and the Capacitive-Coupling method is shown in Figure 18.

FIGURE 17. RECOMMENDED SCHEMATIC FOR TRANSFORMER-COUPLING THE RECEIVE SECTION OF THE XRT73L03 TO THE LINE

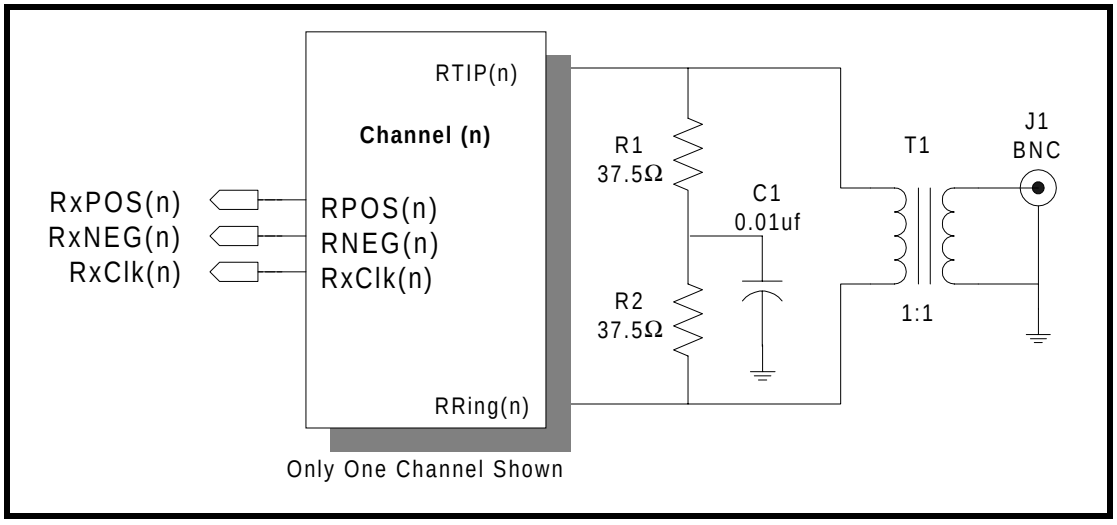
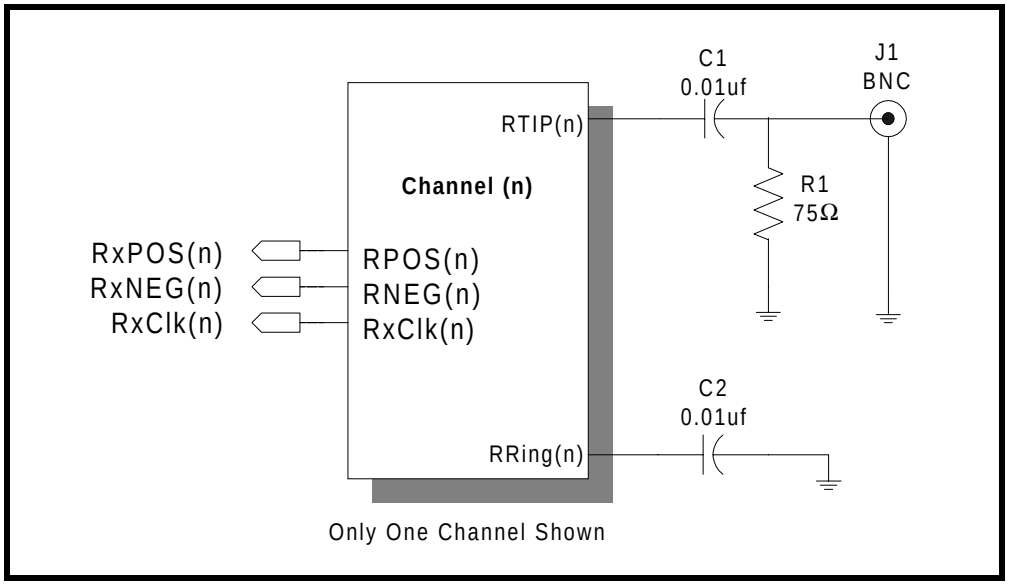


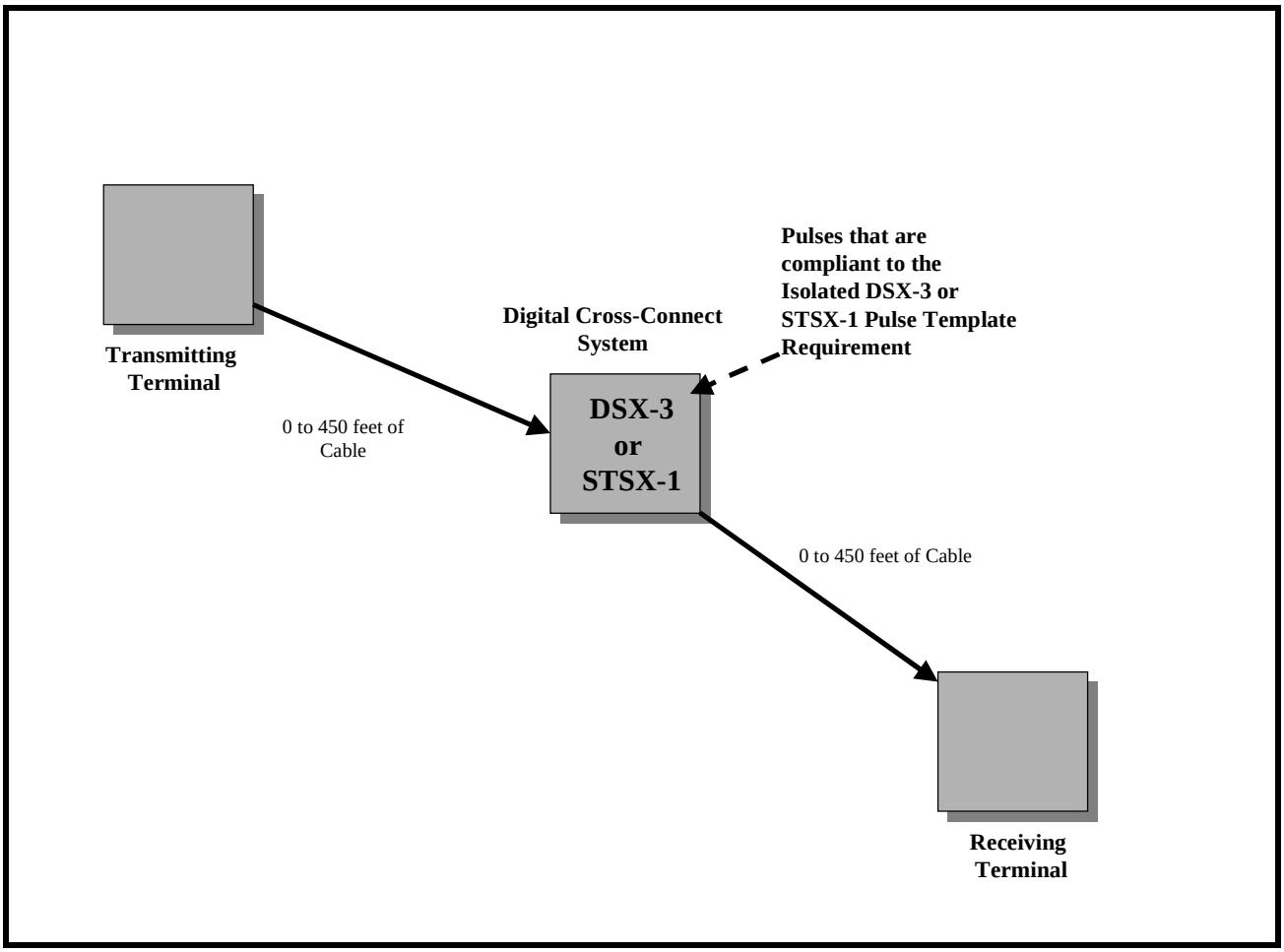
FIGURE 18. RECOMMENDED SCHEMATIC FOR CAPACITIVE-COUPLING THE RECEIVE SECTION OF THE XRT73L03 TO THE LINE



3.2 THE RECEIVE EQUALIZER BLOCK

The purpose of this block is to equalize the incoming distorted signal due to cable loss. The Receive Equalizer attempts to restore the shape of the line signal so that the transmitted data and clock can be recovered reliably.

FIGURE 19. THE TYPICAL APPLICATION FOR THE SYSTEM INSTALLER



- **Design Considerations for DS3 and STS-1 Applications**

When installing equipment into environments depicted in Figure 19, we recommend that the Receive Equalizer be enabled by setting the REQDIS(n) input pin for Channel(n) or the respective bit-fields to "0". The only time that the Receive Equalizer should be disabled is when an off-chip equalizer is in the Receive path between the Digital Cross-Connect system and the RTIP/RRing input pins, or in applications where the Receiver is monitoring the transmit output signal directly.

- **Design Considerations for E3 Applications or if the Overall Cable Length is known**

Figure 19 indicates the following:

a. The length of cable between the Transmitting Terminal and the Digital Cross-Connect system can range between 0 and 450 feet.

b. The length of cable between the Digital Cross-Connect system and the Receive Terminal can range between 0 and 450 feet.

Consequently, the overall cable length between the Transmitting Terminal and the Receiving Terminal can range between very short cable length (e.g., near 0 feet) up to 900 feet.

If during System Installation the overall cable length is known, to optimize the performance of the XRT73L03 in terms of receive jitter performance, etc., enable or disable the Receive Equalizer based upon the following recommendations:

The Receive Equalizer should be turned ON if the Receive Section of a given channel is going to re-

ceive a line signal with an overall cable length of 300 feet or greater. Conversely, turn OFF the Receive Equalizer if the Receive Section of a given channel is going to receive a line signal over a cable length of less than 300 feet.

NOTES:

1. *If the Receive Equalizer block is turned ON when it is receiving a line signal over short cable length the received line signal may be over-equalized, which could degrade performance by increasing the amount of jitter that exists in the recovered data and clock signals or by creating bit-errors.*
2. *The Receive Equalizer has been designed to counter the frequency-dependent cable loss that a line signal experiences as it travels from the transmitting terminal to the receiving terminal. However, the Receive Equalizer was not designed to counter flat loss where all of the Fourier frequency components within the line signal are subject to the same amount of attenuation. Flat loss is handled by the AGC block.*

Disable the Receive Equalizer block by doing either of the following:

a. Operating in the Hardware Mode

Set the REQEN(n) input pin "Low".

b. Operating in the HOST Mode

Write a "0" to the REQEN(n) bit-field in Command Register CR2.

COMMAND REGISTER CR2_(N)

D4	D3	D2	D1	D0
RESERVED	ENDECDIS(n)	ALOSDIS(n)	DLOSDIS(n)	REQEN(n)
X	X	X	X	0

3.3 CLOCK RECOVERY PLL

The purpose of the Clock Recovery PLL is to track the incoming Dual-Rail data stream and to derive and generate a recovered clock signal.

It is important to note that the Clock Recovery PLL requires a line rate clock signal at the ExClk input pin.

The Clock Recovery PLL operates in one of two modes:

- The Training Mode
- The Data/Clock Recovery Mode

3.3.1 The Training Mode

If a given channel in the XRT73L03 is not receiving a line signal via the RTIP and RRing input pins, or if the frequency difference between the line signal and that applied via the ExClk input pin exceeds 0.5%, the channel operates in the Training Mode. When the channel is operating in the Training Mode, it does the following:

a. Declare a Loss of Lock indication by toggling its respective RLOL(n) output pin “High".

b. Output a clock signal via the RxClk(n) output pin which is derived from the signal applied to the EXClk(n) input pin.

3.3.2 The Data/Clock Recovery Mode

If the frequency difference between the line signal and that applied via the ExClk input pin is less than 0.5%, the channel operates in the Data/Clock Recovery mode. In this mode, the Clock Recovery PLL locks onto the line signal via the RTIP and RRing input pins.

3.4 THE HDB3/B3ZS DECODER

The Remote Transmitting Terminal typically encodes the line signal into some sort of Zero Suppression Line Code (e.g., HDB3 for E3 and B3ZS for DS3 and STS-1). The purpose of this encoding activity was to aid in the Clock Recovery process of this data from the Near-End Receiving Terminal. However, once the data has made it across the E3, DS3 or STS-1 Transport Medium and has been recovered by the Clock Recovery PLL, it is now necessary to restore the original content of the data. Hence, the purpose of the HDB3/B3ZS Decoding block is to restore the data transmitted over the E3, DS3 or STS-1 line to its original content prior to Zero Suppression Coding.

3.4.1 B3ZS Decoding DS3/STS-1 Applications

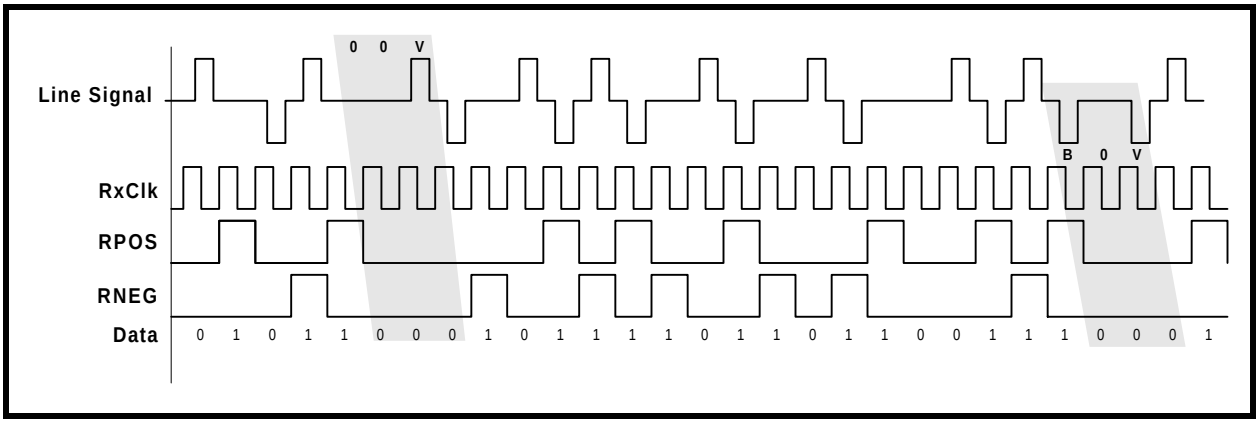
If the XRT73L03 is configured to operate in the DS3 or STS-1 Modes, then the HDB3/B3ZS Decoding Blocks perform B3ZS Decoding. When the Decoders are operating in this mode, each of the Decoders parses through its respective incoming Dual-Rail data and checks for the occurrence of either a "00V" or a "B0V" pattern. If the B3ZS Decoder detects this particular pattern, it substitutes these bits with a "000" pattern.

NOTE: *If the B3ZS Decoder detects any bipolar violations that is not in accordance with theB3ZS Line Code format or if the B3ZS Decoder detects a string of 3 or more consecutive "0's" in the incoming line signal, the B3ZS Decoder*

flags this event as a Line Code Violation by pulsing the LCV output pin "High".

Figure 20 illustrates the B3ZS Decoder at work with two separate Zero Suppression patterns in the incoming Dual-Rail Data Stream.

FIGURE 20. AN EXAMPLE OF B3ZS DECODING

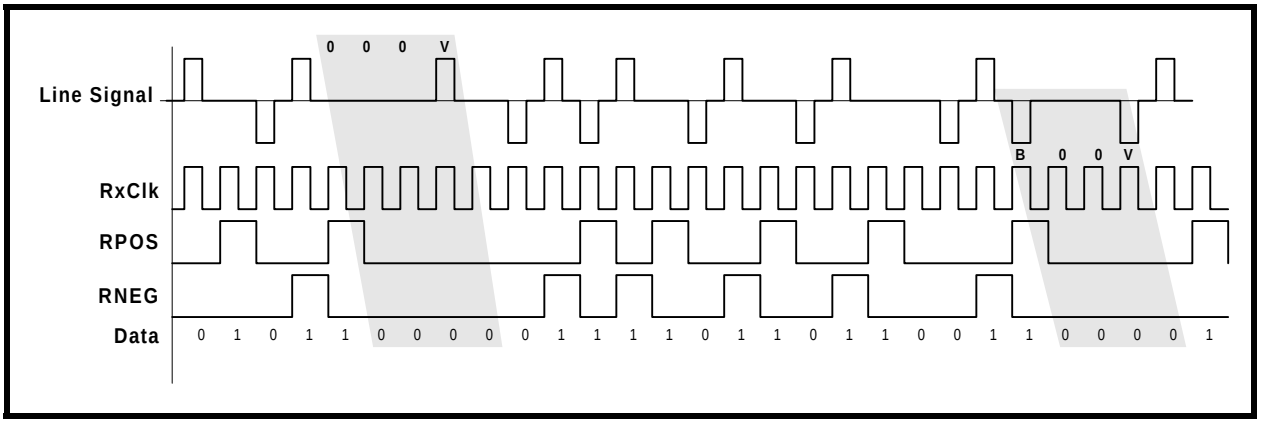


3.4.2 HDB3 Decoding E3 Applications

If the XRT73L03 is configured to operate in the E3 Mode, then each of the HDB3/B3ZS Decoding Blocks performs HDB3 Decoding. When the Decoders are operating in this mode, they each parse through the incoming Dual-Rail data and check for the occurrence of either a "000V" or a "B00V" pattern. If the HDB3 Decoder detects this particular pattern, it substitutes these bits with a "0000" pattern.

Figure 21 illustrates the HDB3 Decoder at work with two separate Zero Suppression patterns in the incoming Dual-Rail Data Stream.

FIGURE 21. AN EXAMPLE OF HDB3 DECODING



NOTE: *If the HDB3 Decoder detects any bipolar violation (e.g., "V") pulses that is not in accordance with the HDB3 Line Code format, or if the HDB3 Decoder detects a string of 4 or more "0's" in the incoming line signal, the HDB3 Decoder flags this event as a Line Code Violation by pulsing the LCV output pin "High".*

3.4.3 Configuring the HDB3/B3ZS Decoder

The XRT73L03 can enable or disable the HDB3/B3ZS Decoder blocks of each Channel by either of the following means.

a. Operating in the HOST Mode

Enable the HDB3/B3ZS Decoder block of Channel(n) by writing a "0" into the ENDECDIS(n) bit-field in Command Register CR2-(n).

COMMAND REGISTER CR2-(N)

D4	D3	D2	D1	D0
Reserved	ENDEC_DIS	ALOSDIS(n)	DLOSDIS(n)	REQEN(n)
X	0	X	X	1

b. Operating in the Hardware Mode

To globally enable all HDB3/B3ZS Decoder blocks in the XRT73L03, pull the ENDEC_DIS input pin “Low". To globally disable all HDB3/B3ZS Decoder blocks in the XRT73L03 and configure the XRT73L03 to transmit and receive in an AMI format, pull the ENDEC_DIS input pin "High".

3.5 LOS Declaration/Clearance

Each channel of the XRT73L03 contains circuitry that monitors the following two parameters associated with the incoming line signals.

1. The amplitude of the incoming line signal via the RTIP and RRing inputs.
2. The number of pulses detected in the incoming line signal within a certain amount of time.

If a given channel of the XRT73L03 determines that the incoming line signal is missing due to either insufficient amplitude or a lack of pulses in the incoming line signal, it declares a Loss of Signal (LOS) condition. The channel declares the LOS condition by toggling its respective RLOS(n) output pin “High” and by setting its corresponding RLOS(n) bit field in Command Register 0 or Command Register 8 to "1".

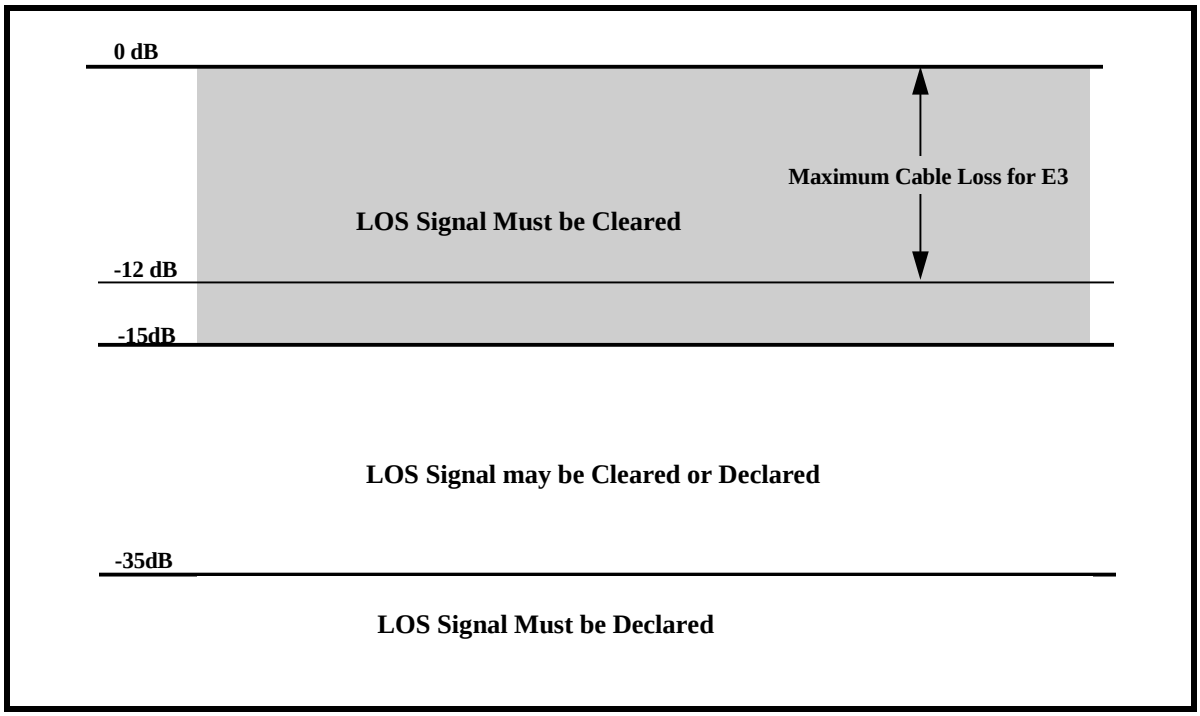
Conversely, if the channel determines that the incoming line signal has been restored (e.g., there is sufficient amplitude and pulses in the incoming line signal), it clears the LOS condition by toggling its respective RLOS(n) output pin "Low" and setting its corresponding RLOS(n) bit-field to "0".

In general, the LOS Declaration/Clearance scheme that is employed in the XRT73L03 is based upon ITU-T Recommendation G.775 for both E3 and DS3 applications.

3.5.1 The LOS Declaration/Clearance Criteria for E3 Applications

When the XRT73L03 is operating in the E3 Mode, a given channel declares an LOS Condition if its receive line signal amplitude drops to -35dB or below. Further, the channel clears the LOS Condition if its receive line signal amplitude rises back to -15dB or above. Figure 22 illustrates the signal levels at which each channel of the XRT73L03 declares and clears LOS.

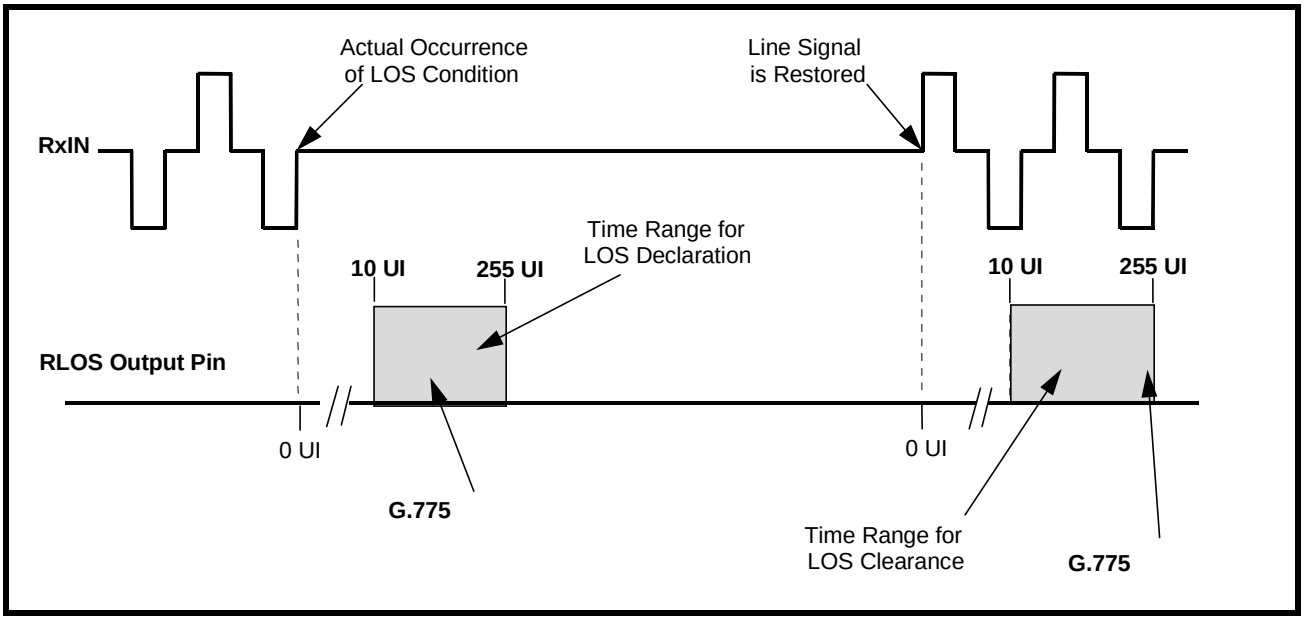
FIGURE 22. THE SIGNAL LEVELS AT WHICH THE XRT73L03 DECLARES AND CLEARS LOS



Timing Requirements associated with Declaring and Clearing the LOS Indicator

The XRT73L03 was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS indicator. In particular, a channel of the XRT73L03 declares an LOS between 10 and 255 UI (or E3 bit-periods) after the actual time the LOS condition occurred. The channel clears the LOS indicator within 10 to 255 UI after restoration of the incoming line signal. Figure 23 illustrates the LOS Declaration and Clearance behavior in response to the Loss of Signal event and then the restoration of the signal.

FIGURE 23. THE BEHAVIOR THE LOS OUTPUT INDICATOR IN RESPONSE TO THE LOSS OF SIGNAL AND THE RESTORATION OF SIGNAL



3.5.2 The LOS Declaration/Clearance Criteria for DS3 and STS-1 Applications

When the XRT73L03 is operating in the DS3 or STS-1 Mode, each channel in the XRT73L03 declares and clears LOS based upon the following two criteria:

- Analog LOS (ALOS) Declaration/Clearance Criteria
- Digital LOS (DLOS) Declaration/Clearance Criteria

In the DS3 Mode, the LOS output (RLOS) is simply the logical "OR" of the ALOS and DLOS states.

1. The Analog LOS (ALOS) Declaration/Clearance Criteria

A channel in the XRT73L03 declares an Analog LOS (ALOS(n)) Condition if the amplitude of the incoming line signal drops below a specific amplitude as defined by the voltage at the LOSTHR input pin and whether the Receive Equalizer is enabled or not.

Table 5 presents the various voltage levels at the LOSTHR input pin, the state of the Receive Equalizer, and the corresponding ALOS (Analog LOS) threshold amplitudes.

TABLE 5: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN FOR DS3 AND STS-1 APPLICATIONS

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS	SIGNAL LEVEL TO CLEAR ALOS
DS3	1	0	≤55mV	≥220mV
	1	1	≤22mV	≥90mV
	0	0	≤35mV	≥155mV
	0	1	≤17mV	≥70mV
STS-1	1	0	≤75mV	≥270mV
	1	1	≤25mV	≥115mV
	0	0	≤55mV	≥210mV
	0	1	≤20mV	≥90mV

Declaring ALOS

A Channel(n) in the XRT73L03 declares ALOS(n) whenever the amplitude of the receive line signal falls below the signal levels to declare ALOS, as specified in Table 5.

Clearing ALOS(n)

A Channel(n) clears ALOS(n) whenever the amplitude of the receive line signal increases above the signal levels to declare ALOS, as specified in Table 5.

There is approximately a 2dB hysteresis in the received signal level that exists between declaring and clearing ALOS(n) in order to prevent chattering in the RLOS(n) output signal.

Monitoring the State of ALOS(n)

If the XRT73L03 is operating in the HOST Mode, the state of ALOS(n) of Channel(n) can be polled or monitored by reading in the contents of Command Register CR0.

COMMAND REGISTER CR0-(N)

D4	D3	D2	D1	D0
RLOL(n)	RLOS(n)	ALOS(n)	DLOS(n)	DMO(n)
Read Only	Read Only	Read Only	Read Only	Read Only

If the ALOS(n) bit-field contains a "1", then the corresponding Channel(n) is currently declaring an ALOS condition. Conversely, if the ALOS(n) bit-field contains a "0", then the channel is not currently declaring an ALOS condition.

Disabling the ALOS Detector

For debugging purposes it may be useful to disable the ALOS Detector in the XRT73L03. If the XRT73L03 is operating in the HOST Mode the ALOS Detector can be disabled by writing a "1" into the ALOSDIS(n) bit-field in Command Register CR2.

COMMAND REGISTER CR2-(N)

D4	D3	D2	D1	D0
Reserved	ENDECDIS(n)	ALOSDIS(n)	DLOSDIS(n)	REQEN(n)
X	X	1	X	X

2. The Digital LOS (DLOS) Declaration/Clearance Criteria

A given Channel(n) in the XRT73L03 declares a Digital LOS (DLOS(n)) condition if the XRT73L03 detects 160±32 or more consecutive "0's" in the incoming data.

The channel clears DLOS if it detects four consecutive sets of 32 bit-periods, each of which contains at least 10 "1's" (e.g., average pulse density of greater than 33%).

Monitoring the State of DLOS

If the XRT73L03 is operating in the HOST Mode the state of DLOS(n) of Channel(n) can be polled or monitored by reading in the contents of Command Register CR0.

COMMAND REGISTER CR0-(N)

D4	D3	D2	D1	D0
RLOL(n)	RLOS(n)	ALOS(n)	DLOS(n)	DMO(n)
Read Only	Read Only	Read Only	Read Only	Read Only

If the DLOS(n) bit-field contains a “1”, then the corresponding Channel(n) is currently declaring a DLOS condition. If the DLOS(n) bit-field contains a “0”, the Channel(n) is currently declaring the DLOS condition.

Disabling the DLOS Detector

For debugging purposes, it is useful to be able to disable the DLOS(n) detector in the XRT73L03. If the XRT73L03 is operating in the HOST Mode the DLOS Detector can be disabled by writing a “1” into the DLOSDIS(n) bit-field of Command Register CR2.

COMMAND REGISTER CR2-(N)

D4	D3	D2	D1	D0
Reserved	ENDECDIS(n)	ALOSDIS(n)	DLOSDIS(n)	REQEN(n)
X	X	X	1	X

NOTE: *Setting both the ALOSDIS(n) and DLOSDIS(n) bit-fields to "1" disables LOS Declaration by Channel(n).*

3.5.3 Muting the Recovered Data while the LOS is being Declared

In some applications it is not desirable for a channel of the XRT73L03 to recover data and route it to the Receiving Terminal while the channel is declaring an LOS condition. Consequently, the XRT73L03 includes an LOS Muting feature. This feature if enabled causes a given channel to halt transmission of the recovered data to the Receiving Terminal while the LOS condition is "true". In this case, the RPOS(n) and RNEG(n) output pins are forced to "0". Once the LOS condition has been cleared, the channel resumes normal transmission of the recovered data to the Receiving Terminal.

This feature is available whenever the XRT73L03 is operating in the HOST or Hardware Mode.

a. Operating in the Hardware Mode.

To enable the MUTing upon LOS feature for all channels of the XRT73L03, pull the LOSMUTEN output pin (pin 78) "High".

b. Operating in the HOST Mode.

The MUTing upon LOS feature for each Channel can be enabled by writing a "1" into the LOSMUT(n) bit-field in Command Register 3.

COMMAND REGISTER CR3-(N)

D4	D3	D2	D1	D0
SR/($\overline{DR}$)_(n)	LOSMUT(n)	RxOFF(n)	RxClk(n)INV	Reserved
X	1x	x	x	x

NOTE: *This step only enables the MUTing upon LOS feature in Channel(n).*

3.6 ROUTING THE RECOVERED TIMING AND DATA INFORMATION TO THE RECEIVING TERMINAL EQUIPMENT

Each channel in the XRT73L03 takes the Recovered Timing and Data information, converts it into CMOS levels and routes it to the Receiving Terminal Equipment via the RPOS(n), RNEG(n) and RxClk(n) output pins.

Each channel of the XRT73L03 can deliver the recovered data and clock information to the Receiving Terminal in either a Single-Rail or Dual-Rail format.

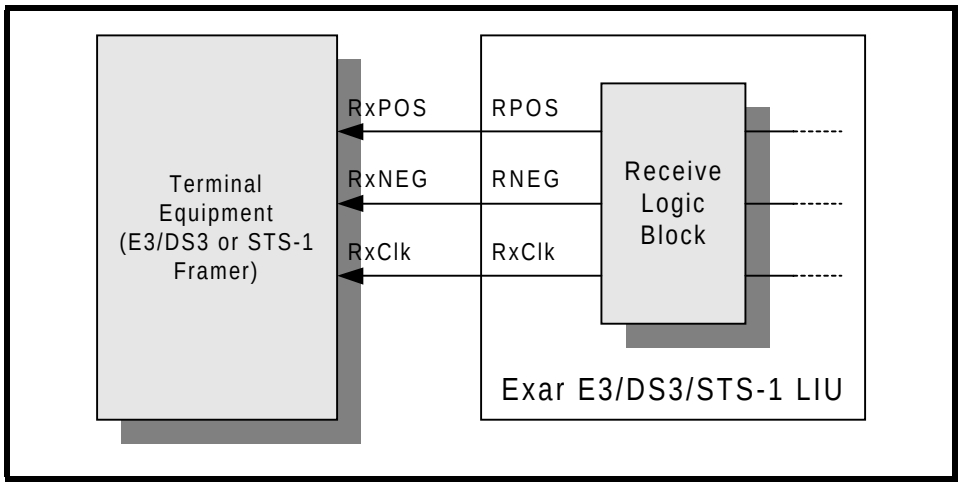
3.6.1 Routing Dual-Rail Format Data to the Receiving Terminal Equipment

Whenever a channel of the XRT73L03 delivers Dual-Rail format to the Terminal Equipment, it does so via the following signals:

- RPOS(n)
- RNEG(n)
- RxClk(n)

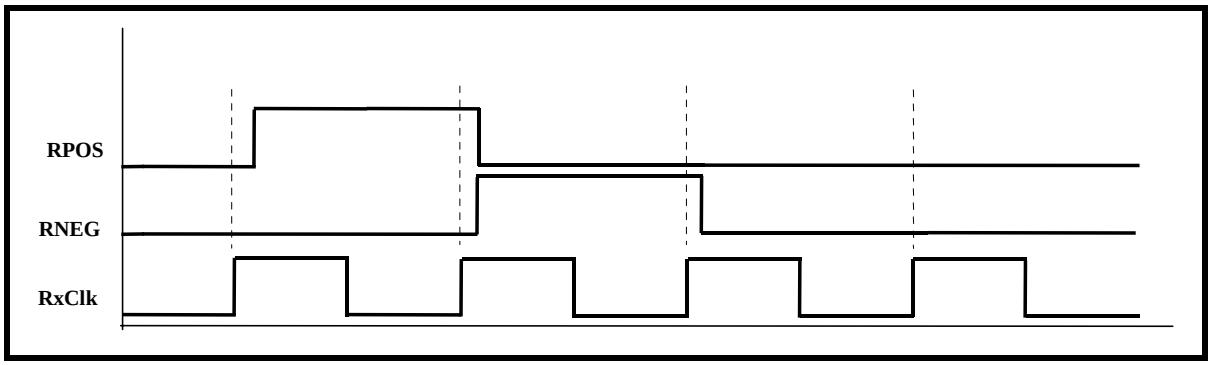
Figure 24 illustrates the typical interface for the transmission of data in a Dual-Rail Format from the Receive Section of a channel to the Receiving Terminal Equipment

FIGURE 24. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT FROM THE RECEIVE SECTION OF THE XRT73L03 TO THE RECEIVING TERMINAL EQUIPMENT



The manner that a given channel transmits Dual-Rail data to the Receiving Terminal Equipment is described below and illustrated in Figure 25. Each Channel(n) of the XRT73L03 typically updates the data on the RPOS(n) and RNEG(n) output pins on the rising edge of RxClk(n).

FIGURE 25. HOW THE XRT73L03 OUTPUTS DATA ON THE RPOS AND RNEG OUTPUT PINS



RxClk(n) is the Recovered Clock signal from the incoming Received line signal. As a result, these clock signals are typically 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications and 51.84 MHz for SONET STS-1 applications.

In general, if a given channel received a positive-polarity pulse in the incoming line signal via the RTIP(n) and RRing(n) input pins, then the channel pulses its corresponding RPOS(n) output pin "High". Conversely, if the channel received a negative-polarity pulse in the incoming line signal via the RTIP(n) and RRing(n) input pins, then the Channel(n) pulses its corresponding RNEG(n) output pin "High".

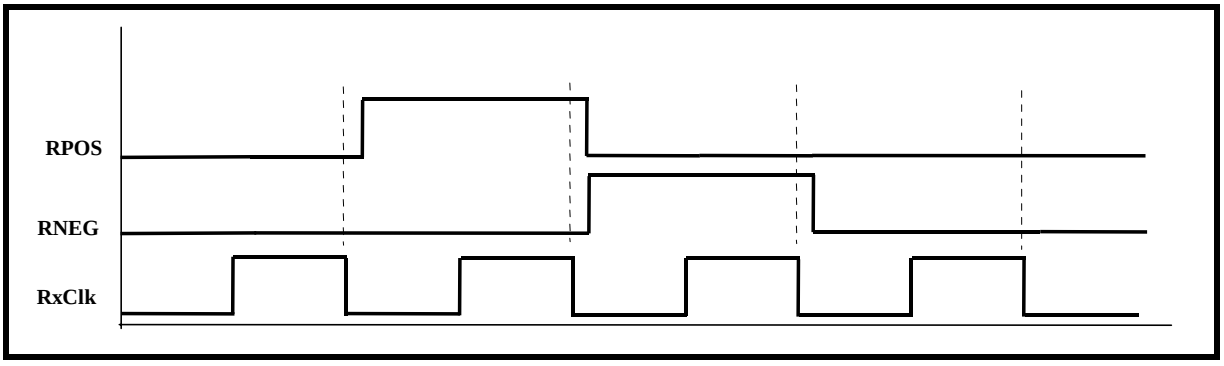
Inverting the RxClk(n) outputs

Each channel can invert the RxClk(n) signals with respect to the delivery of the RPOS(n) and RNEG(n) output data to the Receiving Terminal Equipment. This feature may be useful for those customers whose Receiving Terminal Equipment is designed such that the RPOS(n) and RNEG(n) data must be sampled on the rising edge of RxClk(n). Figure 26 illustrates the behavior of the RPOS(n), RNEG(n) and RxClk(n) signals when the RxClk(n) signal has been inverted.

a. Operating in the Hardware Mode

Setting the RxClkINV pin (pin 62) “High” results in all channels of the XRT73L03 to output the recovered data on RPOS(n) and RNEG(n) on the falling edge of RxClk(n). Setting this pin “Low” results in the recovered data on RPOS(n) and RNEG(n) to output on the rising edge of RxClk(n).

FIGURE 26. THE BEHAVIOR OF THE RPOS, RNEG AND RXCLK SIGNALS WHEN RXCLK IS INVERTED



b. Operating in the HOST Mode

In order to configure a channel of the XRT73L03 to invert the RxClk(n) output signal, the XRT73L03 must be operating in the HOST Mode.

To invert RxClk(n) associated with Channel(n), write a "1" into the RxClk(n)INV bit-field in Command Register CR-3 as illustrated below.

COMMAND REGISTER CR3-(N)

D4	D3	D2	D1	D0
SR/(DR)_(n)	LOSMUT(n)	RxOFF(n)	RxClk(n)INV	Reserved
X	X	X	1	X

Inverting the RxClk(n) signals via the Hardware Mode

Setting the RxClkINV input pin (pin 62) “High" inverts all the RxClk(n) output signals.

3.6.2 Routing Single-Rail Format (Binary Data Stream) data to the Receive Terminal Equipment

a. Operating in the HOST Mode

Configure Channel(n) to output Single-Rail data to the Terminal Equipment by writing a "1" into the SR/(DR)_(n) bit-field of Command Register CR3-(n).

COMMAND REGISTER CR3-(N)

D4	D3	D2	D1	D0
SR/(DR)_(n)	LOSMUT(n)	RxOFF(n)	RxClk(n)INV	Reserved
1	X	X	X	X

The configured channel outputs Single-Rail data to the Receiving Terminal Equipment via its corresponding RPOS(n) and RxClk(n) output pins as illustrated in Figure 27 and Figure 28.

b. Operating in the Hardware Mode

Configure the XRT73L03 to output Single-Rail data from the Receive Sections of all channels by pulling the SR/(DR) pin (pin 57) to VDD.

NOTE: *When the XRT73L03 is operating in the Hardware Mode, the setting of the SR/(DR) input pin applies globally to all three channels.*

FIGURE 27. THE TYPICAL INTERFACE FOR DATA TRANSMISSION IN A SINGLE-RAIL FORMAT FROM THE RECEIVE SECTION OF THE XRT73L03 TO THE RECEIVING TERMINAL EQUIPMENT

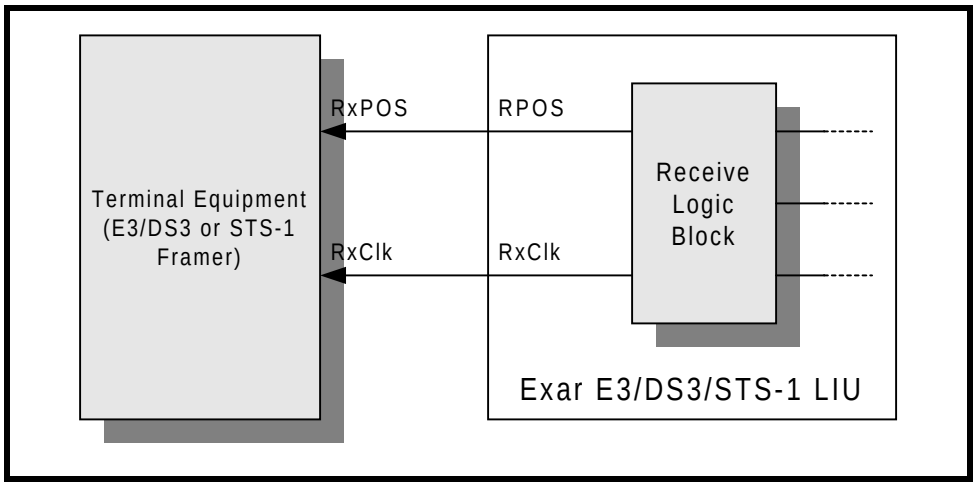
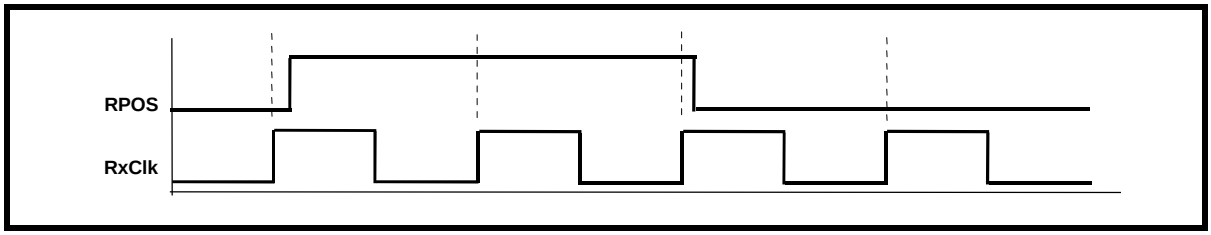


FIGURE 28. THE BEHAVIOR OF THE RPOS AND RXCLK OUTPUT SIGNALS WHILE THE XRT73L03 IS TRANSMITTING SINGLE-RAIL DATA TO THE RECEIVING TERMINAL EQUIPMENT



NOTE: The RNEG(n) output pin is internally tied to Ground whenever this feature is implemented.

3.7 SHUTTING OFF THE RECEIVE SECTION

The Receiver Section in each channel of the XRT73L03 can be shut off. This feature may be useful in some redundant system designs. Particularly, in those designs where the Receive Termination in the Secondary LIU Line Card has been switched-out and is not receiving any traffic in parallel with the Primary Line Card. In this case, it is a waste of power if the LIU on the Secondary Line Card is consuming the normal amount of current. This feature can permit powering down the Receive Section of the LIU's on the Secondary Line Card which reduces their power consumption by approximately 80%.

a. Operating in the Hardware Mode

Shut off the Receive Section of Channel(n) by pulling the RxOFF(n) input pin (pin 15, 19 or 70 respectively) "High". Turn on the Receive Section of Channel(n) by pulling the RxOFF(n) input pin to "Low".

b. Operating in the HOST Mode

Shut off the Receive Section of Channel(n) by writing a "1" into the RxOFF(n) bit-field in Command Register CR3-(n). Turn on the Receive Section of Channel(n) by writing a "0" into the RxOFF(n) bit-field in Command Register CR3-(n).

COMMAND REGISTER CR3-(N)

D4	D3	D2	D1	D0
SR/($\overline{DR}$)_(n)	LOSMUT(n)	RxOFF(n)	RxClk(n)INV	Reserved
X	X	1	X	X

4.0 DIAGNOSTIC FEATURES OF THE XRT73L03

The XRT73L03 supports equipment diagnostic activities by supporting the following Loop-Back modes in each channel in the XRT73L03:

- Analog Local Loop-Back.
- Digital Local Loop-Back
- Remote Loop-Back

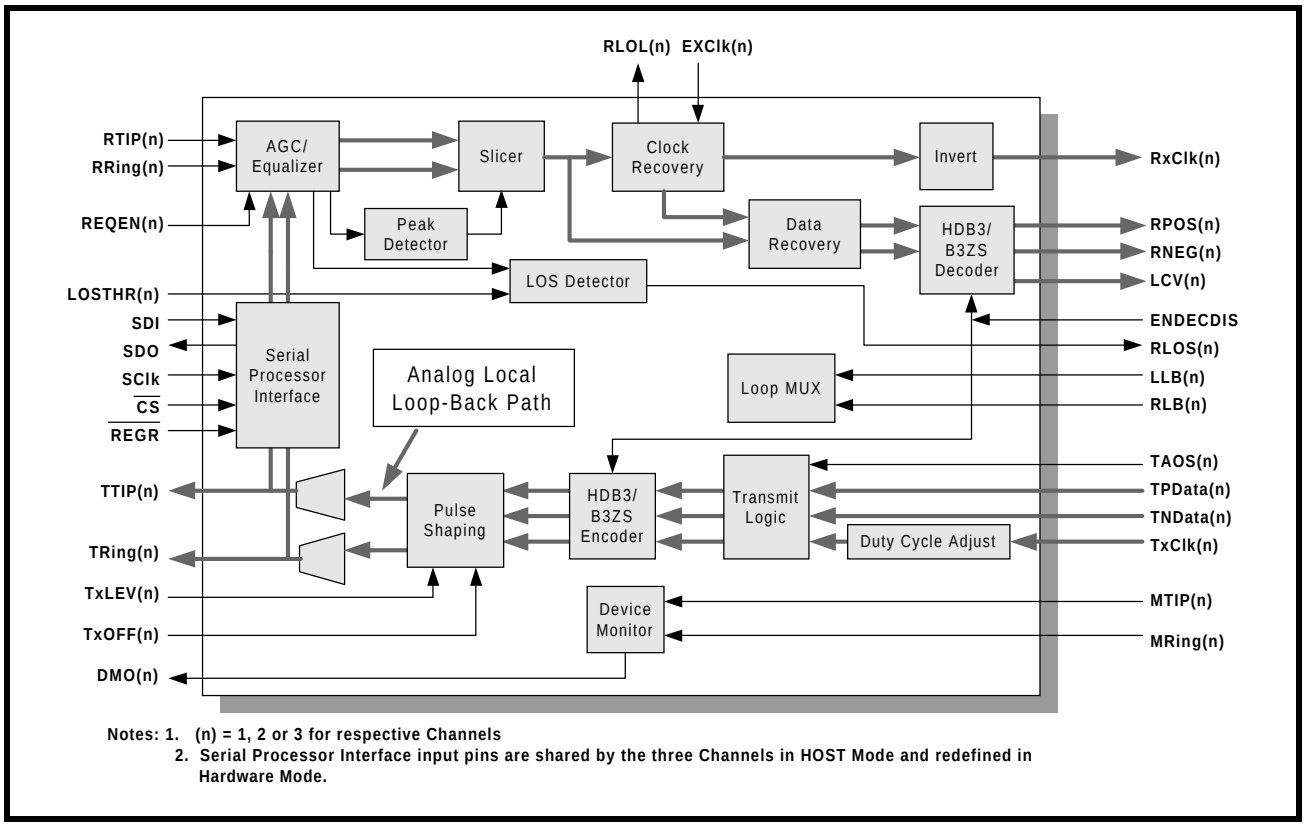
NOTE: *In this data sheet we use the convention that Channel(n) refers to either channel 1, 2 or 3. Similarly, specific input and output pins use this convention to denote which channel it is associated with.*

4.1 THE ANALOG LOCAL LOOP-BACK MODE

When a given channel in the XRT73L03 is configured to operate in the Analog Local Loop-Back Mode, it ignores any signals that are input to its RTIP(n) and RRing(n) input pins. The Transmitting Terminal Equipment transmits clock and data into this channel via the TPData(n), TNData(n) and TxClk(n) input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder. Finally, this data outputs to the line via the TTIP(n) and TRing(n) output pins. Additionally, this data loops back into the Attenuator/Receive Equalizer Block. Consequently, this data is processed through the entire Receive Section of the channel. After this post-Loop-Back data has been processed through the Receive Section it outputs to the Near-End Receiving Terminal Equipment via the RPOS(n), RNEG(n) and RxClk(n) output pins.

Figure 29 illustrates the path the data takes in a given channel of the XRT73L03 when it is configured to operate in the Analog Local Loop-Back Mode.

FIGURE 29. A CHANNEL IN THE XRT73L03 OPERATING IN THE ANALOG LOCAL LOOP-BACK MODE



Notes: 1. (n) = 1, 2 or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the three Channels in HOST Mode and redefined in Hardware Mode.

A given channel in the XRT73L03 can be configured to operate in the Analog Local Loop-Back Mode by employing either one of the following two steps:

NOTE: *See Table 2 for a description of Command Registers and Addresses for the different channels.*

a. Operating in the HOST Mode

To configure Channel (n) to operate in the Analog Local Loop-Back Mode, write a "1" into the LLB(n) bit-field and a "0" into the RLB(n) bit-field in Command Register CR4.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{\text{DS3}}$_ Ch(n)	E3_ Ch(n)	LLB(n)	RLB(n)
X	X	X	1	0

b. Operating in the Hardware Mode

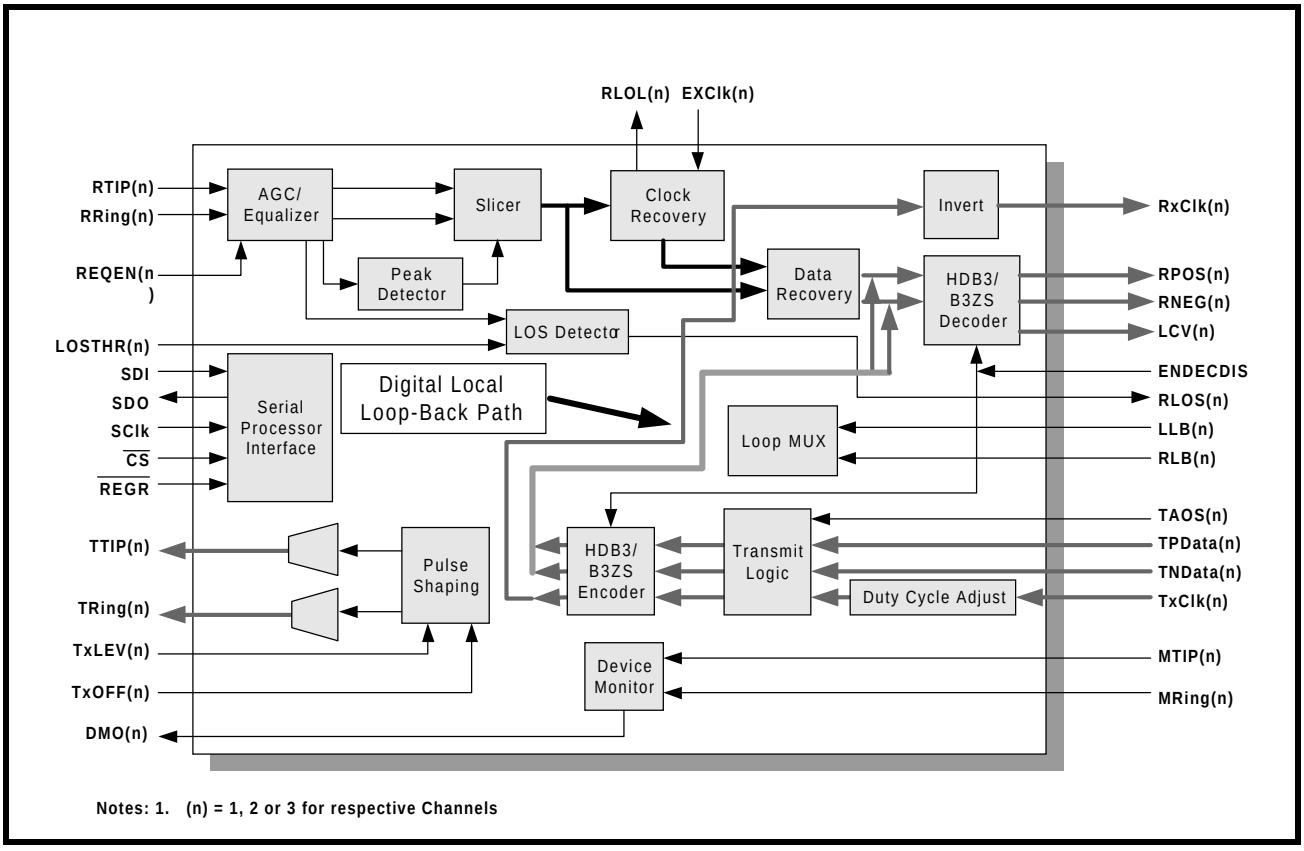
To configure Channel (n) to operate in the Analog Local Loop-Back Mode, set the LLB(n) input pin (pin 34, 54 or 42) “High" and the RLB(n) input pin (pin 35, 53 or 43) “Low".

4.2 The Digital Local Loop-Back Mode.

When a given channel in the XRT73L03 is configured to operate in the Digital Local Loop-Back Mode, the channel ignores any signals that are input to the RTIP and RRing input pins. The Transmitting Terminal Equipment transmits clock and data into the XRT73L03 via the TPData, TNData and TxClk input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder block. At this point, this data loops back to the HDB3/B3ZS Decoder block. After this post-Loop-Back data has been processed through the HDB3/B3ZS Decoder block, it outputs to the Near-End Receiving Terminal Equipment via the RPOS, RNEG and RxClk output pins.

Figure 30 illustrates the path the data takes in the XRT73L03 when the chip is configured to operate in the Digital Local Loop-Back Mode.

Figure 30. The Digital Local Loop-Back path in a given channel of the XRT73L03



Notes: 1. (n) = 1, 2 or 3 for respective Channels

To configure a channel to operate in the Digital Local Loop-Back Mode, employ either one of the following two-steps:

a. Operating in the HOST Mode

To configure Channel (n), write a “1" into both the LLB and RLB bit-fields in Command Register CR4-(n), as illustrated below.

COMMAND REGISTER CR4-(N)

D4	D3	D2	D1	D0
X	STS-1/$\overline{\text{DS3}}$_Ch(n)	E3_Ch(n)	LLB(n)	RLB(n)
X	X	X	1	1

b. Operating in the Hardware Mode

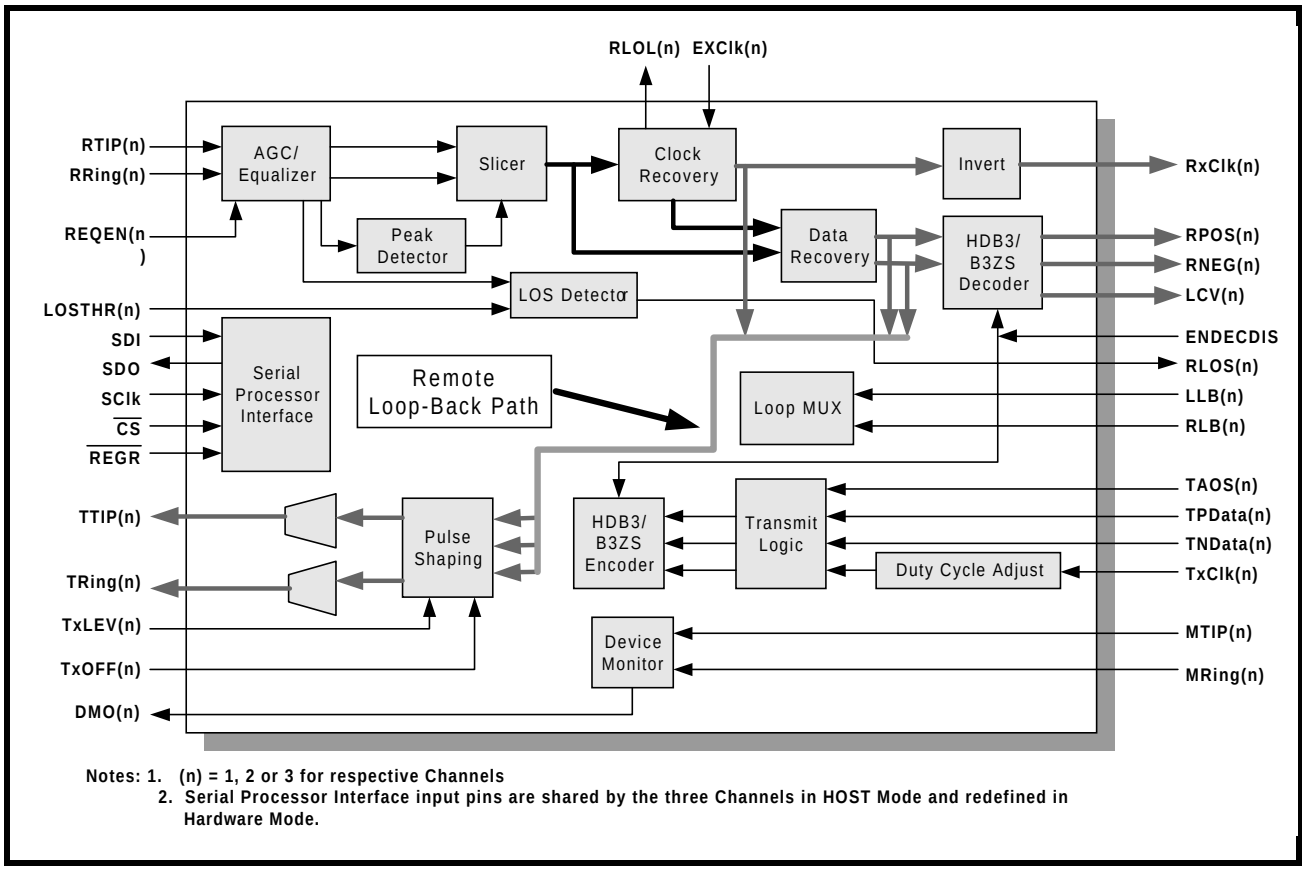
To configure Channel (n), pull both the LLB input pin (pin 34, 54 or 42) and the RLB input pin (pin 35, 53 or 43) “High".

4.3 THE REMOTE LOOP-BACK MODE

When a given channel of the XRT73L03 is configured to operate in the Remote Loop-Back Mode, the channel ignores any signals that are input to the TPData and TNData input pins. The channel receives the incoming line signal via the RTIP and RRing input pins. This data is processed through the entire Receive Section of the channel and outputs to the Receive Terminal Equipment via the RPOS, RNEG and RxClk output pins. Additionally, this data is internally looped back into the Pulse-Shaping block in the Transmit Section. At this point, this data is routed through the remainder of the Transmit Section of the channel and transmitted out onto the line via the TTIP(n) and TRing(n) output pins.

Figure 31 illustrates the path the data takes in the XRT73L03 when the chip is configured to operate in the Remote Loop-Back Mode.

FIGURE 31. THE REMOTE LOOP-BACK PATH IN A GIVEN XRT73L03 CHANNEL



Notes: 1. (n) = 1, 2 or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the three Channels in HOST Mode and redefined in Hardware Mode.

To configure a channel to operate in the Remote Loop-Back Mode employ either one of the following two steps

a. Operating in the HOST Mode

To configure Channel (n), write a "1" into the RLB bit-field and a "0" into the LLB bit-field in Command Register CR4.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_Ch(n)	E3_Ch(n)	LLB(n)	RLB(n)
X	X	X	0	1

b. Operating in the Hardware Mode

To configure Channel(n), pull both the RLB input pin (pin 35, 53 or 43) to “High" and the LLB input pin (pin 34, 54 or 42) to "Low".

4.4 TxOFF FEATURES

The Transmit Section of each Channel in the XRT73L03 can be shut off. When this feature is invoked, the Transmit Section of the configured channel is shut-off and the Transmit Output signals TTIP(n) and TRing(n) are tri-stated. This feature is useful for system redundancy conditions or during diagnostic testing.

a. Operating in the Hardware Mode

Shut off the Channel(n) Transmit Driver by toggling the TxOFF(n) input pin (pin 88, 87 or 86) "High". Turn on the Transmit Driver by toggling the TxOFF(n) input pin "Low".

b. Operating in the HOST Mode

Turn off the Channel(n) Transmit Driver by setting the TxOFF(n) bit-field in Command Register CR1-(n) to "1".

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF(n)	TAOS(n)	TxClkINV(n)	TxLEV(n)	TxBIN(n)
1	X	X	X	X

Writing a "0" into this bit-field enables the Channel(n) Transmit Driver.

NOTE: *In order to permit a system designed for redundancy to quickly shut-off a defective line card and turn-on the back-up line card, the XRT73L03 was designed such that either Transmitter can quickly be turned-on or turned-off by toggling the TxOFF(n) input pins. This approach is much quicker then setting the TxOFF(n) bit-fields via the Microprocessor Serial Interface.*

Table 6 presents a Truth Table which relates the setting of the TxOFF external pin and bit-field for a channel to the state of the Transmitter. This table applies to all Channels of the XRT73L03.

TABLE 6: THE RELATIONSHIP BETWEEN THE TXOFF INPUT PIN, THE TXOFF BIT FIELD AND THE STATE OF THE TRANSMITTER

STATE OF THE TXOFF INPUT PIN	STATE OF THE TXOFF BIT FIELD	STATE OF THE TRANSMITTER
LOW	0	ON (Transmitter is Active)
LOW	1	OFF (Transmitter is Tri-Stated)
HIGH	0	OFF (Transmitter is Tri-Stated)
HIGH	1	OFF (Transmitter is Tri-Stated)

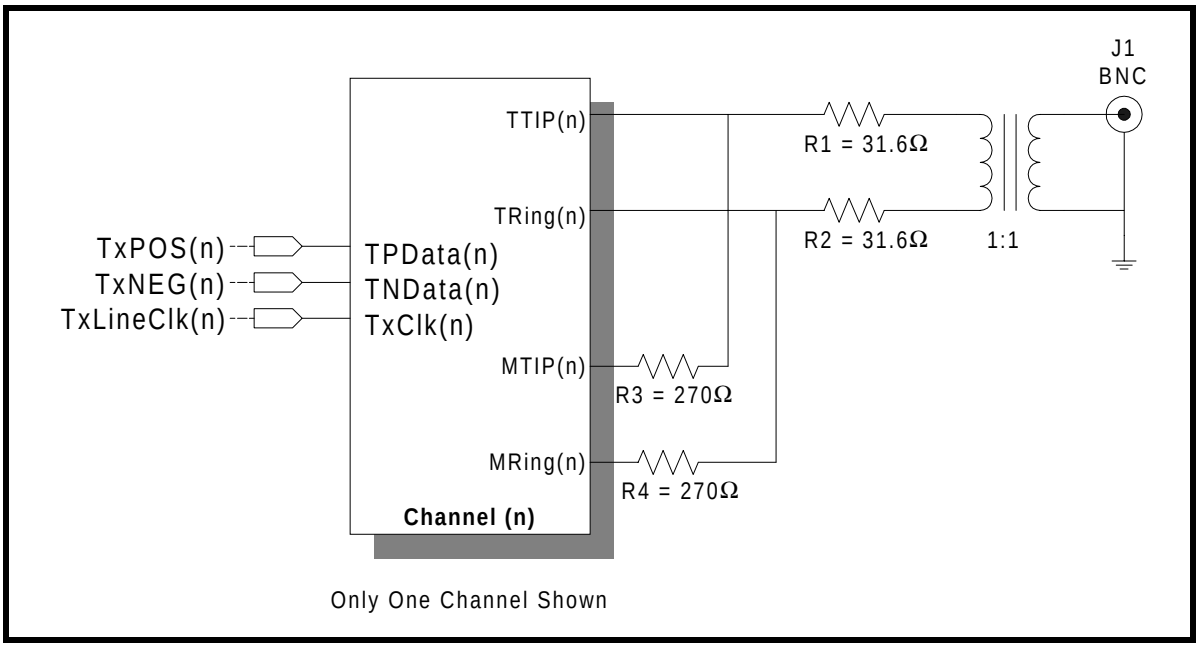
To control the state of each transmitter via the Microprocessor Serial interface, connect the TxOFF(n) input pins to GND.

4.5 THE TRANSMIT DRIVE MONITOR FEATURES

The Transmit Drive Monitor is used to monitor the line in the Transmit Direction for the occurrence of fault conditions such as a short circuit on the line, a defective Transmit Drive in the XRT73L03 or another LIU.

Activate the Channel(n) Transmit Drive Monitor by connecting the MTIP(n) pin (pin 117, 94 or 105) to the TTIP(n) line through a 270 Ohm resistor connected in series, and connecting the MRing(n) pin (pin 116, 95 or 104) to the TRing(n) line through a 270 Ohm resistor connected in series. Such an approach is illustrated in Figure 32.

FIGURE 32. THE XRT73L03 EMPLOYING THE TRANSMIT DRIVE MONITOR FEATURES



When the Transmit Drive Monitor circuitry in a given line is connected to the line as illustrated in Figure 32, then it monitors the line for transitions. As long as the Transmit Drive Monitor circuitry detects transitions on the line via the MTIP(n) and MRing(n) pins, it keeps the DMO (Drive Monitor Output) signal "Low". However, if the Transmit Drive Monitor circuit detects no transitions on the line for 128±32 TxClk periods, the DMO (Drive Monitor Output) signal toggles "High".

NOTE: *The Transmit Drive Monitor circuit does not have to be used to operate the Transmit Section of the XRT73L03. This is purely a diagnostic feature.*

4.6 THE TAOS (TRANSMIT ALL ONES) FEATURE

The XRT73L03 can command any channel to transmit an all “1’s” pattern onto the line by toggling a single input pin or by setting a single bit-field in one of the Command Registers to "1".

NOTE: *When this feature is activated, the Transmit Section of the configured channel in the XRT73L03 overwrites the Terminal Equipment data with an all “1’s” pattern.*

a. Operating in the Hardware Mode

Configure Channel(n) to transmit an all “1’s” pattern by toggling the TAOS(n) input pin (pin 2, 85 or 84) “High". Terminate the all “1’s” pattern by toggling the TAOS(n) input pin "Low".

b. Operating in the HOST Mode

Configure Channel(n) to transmit an all “1’s” pattern by writing to Command Register CR1-(n) and setting the TAOS(n) bit-field (bit D3) to "1".

COMMAND REGISTER CR1-(N)

D4	D3	D2	D1	D0
TxOFF(n)	TAOS(n)	TxClkINV(n)	TxLEV(n)	TxBIN(n)
0	1	X	X	X

Terminate the all “1’s” pattern by writing to Command Register CR1-(n) and setting the TAOS(n) bit-field (D3) to "0".

5.0 THE MICROPROCESSOR SERIAL INTERFACE

The on-chip Command Registers of XRT73L03 DS3/E3/STS-1 Line Interface Unit IC are used to configure the XRT73L03 into a wide-variety of modes. This section discusses the following:

1. The description of the Command Registers.
2. A description on how to use the Microprocessor Serial Interface.

5.1 DESCRIPTION OF THE COMMAND REGISTERS

Table 2 lists the Command Registers, their Addresses and their bit-formats.

TABLE 7: ADDRESSES AND BIT FORMATS OF XRT73L03 COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	TYPE	D4	D3	D2	D1	D0
CHANNEL 1							
0x00	CR0-1	RO	RLOL1	RLOS1	ALOS1	DLOS1	DMO1
0x01	CR1-1	R/W	TxOFF1	TAOS1	TxClkINV1	TxLEV1	TxBIN1
0x02	CR2-1	R/W	Reserved	ENDECDIS1	ALOSDIS1	DLOSDIS1	REQEN1
0x03	CR3-1	R/W	SR/$\overline{\text{DR}}$_1	LOSMUT1	RxOFF1	RxClk1INV	Reserved
0x04	CR4-1	R/W	Reserved	STS-1/$\overline{\text{DS3}}$ Channel 1	E3_CH1	LLB1	RLB1
0x05	CR5-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL 2							
0x08	CR0-2	RO	RLOL2	RLOS2	ALOS2	DLOS2	DMO2
0x09	CR1-2	R/W	TxOFF2	TAOS2	TxClkINV2	TxLEV2	TxBIN2
0x0A	CR2-2	R/W	Reserved	ENDECDIS2	ALOSDIS2	DLOSDIS2	REQEN2
0x0B	CR3-2	R/W	SR/$\overline{\text{DR}}$_2	LOSMUT2	RxOFF2	RxClk2INV	Reserved
0x0C	CR4-2	R/W	Reserved	STS-1/$\overline{\text{DS3}}$ Channel 2	E3_CH2	LLB2	RLB2
0x0D	CR5-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0E	CR6-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0F	CR7-2	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL 3							
0x10	CR0-3	RO	RLOL3	RLOS3	ALOS3	DLOS3	DMO3
0x11	CR1-3	R/W	TxOFF3	TAOS3	TxClkINV3	TxLEV3	TxBIN3
0x12	CR2-3	R/W	Reserved	ENDECDIS3	ALOSDIS3	DLOSDIS3	REQEN3
0x13	CR3-3	R/W	SR/$\overline{\text{DR}}$_3	LOSMUT3	RxOFF3	RxClk3INV	Reserved
0x14	CR4-3	R/W	Reserved	STS-1/$\overline{\text{DS3}}$ Channel 3	E3_CH3	LLB3	RLB3
0x15	CR5-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x16	CR6-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x17	CR7-3	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Address

The register addresses are presented in the **Hexadecimal** format.

Type:

The Command Registers are either Read-Only (RO) or Read/Write (R/W) registers. Each channel of the XRT73L03 has eight command registers, CR0-(n) through CR7-(n) where (n) = 1, 2 or 3. The associated addresses for each channel is presented in Table 2.

NOTE: *The default value for each of the bit-fields in these registers is "0".*

5.2 DESCRIPTION OF BIT-FIELDS FOR EACH COMMAND REGISTER

5.2.1 Command Register - CR0-(n)

The bit-format and default values for Command Register CR0-(n) are listed below followed by the function of these bit-fields.

COMMAND REGISTER CR0-(N)

D4	D3	D2	D1	D0
RLOL	RLOS	ALOS	DLOS	DMO
1	1	1	1	1

Bit D4 - RLOL1 (Receive Loss of Lock Status - Channel(n))

This Read-Only bit-field reflects the lock status of the Channel(n) Clock Recovery Phase-Locked-Loop in the XRT73L03.

This bit-field is set to “0" if the Clock Recovery PLL is in lock with the incoming line signal. This bit-field is set to "1" if the Clock Recovery PLL is out of lock with the incoming line signal.

Bit D3 - RLOS1 (Receive Loss of Signal Status - Channel(n))

This Read-Only bit-field indicates whether or not Channel(n) of the Receiver is currently declaring an LOS (Loss of Signal) Condition.

This bit-field is set to "0" if Channel(n) is NOT currently declaring the LOS Condition or, this bit-field is set to "1" if Channel(n) is declaring an LOS Condition.

Bit D2 - ALOS1 (Analog Loss of Signal Status - Channel(n))

This Read-Only bit-field indicates whether or not the Channel(n) Analog LOS Detector is currently declaring an LOS condition.

This bit-field is set to "0" if the Analog LOS Detector is NOT currently declaring a LOS condition. This bit-field is set to "1" if the Analog LOS Detector is currently declaring a LOS condition.

NOTE: *The purpose is to isolate the Detector (e.g., either the Analog LOS or the Digital LOS detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.*

Bit D1 - DLOS1 (Digital Loss of Signal Status - Channel(n))

This Read-Only bit-field indicates whether or not the Channel(n) Digital LOS Detector is currently declaring an LOS condition.

This bit-field is set to "0" if the Digital LOS Detector is NOT currently declaring an LOS condition. This bit-field is set to "1" if the Digital LOS Detector is currently declaring an LOS condition.

NOTE: *The purpose is to isolate the Detector (e.g., either the Analog LOS or the Digital LOS detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.*

Bit D0 - DMO (Drive Monitor Output Status - Channel(n))

This Read-Only bit-field reflects the status of the DMO output pin.

5.2.2 Command Register CR1

The bit-format and default values for Command Register CR1-(n) are listed below followed by the function of these bit-fields.

COMMAND REGISTER CR1-(N)

D4	D3	D2	D1	D0
TxOFF(n)	TAOS(n)	TxClkINV(n)	TxLEV(n)	TxBIN(n)
0	0	0	0	0

Bit D4 - TxOFF(n) (Transmitter OFF - Channel(n))

This Read/Write bit-field is used to turn off the Channel(n) Transmitter.

Writing a "1" to this bit field turns off the Transmitter and tri-state the Transmit Output. Writing a "0" to this bit-field turns on the Transmitter.

Bit D3 - TAOS(n) (Transmit All OneS - Channel(n))

This Read/Write bit-field is used to command the Channel(n) Transmitter to generate and transmit an all “1’s” pattern onto the line.

Writing a "1" to this bit-field commands the Transmitter to transmit an all “1’s” pattern onto the line. Writing a "0" to this bit-field commands normal operation.

Bit D2 - TxClkINV(n) (Transmit Clock Invert - Channel(n))

This Read/Write bit-field is used to configure the Transmitter in the XRT73L03 to sample the signal at the TPData and TNData pins on the rising edge or falling edge of TxClk (the Transmit Line Clock signal).

Writing a "1" to this bit-field configures the Transmitter to sample the TPData and TNData input pins on the rising edge of TxClk. Writing a "0" to this bit-field configures the Transmitter to sample the TPData and TNData input pins on the falling edge of TxClk.

Bit D1 - TxLEV(n) (Transmit Line Build-Out Enable/Disable Select - Channel(n))

This Read/Write bit-field is used to enable or disable the Channel(n) Transmit Line Build-Out circuit in the XRT73L03.

Setting this bit-field "High" disables the Channel(n) Line Build-Out circuit. In this mode, Channel(n) outputs partially-shaped pulses onto the line via the TTIP(n) and TRing(n) output pins.

Setting this bit-field "Low" enables the Channel(n) Line Build-Out circuit. In this mode, Channel(n) outputs shaped pulses onto the line via the TTIP(n) and TRing(n) output pins.

In order to comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements (per Bellcore GR-499-CORE or GR-253-CORE):

a. Set this bit-field to "1" if the cable length between the Cross-Connect and the transmit output of Channel(n) is greater than 225 feet.

b. Set this bit-field to "0" if the cable length between the Cross-Connect and the transmit output of Channel(n) is less than 225 feet.

NOTE: *This bit-field is active only if the XRT73L03 is configured to operate in the DS3 or SONET STS-1 Modes.*

If the cable length is greater than 225 feet, set this bit-field to "1" in order to increase the amplitude of the Transmit Output Signal. If the cable length is less than 225 feet, set this bit-field to "0".

NOTE: *This option is only available when the XRT73L03 is operating in the DS3 or STS-1 Mode.*

Bit D0 - TxBIN(n) (Transmit Binary Data - Channel(n))

This Read/Write bit-field is used to configure the Channel(n) Transmitter to accept an un-encoded binary data stream via the TPData input and convert this data into the appropriate bipolar signal for the line.

Writing a "1" configures the Transmitter to accept a binary data stream via the TPData input. The TNData input is ignored.

This form of data acceptance is sometimes referred to as Single-Rail mode operation. The Transmitter then encodes this data into the appropriate line code (e.g., B3ZS or HDB3) prior to its transmission over the line.

Writing a "0" configures the Transmitter to accept data in a Dual-Rail manner (e.g., via both the TPData and TNData inputs).

5.2.3 Command Register CR2-(n)

The bit-format and default values for Command Register CR2-(n) are listed below followed by the function of each of these bit-fields.

COMMAND REGISTER CR2-(N)

D4	D3	D2	D1	D0
Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQEN
X	0	0	0	0

Bit D4 - Reserved

Bit D3 - ENDECDIS (B3ZS/HDB3 Encoder/Decoder-Disable - Channel(n))

This Read/Write bit-field is used to enable or disable the Channel(n) B3ZS/HDB3 Encoder and Decoder blocks.

Writing a "1" to this bit-field disables the B3ZS/HDB3 Encoder and Decoder blocks. Writing a "0" to this bit-field enables the B3ZS/HDB3 Encoder and Decoder blocks.

NOTE: *This Encoder/Decoder performs HDB3 Encoding/Decoding if the XRT73L03 is operating in the E3 Mode. Otherwise it performs B3ZS Encoding/Decoding.*

Bit D2 - ALOSDIS (Analog LOS Disable - Channel(n))

This Read/Write bit-field is used to enable or disable the Channel(n) Analog LOS Detector.

Writing a "0" to this bit-field enables the Analog LOS Detector. Writing a "1" to this bit-field disables the Analog LOS Detector.

NOTE: *If the Analog LOS Detector is disabled, then the RLOS input pin is only asserted by the DLOS (Digital LOS Detector).*

Bit D1 - DLOSDIS (Digital LOS Disable - Channel(n))

This Read/Write bit-field to used to enable or disable the Channel(n) Digital LOS Detector .

Writing a "0" to this bit-field enables the Digital LOS Detector. Writing a "1" to this bit-field disables the Digital LOS Detector.

NOTE: If the Digital LOS Detector is disabled, then the RLOS input pin is only asserted by the ALOS (Analog LOS Detector).

Bit D0 - REQEN (Receive Equalization Enable - Channel(n))

This Read/Write bit-field is used to either enable or disable the Channel(n) internal Receive Equalizer of the XRT73L03.

Writing a "1" to this bit-field enables the Internal Equalizer. Writing a "0" to this bit-field disables the Internal Equalizer.

5.2.4 Command Register CR3-(n)

The bit-format and default values for Command Register CR3 are listed below followed by the function of these bit-fields.

COMMAND REGISTER CR3-(N)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_(n)	LOSMUT(n)	RxOFF(n)	RxClk(n)INV	Reserved
0	1	0	0	0

Bit D4 - SR/$\overline{DR}$_(n)(Single-Rail/Dual-Rail Data Output - Channel(n))

This Read/Write bit-field is used to configure Channel(n) in the XRT73L03 to output the received data from the Remote Terminal in a binary or Dual-Rail format.

Writing a "1" to this bit-field configures Channel(n) to output data to the Terminal Equipment in a binary Single-Rail format via the RPOS(n) output pin. RNEG(n) is grounded. Writing a "0" to this bit-field configures Channel(n) to output data to the Terminal Equipment in a Dual-Rail format via both the RPOS(n) and RNEG(n) output pins.

Bit D3 - LOSMUT(n) (Recovered Data MUTing during LOS Condition - Channel(n))

This Read/Write bit-field is used to configure Channel(n) in the XRT73L03 to NOT output any recovered data from the line while it is declaring an LOS condition.

Writing a "0" to this bit-field configures the chip to output recovered data even while the XRT73L03 is declaring an LOS condition. Writing a "1" to this bit-field configures the chip to NOT output the recovered data while an LOS condition is being declared.

NOTE: In this mode, RPOS(n) and RNEG(n) is set to "0" asynchronously.

Bit D2 - RxOFF(n) (Receive Section - Shut OFF Select)

This Read/Write bit-field is used to shut-off the Receive Section of Channel(n) in the XRT73L03. The purpose of this feature is to permit conservation of power consumption when this is the back-up device in a Redundancy System.

Writing a "1" into this bit-field shuts off the Receive Section of Channel(n). Writing a "0" into this bit-field turns on the Receive Section of Channel(n).

Bit D1 - RxClk(n)INV (Invert RxClk(n))

This Read/Write bit-field is used to configure the Receiver of Channel(n) of the XRT73L03) to output the recovered data on either the rising edge or the falling edge of the RxClk(n) clock signal.

Writing a "0" to this bit-field configures the Receiver to output the recovered data on the rising edge of the RxClk(n) output signal. Writing a "1" to this bit-field configures the Receiver to output the recovered data on the falling edge of the RxClk(n) output signal.

Bit D0 - Reserved

This bit-field has no defined functionality.

Command Register CR4-(n)

The bit-format and default values for Command Register CR4 are listed below followed by the function of each of these bit fields.

COMMAND REGISTER CR4-(N)

D4	D3	D2	D1	D0
Reserved	STS-1/$\overline{DS3}$_ Ch(n)	E3_Ch(n)	LLB(n)	RLB(n)
0	0	0	0	0

Bit D4 - Reserved

This bit-field has no defined functionality.

Bit D3 - STS-1/($\overline{DS3}$_(n)) - Channel(n) - Mode Select

This Read/Write bit field is used to configure Channel(n) to operate in either the SONET STS-1 Mode or the DS3 Mode.

Writing a "0" into this bit-field configures Channel(n) to operate in the DS3 Mode. Writing a "1" into this bit-field configures Channel(n) to operate in the SONET STS-1 Mode.

NOTE: *This bit-field is ignored if the E3_Ch(n) bit-field (e.g., D2 in this Command Register) is set to "1".*

Bit D2 - E3 Mode Select - Channel(n)

This Read/Write bit-field is used to configure Channel(n) to operate in the E3 Mode.

Writing a "0" into this bit-field configures Channel(n) to operate in either the DS3 or SONET STS-1 Mode as specified by the setting of the DS3 bit-field in this Command Register. Writing a "1" into this bit-field configures Channel(n) to operate in the E3 Mode.

Bit D1 - LLB(n) (Local Loop-Back - Channel(n))

This Read/Write bit-field along with RLB(n) is used to configure Channel(n) to operate in any one of a variety of Loop-Back modes.

Table 8 relates the contents of LLB(n) and RLB(n) and the corresponding Loop-Back mode for Channel(n).

Bit D0 - RLB(n) (Remote Loop-Back - Channel(n))

This Read/Write bit-field along with LLB(n) is used to configure Channel(n) to operate in any one of a variety of Loop-Back modes.

Table 8 relates the contents of LLB(n) and RLB(n) and the corresponding Loop-Back mode for Channel(n).

TABLE 8: CONTENTS OF LLB(N) AND RLB(N) AND THE CORRESPONDING LOOP-BACK MODE FOR CHANNEL(N)

LLB(n)	RLB(n)	LOOP-BACK MODE (FOR CHANNEL(n))
0	0	None
1	0	Analog Loop-Back Mode (See Section 4.1 for Details)
1	1	Digital Loop-Back Mode (See Section 4.2 for Details
0	1	Remote Loop-Back Mode (See Section 4.3 for Details

5.3 OPERATING THE MICROPROCESSOR SERIAL INTERFACE.

The XRT73L03 Serial Interface is a simple four wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

- $\overline{CS}$ - Chip Select (Active Low)
- SClk - Serial Clock
- SDI - Serial Data Input
- SDO - Serial Data Output

Using the Microprocessor Serial Interface

The following instructions for using the Microprocessor Serial Interface are best understood by referring to the diagram in Figure 33 and the timing diagram in Figure 34.

In order to use the Microprocessor Serial Interface, a clock signal must be first applied to the SClk input pin. Then, initiate a Read or Write operation by asserting the active-low Chip Select input pin $\overline{CS}$. It is important to assert the $\overline{CS}$ pin (e.g., toggle it “Low") at least 50ns prior to the very first rising edge of the clock signal.

Once the $\overline{CS}$ input pin has been asserted, the type of operation and the target register address must now be specified. Provide this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input.

NOTE: *Each of these bits is clocked into the SDI input on the rising edge of SClk.*

Bit 1- R/W (Read/Write) Bit

This bit is clocked into the SDI input on the first rising edge of SClk after $\overline{CS}$ has been asserted. This bit indicates whether the current operation is a Read or Write operation. A "1" in this bit specifies a Read operation, a "0" in this bit specifies a Write operation.

Bits 2 through 6: The five (5) bit Address Values (labeled A0, A1, A2 , A3 and A4)

The next five rising edges of the SClk signal clocks in the 5-bit address value for this particular Read or Write operation. The address selects the Command Register in the XRT73L03 that the user either be reading data from or writing data to. The address bits must be applied to the SDI input pin in ascending order with the LSB (least significant bit) first.

Bit 7:

A5 must be set to "0" as shown in Figure 33.

Bit 8 - A6:

The value of "A6" is a don't care.

Once these first 8 bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a Read or Write operation.

Read Operation

Once the last address bit (A4) has been clocked into the SDI input, the Read operation proceeds through an idle period lasting two SClk periods. On the falling edge of SClk Cycle #8 (see Figure 33) the serial data output signal (SDO) becomes active. At this point, reading the data contents of the addressed Command Register at Address [A4, A3, A2, A1, A0] via the SDO output pin can begin. The Microprocessor Serial Interface outputs this five bit data word (D0 through D4) in ascending order with the LSB first, on the falling edges of the SClk pin. Consequently, the data on the SDO output pin is sufficiently stable for reading by the Microprocessor on the very next rising edge of the SClk pin.

Write Operation

Once the last address bit (A4) has been clocked into the SDI input, the Write operation proceeds through an idle period lasting two SClk periods. Prior to the rising edge of SClk Cycle # 9 (see Figure 33). Apply the desired eight bit data word to the SDI input pin via the Microprocessor Serial Interface. The Microprocessor Serial Interface latches the value on the SDI input pin on the rising edge of SClk. Apply this word (D0 through D7) serially, in ascending order with the LSB first.

Simplified Interface Option

The design of the circuitry connecting to the Microprocessor Serial Interface can be simplified by tying both the SDO and SDI pins together and reading data from and/or writing data to this combined signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal is tri-stated.

NOTES:

1. *A5 is always "0"*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*
4. *Shaded blocks denotes a "don't care" value*

FIGURE 33. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE

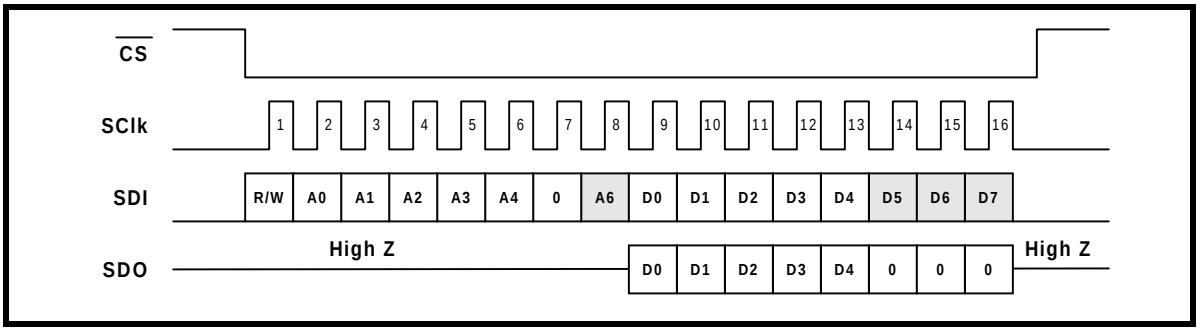
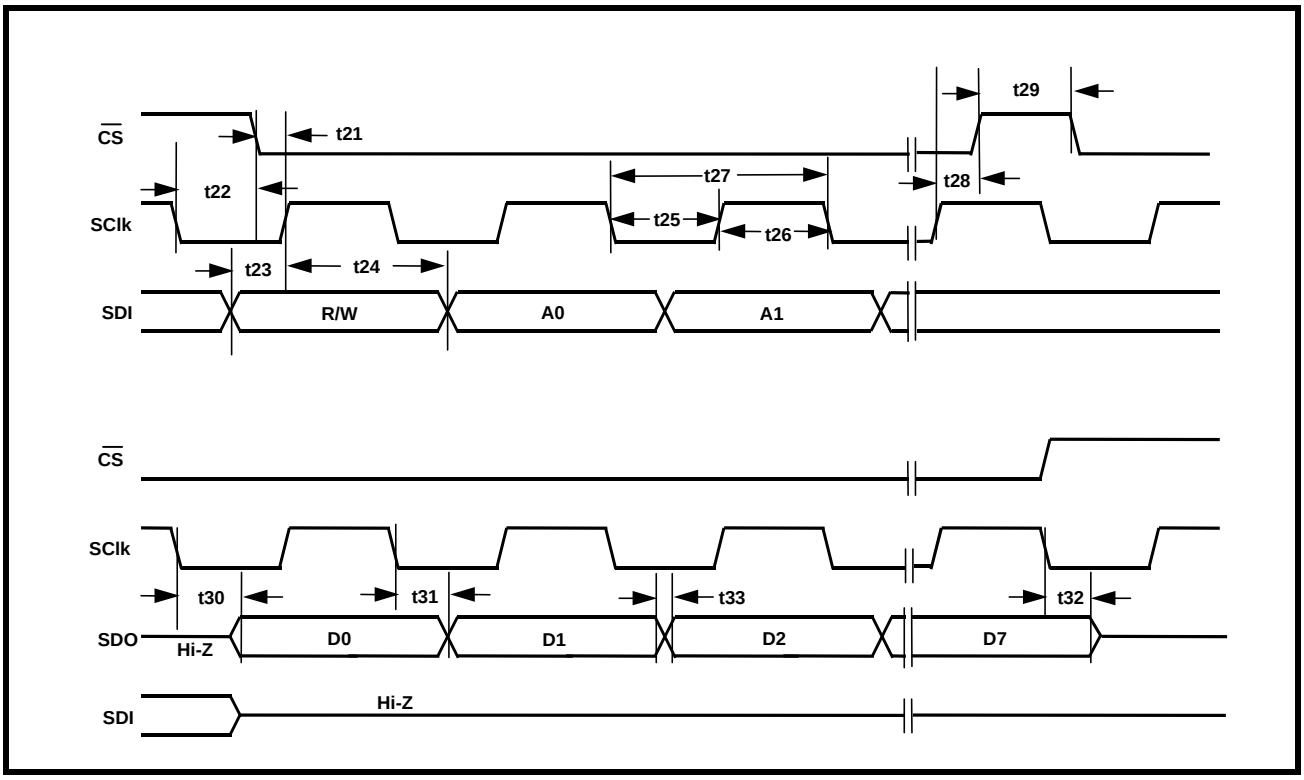


FIGURE 34. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

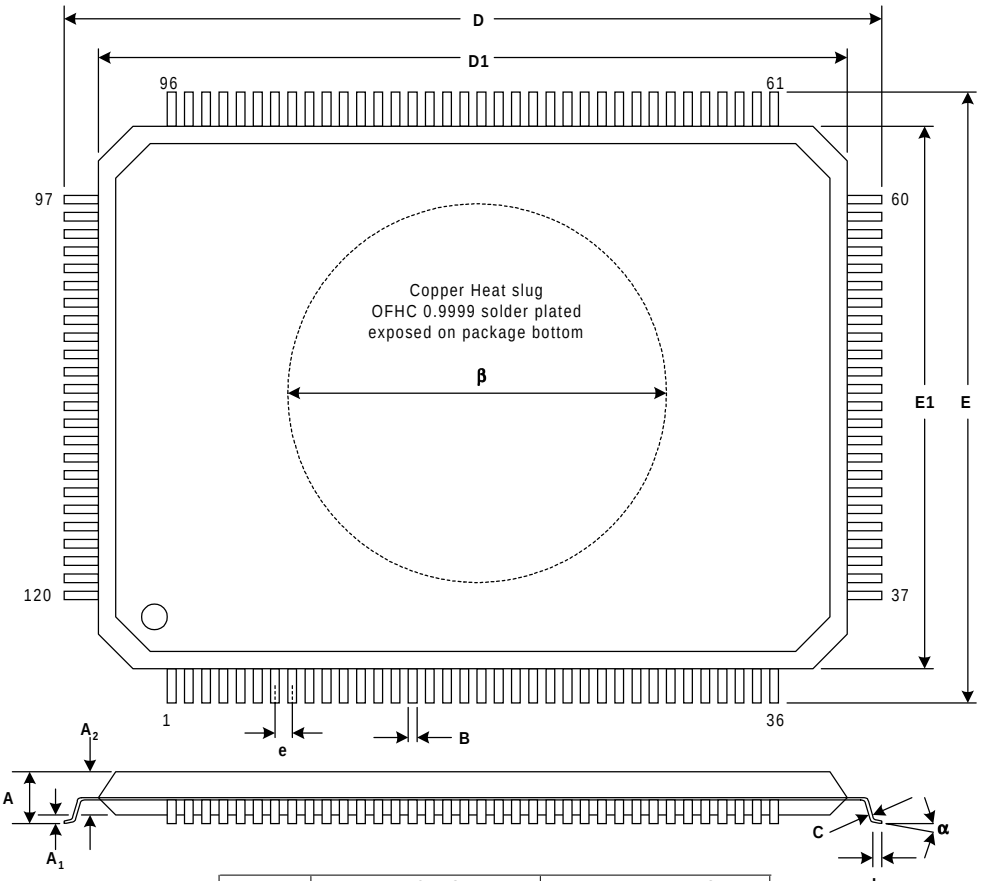


ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73L03IV	120 Pin Thermally Enhanced TQFP 14mm X 20mm	-40°C to +85°C
THERMAL INFORMATION	Theta-J_A = 23° C/W	Theta-J_C =7° C/W

PACKAGE DIMENSIONS

120 LEAD THIN QUAD FLAT PACK
14mm X 20 mm, TQFP
Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.80	22.20
D1	0.783	0.791	19.90	20.10
E	0.622	0.638	15.80	16.20
E1	0.547	0.555	13.90	14.10
e	0.020BSC		0.50BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	0.370	0.390	9.40	9.90

Note: The control dimension is the millimeter column

REVISION HISTORY

Rev. 1.0.1 to Rev.1.0.2

Edits to describe one channel only, as applicable to all channels. Corrected pin names for consistency.

Rev. 1.0.2 to Rev. 1.0.3

Pin names, numbers and rotation have been changed.

Rev. 1.0.3 to Rev. 1.0.4

Changed package to 14X20mm with 0.5mm pin spacing. Pin #'s/ pin names have been changed.

Rev. 1.0.4 to Rev. 1.0.5

Added 120 lead 14x14mm, 0.4mm pitch package into data sheet, pin names have changed from Rev. 1.0.3.

Rev. 1.0.5 to Rev. 1.0.6

Rotated pins on 14X14mm package (pin 1 became 31).

Rev. 1.0.6 to Rev. A1.0.7

Corrected references to similar pins in the pin list to correspond to the changes in pin out.

Rev.A1.0.7 to P1.0.7

Changed Advanced Confidential to Preliminary

Rev. P1.0.7 to P1.0.8

Minor typo changes modified Block Diagram to call out Tx Control.

Rev. P1.0.8 to P1.0.9

Removed excess " " marks. Deleted the 14x14mm package which is no longer offered.

Rev. P1.0.9 to P1.0.10

Pins 47 thru 52 were shifted, 52 and 53 are No Connection Pins, not 47 and 48.

Rev. P1.0.10 to Rev. 1.0.11

Removed unnecessary verbiage.

Rev. P1.0.11 to Rev. P1.0.12

Add copper heat slug to package outline drawing and add explantion in text of electrical characteristics.

Rev. P1.0.12 to Rev. P1.0.13

Revised figures 4 and 5, corrected pin numbers on tables 1 & 3.

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