15W/Ch STEREO CLASS-D AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TMPA420DS is a Bridge-Tied-Load (BTL) output Class-D audio power amplifier for driving speakers with high power efficiency. It is able to drive 4Ω, 6Ω, 8Ω or 16Ω speakers. The output power can be up to 15W per channel. No external heat-sink is necessary.

The gain of the amplifier is defined by either gain0/gain1 gain control or by input resistance. Thermal protection and short-circuit protection are integrated for safety purpose.

The internal de-pop circuitry eliminates pop noise at power-up & shutdown operations.

FEATURES

- ♦ **15W/Ch Stereo Class-D Output**
- ♦ **Power efficiency is up to 82%**
- ♦ **Convenient gain control**
- ♦ **Time delay for de-pop control**
- ♦ **Thermal Protection**
- ♦ **Output Pin Short-Circuit Protection**
- ♦ **Low Quiescent Current (10mA Typical at 12V)**
- ♦ **Low Current in Shutdown Mode (<1μA Typical)**
- ♦ **Separate VCC & PVCC**
- ♦ **Regulated 5-V Supply Output**

APPLICATIONS

LCD Monitors, TVs, DVD Players and Powered Speakers

PACKAGE

QFN48 available

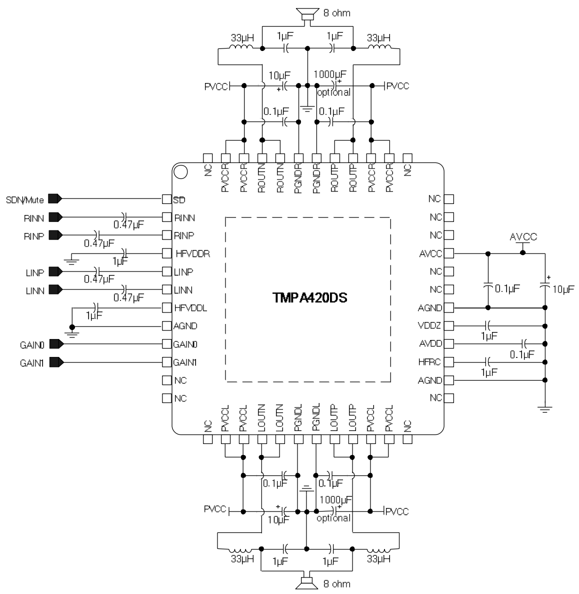
For best performance, please refer to

http://www.taimec.com.tw/English/EVM.htm

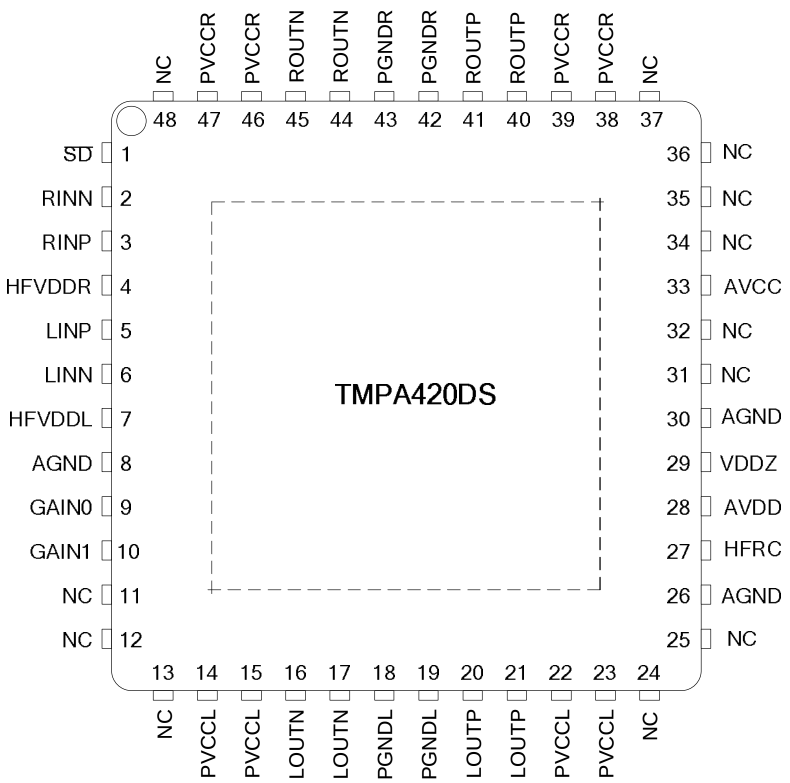
http://www.class-d.com.tw/English/EVM.htm

for PCB layout.

REFERENCE CIRCUIT



QFN PACKAGE
(TOP VIEW)



（Please email david@taimec.com.tw for complete datasheet.）

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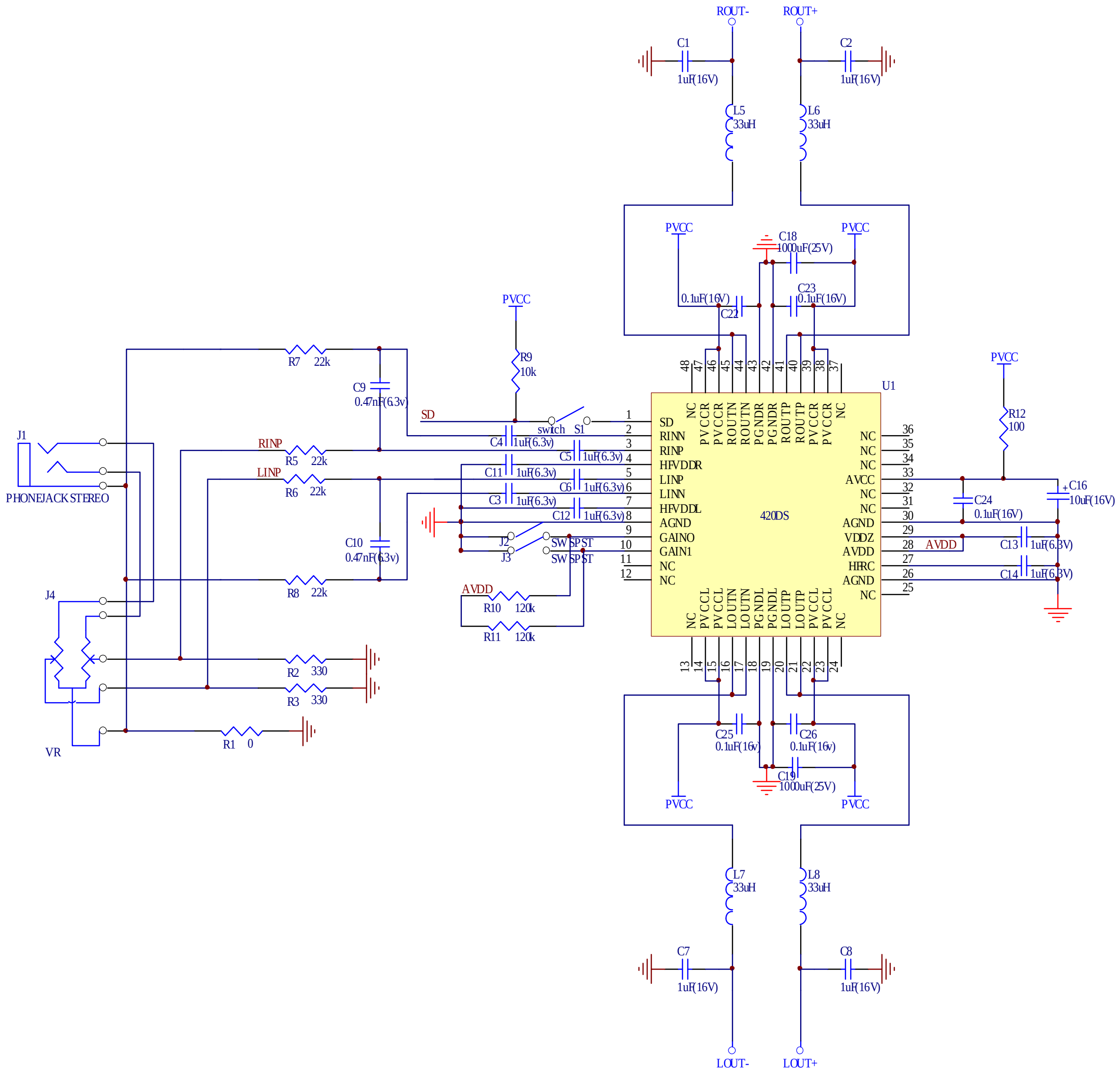
Note that the external components or PCB layout should be designed not to generate abnormal voltages to the chip to prevent from latch up which may cause damage to the device.

Typical Application



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO		
AGND	8,26,30	—	Analog ground
AVCC	33	—	High-voltage power supply (8V to 15V)
AVDD	28	I	5-V voltage
HFVDDR	4	O	2.5-V Reference for convenience of single-ended inputs
HFVDDL	7	O	2.5-V Reference for convenience of single-ended inputs
HFRC	27	O	Power up delay
LINN	6	I	Negative differential input for left channel
LINP	5	I	Positive differential input for left channel
LOUTN	16,17	O	Class-D negative output for left channel
LOUTP	20,21	O	Class-D positive output for left channel
PGNDL	18,19	—	Power ground for left channel
PGNDR	42,43	—	Power ground for right channel
PVCCL	14,15,22,23	—	Power supply for left channel(8V to 15V)
PVCCR	38,39,46,47	—	Power supply for right channel(8V to 15V)
RINP	3	I	Positive differential input for right channel
RINN	2	I	Negative differential input for right channel
ROUTN	44,45	O	Class-D negative output for right channel
ROUTP	40,41	O	Class-D positive output for right channel
$\overline{SD}$	1	I	Shutdown (Low valid)
GAIN0	9	I	Gain0 control
GAIN1	10	I	Gain1 control
VDDZ	29	O	5-V Regulated output (25mA output)
NC	11,12,13,24, 25,31,32,34, 35, 36,37,48	—	No connection

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted(1)

Supply voltage, PV_{CCR}, PV_{CCL}, AV_{CC} (Iload=0)	In normal mode	-0.3V to 17V	V
	In shutdown mode	-0.3V to 17V	V
Input voltage, $\overline{SD}$		-0.3V to AV_{CC}+0.3V	V
Input voltage, Gain0, Gain1, LINN, LINP, RINN, RINP		-0.3V to 5V	V
Continuous total power dissipation		See package dissipation ratings	
Operating free-air temperature, T_A		-20 to 85	°C
Operating junction temperature, T_J		-20 to 150	°C
Storage temperature, T_{stg}		-40 to 150	°C

(1) Stresses beyond those listed under"absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions "is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CCR}, PV_{CCL}, AV_{CC}	8	15	V
High-level input voltage, V_{IH}	$\overline{SD}$, Gain0, Gain1	2.0		V
Low-level input voltage, V_{IL}	$\overline{SD}$, Gain0, Gain1		0.8	V
High-level input current, I_{IH}	V_{CC}=15V, $\overline{SD}$ =15V		100	uA
	V_{CC}=15V, Gain0=Gain1=5V		5	
Low-level input current, I_{IL}	V_{CC}=15V, $\overline{SD}$ =0V		0.5	uA
	V_{CC}=15V, Gain0=Gain1=0V		0.5	
Operating free-air temperature, T_A		-20	85	°C

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR	$T_A \le 25$ °C POWER RATING	T_A = 70 °C POWER RATING	T_A = 85 °C POWER RATING
QFN48(FD)	33 mW/ °C	4.125W	2.64W	2.15W

DC CHARACTERISTICS

T_A=25 °C, V_{CC}=15V, R_L=8Ω speaker (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	LINN LINP RINN RINP AC grounded			30		mV
V_{DD}/AV_{DD}	5-V Regulated output	I_O=0 to25mA, $\overline{SD}$ =High, V_{CC}=8V to 15V		4.5	5.0	5.5	V
f_{OSC}	Oscillator frequency	PV_{CC}= V_{CC}=8-15V		250		350	kHz
HFV_{DDR}/HFV_{DDL}	Half V_{DD} reference output	No load			0.5x AV_{DD}		
I_{CC}	Quiescent current (no load)	$\overline{SD}$ =High, V_{CC}= 12V			10	20	mA
		$\overline{SD}$ =High, V_{CC}= 15V			16	30	
$I_{CC(SD)}$	Supply current in shutdown mode	$\overline{SD}$ =0.8V, V_{CC}= 9V~15V			1		uA
$r_{ds(on)}$	Drain-source on-state resistance for all outputs	V_{CC}=15V I_O=1A,	High side		600		mΩ
			Low side		500		
			Total		1100		
Gain	Voltage Gain at Vcc=15V	Gain0=High, Gain1= High			34		dB
		Gain0=Low, Gain1=High			28		
		Gain0=High, Gain1= Low			22		
		Gain0=Low, Gain1= Low			18		
	Voltage Gain at Vcc=12V	Gain0=High, Gain1= High			32		dB
		Gain0=Low, Gain1=High			26		
		Gain0=High, Gain1= Low			20		
		Gain0=Low, Gain1= Low			16		
	Voltage Gain at Vcc=9V	Gain0=High, Gain1= High			30		
		Gain0=Low, Gain1=High			25		
		Gain0=High, Gain1= Low			19		
		Gain0=Low, Gain1= Low			14		
Zi	Input resistance of RINN/RINP/LINN/LINP	Gain0=High, Gain1= High			15		kΩ
		Gain0=Low, Gain1=High			30		
		Gain0=High, Gain1= Low			60		
		Gain0=Low, Gain1= Low			100		

AC CHARACTERISTICS

T_A=25 °C, V_{CC}=15V, R_L=8Ω speaker (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
*$P_{O(max)}$	Maximum continuous output power (r.m.s) at 1kHz, (Limited by thermal condition)	R_L=4Ω	15V		12.5		W
			12V		10		
			9V		6.22		
		R_L=6Ω	15V		15		W
			12V		9.3		
			9V		5.34		
		R_L=8Ω	15V		12.7		W
			12V		8		
			9V		4.58		
		R_L=16Ω	15V		7.65		W
			12V		4.8		
			9V		2.73		
V_n	Output noise				-70		dBV
SNR	Signal-to-noise ratio	Maximum output at THD+N＜0.5%, f=1kHz			85		dB
Crosstalk	Crosstalk between outputs	Gain0=Gain1=high, V_{CC}=12V, P_O=1W R_L=8Ω			-60		dB
	Thermal trip point				145		°C
	Thermal hysteresis				25		°C

*Important notice：More copper area and vias are required for high output power especially when the output power is higher than 7W×2.

DETAILED DESCRIPTION

Efficiency

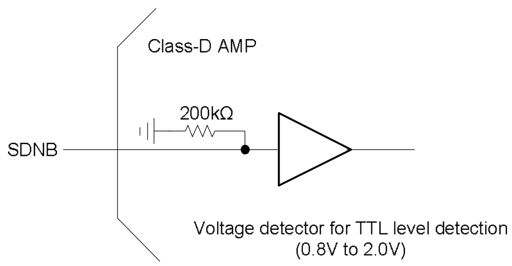
The output transistors of a class D amplifier act as switches. The power loss is mainly due to the turn on resistance of the output transistors when driving current to the load. As the turn on resistance is so small that the power loss is small and the power efficiency is high. With 8 ohm load the power efficiency can be better than 80%.

PCB layout for power dissipation

No heat sink is necessary for power dissipation. However the PCB layout should be well designed to dissipate heat for high output power. With 80% power efficiency the generated heat when driving 15 watts to the 8 ohm load is about 3.75 watts. The heat can be carried out through the thermal pad of the device to the PCB. To ensure proper dissipation of heat the PCB has to have heat path from the bottom of the device which is soldered to the PCB. The area of the metal on the PCB for heat dissipation should be big enough. It is suggested that both sides of the PCB are used for power dissipation.

Shutdown

The shutdown mode reduces power consumption. A LOW at shutdown pin forces the device in shutdown mode and a HIGH forces the device in normal operating mode. Shutdown mode is useful for power saving when not in use. This function is useful when other devices like earphone amplifier on the same PCB are used but class D amplifier is not necessary.
Internal circuit for shutdown is shown below.



HFRC（pop-less）

HFRC provides a way of soft start up delay. A half_Vcc voltage detector is integrated to detect a RC charge up. The resistor of 320k ohms of the RC circuit is also integrated in the chip but the capacitor is externally hooked up. For C=1uF the half_Vcc delay is

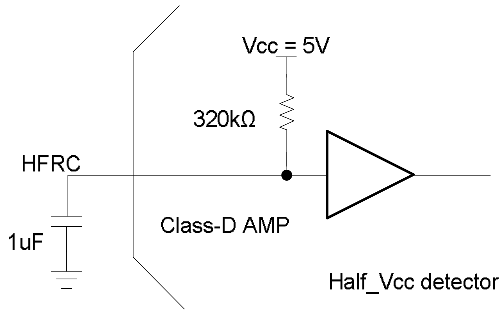
$$1-e^{-t/RC}=0.5$$

or

$$e^{-t/RC}=0.5$$

that is

$t = -RC\ ln(0.5) = (320k \times 1u)(0.693) = 0.22$ seconds



Differential input VS single ended input

Differential input offers better noise immunity over single ended input. A differential input amplifier suppresses common noise and amplifies the difference voltage at the inputs. For single ended applications just tie the negative input end of the balanced input structure to ground. If external input resistors are used, the negative input has to be grounded with a series resistor of the same value as the positive input to reduce common noise.

Voltage gain

The voltage gain can be set through gain0/gain1 control or by external input resistors connecting to input pins. If external resistors are used they should be well matched. Well matched resistors are also required even for single ended input configuration for low noise. Suppose the external input resistors Rext are used then the voltage gain is roughly

Av=750k ohms / (Rext+15k ohms) for gain0=gain1=High

Where 15k ohms is the internal resistance of the input pins. For other gain0/gain1 states please refer to DC CHARACTERISTICS for different input resistance.

Input filter

AC coupling capacitors are required to block the DC voltage from the device. They also define the –3db frequency at the low frequency side.

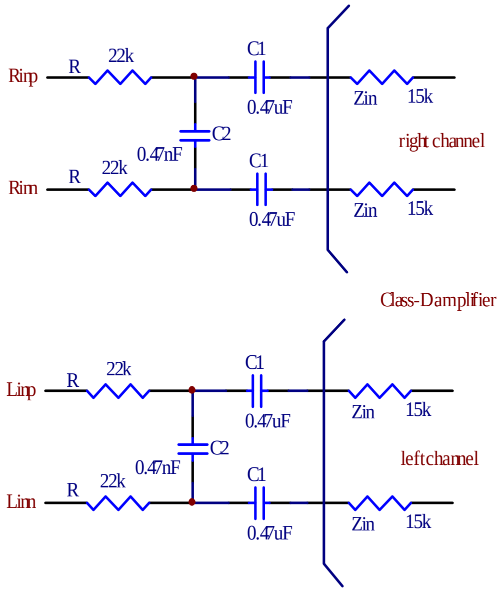
The –3db frequency of the low frequency side is

$$f_{-3db} = 1/(2\pi R C)$$

where C is the AC coupling capacitance and R is the total resistance in series with C.

Note that R=Zin(internal resistance) + Rext(external resistance)
Also note that the input resistance of RINN/RINP/LINN/LINP is 15K ohms at Gain0=Gain1=high. Please refer to DC CHARACTERISTICS for detail.

In the following diagram Rext=22k ohms, Zin=15k ohms and C=C1=0.47uF. Thus the –3db frequency at the low frequency side is about 9Hz.



A bypass capacitor placed in between the positive signal path and negative signal path is to attenuate the high frequencies. It defines the –3bd frequency at the high frequency side. The input filter becomes a band pass filter.
The –3db frequency of the high frequency side is

f–3db=1/(2 π RC)

where C is the bypass capacitance and R is the total resistance in parallel with C.

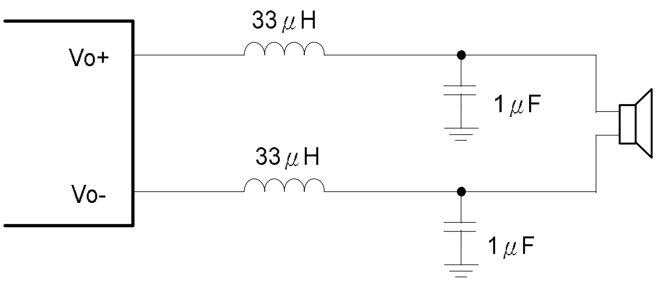
In this example Rext=22k ohms, Zin=15k ohms and C=C2=0.47nF. Thus the –3db frequency at the high frequency side is about 19kHz.

Output filter

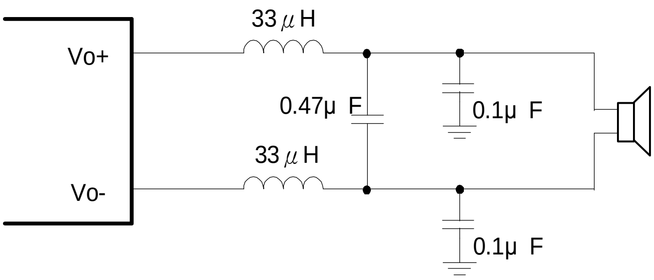
Ferrite bead filter can be used for EMI purpose. The ferrite filter reduces EMI around 1 MHz and higher（FCC and CE only test radiated emissions greater than 30 MHz）. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency（<1 MHz）EMI sensitive circuits and/or there are long wires from the amplifier to the speaker. EMI is also affected by PCB layout and the placement of the surrounding components.

The suggested LC values for different speaker impendence are showed in following figures for reference.



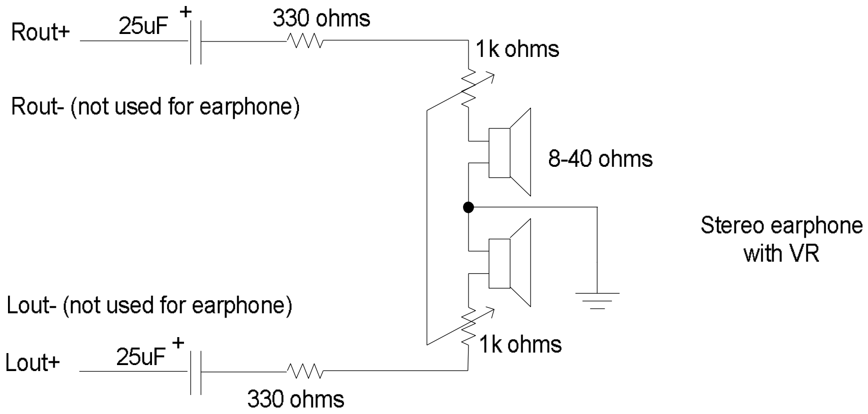
Typical LC Output Filter (1)

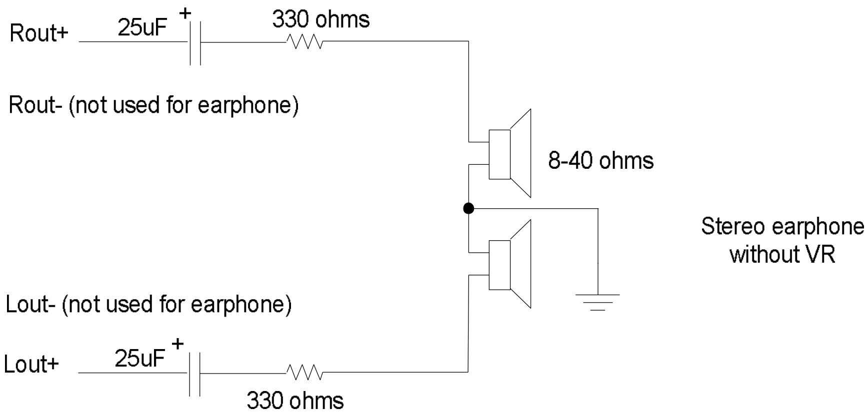


Typical LC Output Filter (2)

EARPHONE USE

Class-D output can be used to drive earphone. However to avoid high power to overdrive earphone and to prevent human ear to accidentally be hurt, a resistor has to be put in series with the earphone speaker. Typically a resistor of 330 ohms is adequate for this purpose. Since stereo earphone can not have BTL configuration, one end of BTL signals can be used as SE (single-ended) output.





Over temperature protection

A temperature sensor is built in the device to detect the temperature inside the device. When a high temperature around 145°C and above is detected the switching output signals are disabled to protect the device from over temperature. Automatic recovery circuit enables the device to come back to normal operation when the internal temperature of the device is below around 120 °C.

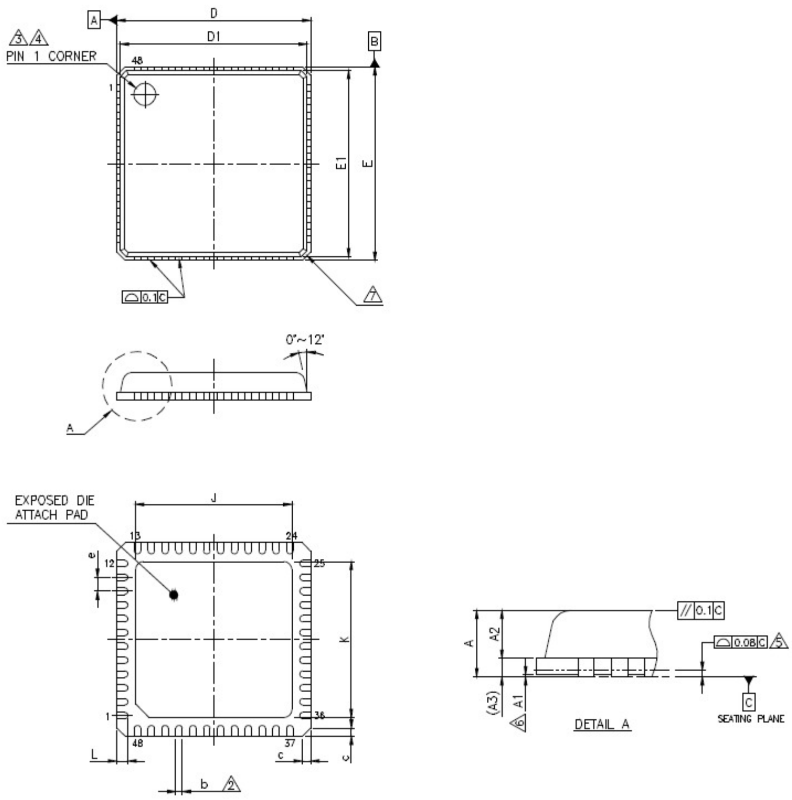
Over temperature protection

A temperature sensor is built in the device to detect the temperature inside the device. When a high temperature around 145°C and above is detected the switching output signals are disabled to protect the device from over temperature. Automatic recovery circuit enables the device to come back to normal operation when the internal temperature of the device is below around 120°C.

Over current protection

A current detection circuit is built in the device to detect the switching current of the output stages of the device. It disables the device when a pulse current beyond 8 amps is detected. It protects the device when there is an accident short between outputs or between output and ground pins. It also protects the device when an abnormal low impedance is tied to the output. High current beyond the specification may potentially causes electron migration and permanently damage the device. Shutdown or power down is necessary to resolve the protection situation. There is no automatic recovery from over current protection.

Physical Dimensions (IN MILLIMETERS)



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
⚠ A2	0.65 REF.		
A3	0.203 REF.		
b	0.18	0.25	0.30
C	0.24	0.42	0.60
D	7.00 BSC.		
D1	6.75 BSC.		
E	7.00 BSC.		
E1	6.75 BSC.		
e	0.50 BSC.		
J	2.25	4.70	5.25
K	2.25	4.70	5.25
L	0.30	0.40	0.50

UNIT : mm

NOTES :

1. JEDEC : MO-220-J.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).

⚠2 DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.

⚠3 THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.

⚠4 EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.

⚠5 APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.

⚠6 APPLIED ONLY TO TERMINALS.

⚠7 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

QFN48

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