



Accutec Microcircuit Corporation

AK581024AG / AK581024AS 1,048,576 x 8 bit CMOS Dynamic Random Access Memory

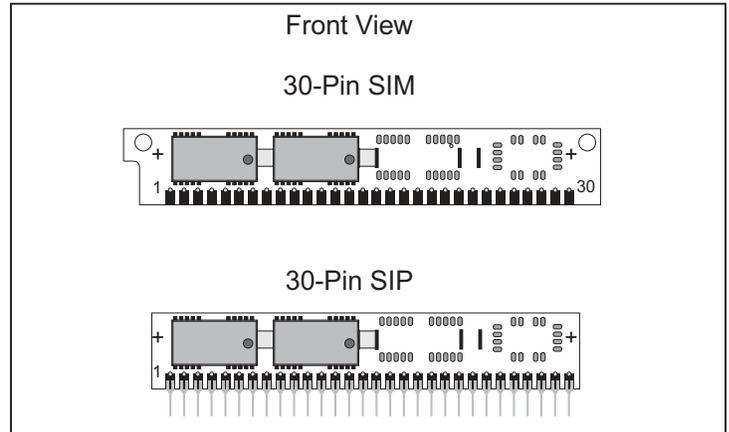
DESCRIPTION

The Accutec AK581024 high density memory modules is a random access memory organized in 1 Meg x 8 bit words. The assembly consists of two 1 Meg x 4 DRAMs in surface mount packages mounted to a printed circuit board. The module can be configured as a leadless 30 pad SIMM or a leaded 30 pin SIP. This packaging approach provides a better than 6 to 1 density increase over standard DIP packaging.

The operation of the AK581024 is identical to two 1 Meg x 4 DRAMs. The data input/output is brought out separately for each 1 Meg x 4 device, with common $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ control. The $\overline{\text{OE}}$ pins are tied to V_{ss} which dictates the use of early-write cycles to prevent contention of D and Q. Since the Write-Enable ($\overline{\text{WE}}$) signal must always go low before $\overline{\text{CAS}}$ in a write cycle, Read-Write and Read-Modify-Write operation is not possible.

FEATURES

- 1 Meg x 8 bit organization
- Optional 30 Pad SIM (Single In-Line Module) or 30 Pin leaded SIP (Single In-Line Package)
- JEDEC approved pinout
- Common $\overline{\text{CAS}}$, $\overline{\text{RAS}}$ and $\overline{\text{WE}}$ control for eight DQ lines
- Separate $\overline{\text{CAS}}$ control for one separate pair of D and Q lines
- 1024 refresh cycles/16ms, A_0 to A_9
- 1.10 Watt active and 23.5 mWatt standby (max)
- Operating free air temperature: 0° to 70°C
- Upward compatible with AK584096 and AK5816384
- Functionally and Pin compatible with AK481024
- Available with access times of 60 to 100 ns



PIN NOMENCLATURE

DQ ₁ - DQ ₈	Data In/Data Out
A ₀ - A ₉	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Write Enable
V _{cc}	5v Supply
V _{ss}	Ground
NC	No Connect

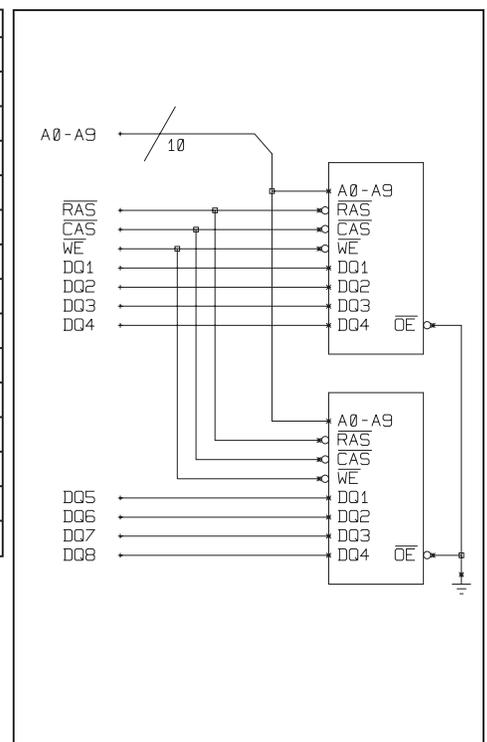
MODULE OPTIONS

Leadless SIM: AK581024ASP
Leaded SIP: AK581024AGP

PIN ASSIGNMENT

PIN #	SYMBOL	PIN #	SYMBOL
1	V _{cc}	16	DQ ₅
2	CAS	17	A ₈
3	DQ ₁	18	A ₉
4	A ₀	19	NC
5	A ₁	20	DQ ₆
6	DQ ₂	21	WE
7	A ₂	22	V _{ss}
8	A ₃	23	DQ ₇
9	V _{ss}	24	NC
10	DQ ₃	25	DQ ₈
11	A ₄	26	NC
12	A ₅	27	RAS
13	DQ ₄	28	NC
14	A ₆	29	NC
15	A ₇	30	V _{cc}

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

PART NUMBER CODING INTERPRETATION

Position	1	2	3	4	5	6	7	8
1 Product								
	AK = Accuthek Memory							
2 Type								
	4 = Dynamic RAM							
	5 = CMOS Dynamic RAM							
	6 = Static RAM							
3 Organization/Word Width								
	1 = by 1 16 = by 16							
	4 = by 4 32 = by 32							
	8 = by 8 36 = by 36							
	9 = by 9							
4 Size/Bits Depth								
	64 = 64K		4096 = 4 MEG					
	256 = 256K		8192 = 8 MEG					
	1024 = 1 MEG		16384 = 16 MEG					
5 Package Type								
	G = Single In-Line Package (SIP)							
	S = Single In-Line Module (SIM)							
	D = Dual In-Line Package (DIP)							
	W = .050 inch Pitch Edge Connect							
	Z = Zig-Zag In-Line Package (ZIP)							
6 Special Designation								
	P = Page Mode							
	N = Nibble Mode							
	K = Static Column Mode							
	W = Write Per Bit Mode							
	V = Video Ram							
7 Separator								
	- = Commercial 0°C to +70°C							
	M = Military Equivalent Screened (-55°C to +125°C)							
	I = Industrial Temperature Tested (-45°C to +85°C)							
	X = Burned In							
8 Speed (first two significant digits)								
	DRAMS				SRAMS			
	60 = 60 nS		12 = 12 nS					
	70 = 70 nS		15 = 15 nS					
	80 = 80 nS		20 = 20 nS					

The numbers and coding on this page do not include all variations available, but are shown as examples of the most widely used variations. Contact Accuthek if other information is required.



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EXAMPLES:

AK581024ASP-60

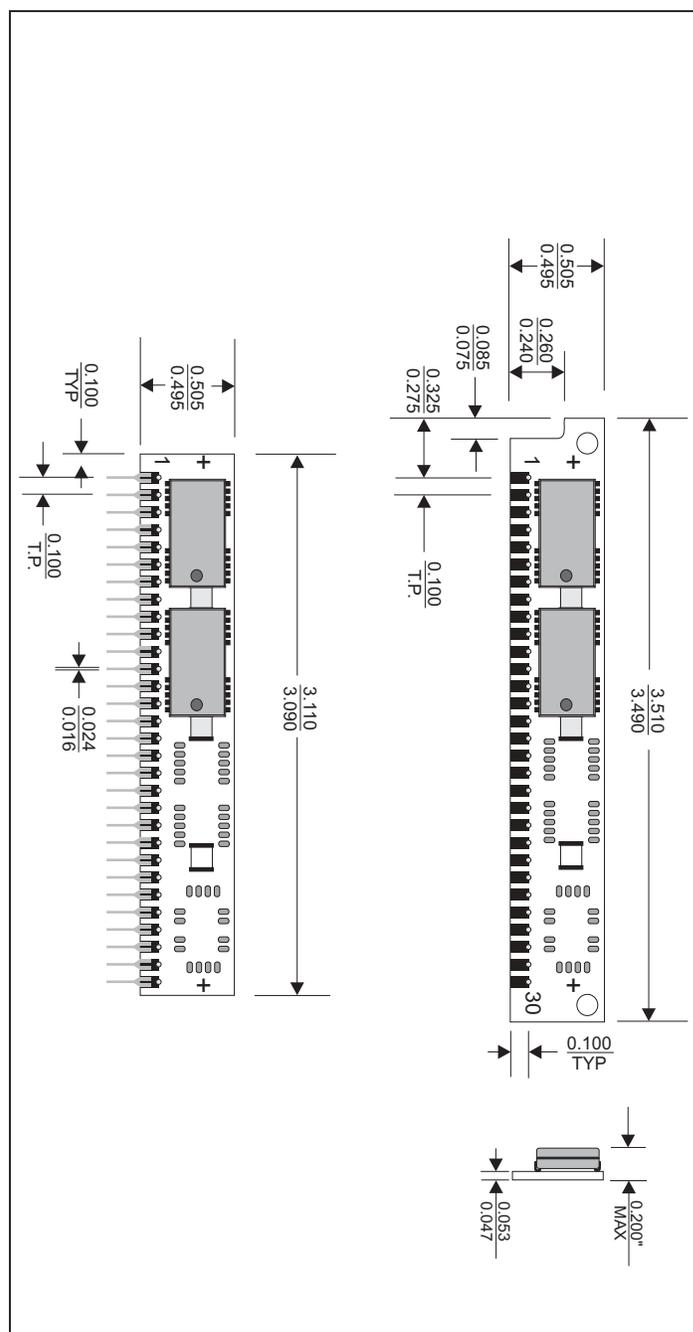
1 Meg x 8, Dynamic RAM, Leadless SIM, Page Mode, Commercial, 60 nSEC Access Time

AK581024AGP-70

1 Meg x 8, Dynamic RAM, Leaded SIP, Page Mode Commercial, 70 nSEC AccessTime

MECHANICAL DIMENSIONS

Inches



Accuthek reserves the right to make changes in specifications at any time and without notice. Accuthek does not assume any responsibility for the use of any circuitry described; no circuit patent licenses are implied. Preliminary data sheets contain minimum and maximum limits based upon design objectives, which are subject to change upon full characterization over the specific operating conditions.