Si85xx UNIDIRECTIONAL AC CURRENT SENSORS

Features

- Single-chip ac current sensor/conditioner
- Low loss: Less than 1.3 mΩ primary series resistance; less than 2 nH primary inductance at 25 ºC
- Leading-edge noise suppression eliminates need for leading-edge blanking
- "Ping-Pong" output version allows one Si85xx to replace two current transformers in full-bridge applications
- 5, 10, and 20 A full-scale versions
- $\overline{\text{FAULT}}$ output helps safeguard operation
- 1,000 VDC isolation
- Accurate to ±5% of measurement
- Large 2 V_{PP} output pins signal at full scale
- High-side or low-side current sensing
- –40 to 125 ºC operating range (Si85x4/5/6)
- Small 4 x 4 x 1 mm package
- Low cost

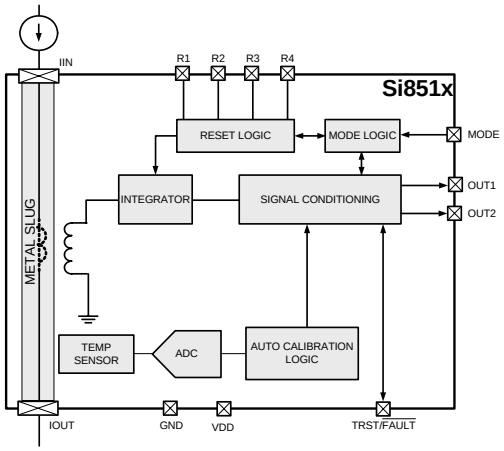
Applications

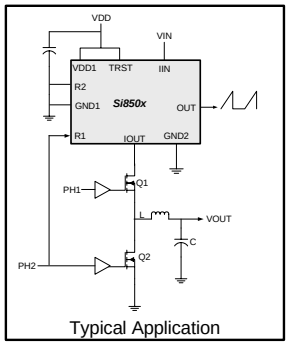
- Power supplies
- Motor controls
- Lighting equipment
- Industrial equipment

Description

The Si85xx products are unidirectional ac current sensors available in full-scale ranges of 5, 10, and 20 A. Si85xx products are ideal upgrades for older current-sensing technologies offering size, performance and cost advantages over current transformers, Hall effect devices, DCR circuits and other approaches. The Si85xx are extremely low loss, adding less than 1.3 mΩ of series resistance and less than 2 nH series inductance in the sensing path at 25 ºC. Current-sensing terminals are isolated from the other package pins to a maximum voltage of 1,000 VDC.

Functional Block Diagram

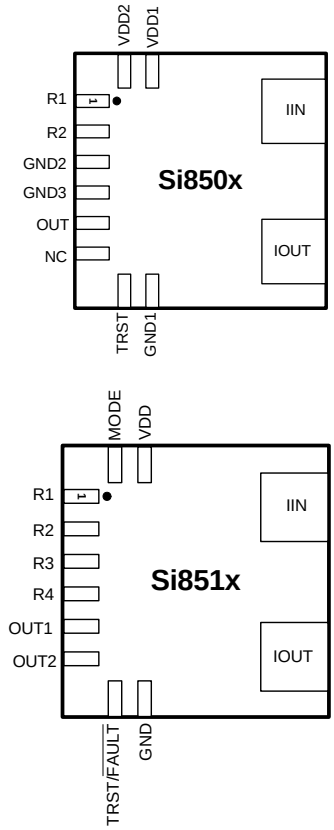




Typical Application

Pin Assignments:
See page 20

12-Pin QFN



Patents pending

TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Electrical Specifications

TA = –40 to +85 ºC (typical specified at 25 ºC), VDD = 2.7 to 5.5 V

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage (V_{DD})		2.7	—	5.5	V
Supply Current	Fully enabled, input frequency = 1 MHz	—	4	7	mA
Undervoltage Lockout (V_{UVLO})		2.1	2.3	2.5	V
Undervoltage Lockout Hysteresis (V_{HYST})		—	100	—	mV
Logic Input HIGH Level	MODE, R1, R2, R3, R4 inputs (TTL compatible)	2.0	—	—	V
Logic Input LOW Level		—	—	0.8	V
Reset Time (t_R)		250	—	—	ns
R1, R2, R3, R4 Input Rise Time (t_{RR})		—	—	30	ns
R1, R2, R3, R4 Input Fall Time (t_{FR})		—	—	30	ns
Measurement Watchdog Timeout (t_{WD})		30	50	80	µs
Series Input Resistance	Measured from IIN to IOUT	—	1.3	—	mΩ
Series Inductance	Measured from IIN to IOUT	—	2	—	nH
Input/Output Delay	OUT, OUT1, OUT2 delay relative to input	—	50	100	ns
Start-Up Self-Cal Delay (t_{CAL})	Time from VDD = V_{UVLO} + V_{HYST} to cal complete	—	150	200	µs
Input Common Mode Voltage Range		—	—	1,000	V
Operating Input Frequency Range (f)		50	—	1,200	kHz
DC Power Supply Rejection Ratio		—	80	—	db
Sensitivity	Si85x1/4/7	—	400	—	mV/A
	Si85x2/5/8	—	200	—	mV/A
	Si85x3/6/9	—	100	—	mV/A
OUT, OUT1, OUT2 Offset Voltage (V_{OUTMIN})	Current flow from I_{IN} to I_{OUT} = 0	—	10	—	mV
VOUT Slew Rate	OUT, OUT1, OUT2 load = 5K || 50 pF	—	50	—	V/µs
OUT, OUT1, OUT2 Output Resistance		20		30	Ω
Measurement Error (%)—all devices (–40 to 85 ºC Temp Range)	5 to 10% of full scale	–20	—	+20	%
	10 to 20% of full scale	–10	—	+10	%
	20 to 100% of full scale	–5	—	+5	%

Table 1. Electrical Specifications (Continued)

TA = –40 to +85 ºC (typical specified at 25 ºC), VDD = 2.7 to 5.5 V

Parameter	Conditions	Min	Typ	Max	Unit
Measurement Error (%)—all devices (–40 to 125 ºC Temp Range)	5 to 10% of full scale	–30	—	+30	%
	10 to 20% of full scale	–25	—	+25	%
	20 to 100% of full scale	–20	—	+20	%

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Storage temperature	T_{STG}	–65		+150	ºC
Ambient temperature under bias	T_A	–40		+125	ºC
Supply voltage	V_{DD}			5.75	V
Voltage on any pin with respect to ground (not including IIN, IOUT)	V_{IN}	–0.5		VDD + 0.5	V
Lead solder temperature (10 sec.)	-			260	ºC
DC isolation	-			1000	VDC

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Functional Overview

The Si85xx AC Current Sensor family of products mimic the functionality of a traditional current transformer (CT) circuit with burden resistor, diode and output filter, but offers enhanced performance and added capabilities. These devices use inductive current sensing and on-board signal conditioning electronics to generate a 2 V full-scale output signal proportional to the ac current flowing from the IIN to the IOUT terminals. As shown in Figure 1 and Figure 2, current flowing through the metal package slug induces a signal in the pickup coil on-board the Si85xx die. This signal is applied to the input of an integrator that re-constructs the ac current flowing from IIN to IOUT. On-board circuitry provides cycle-by-cycle integrator reset, and temperature and offset voltage compensation to achieve measurement accuracy to within ±5%.

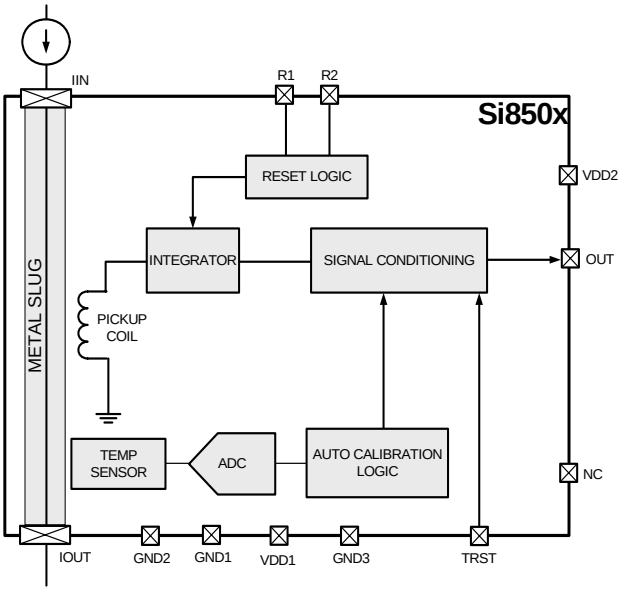


Figure 1. Si850x (Single Output) Block Diagram

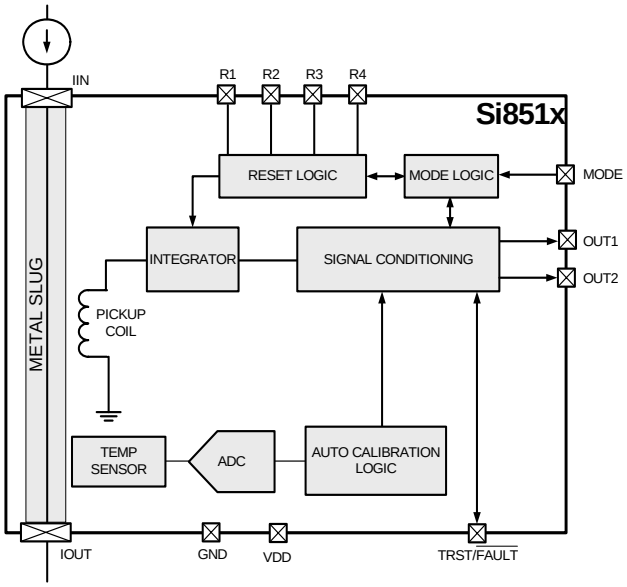


Figure 2. Si851x (Ping Pong Output) Block Diagram

The Si85xx is superior to other current sensing approaches and benefits the system in a number of ways:

- **Small size:** With its 4x4 mm footprint and 1 mm height, the Si85xx is among the smallest current sensors available.
- **Large output signal:** The 2.0 V full-scale output swing offers superior noise immunity versus other current sensing technologies.
- **Low loss:** The Si85xx adds only 1.3 mΩ (at 25 °C) to the sensing path making it one of the lowest loss current sensors available. Low 2 nH primary series inductance is 2,000 times lower compared to a CT, and results in significantly less ringing.
- **High precision:** The Si8501/2/3 versions are available with a max error of ±5% of reading; one of the highest accuracy current sensors available.
- **Ping-Pong output mode (Si851x):** Alternately routes the current measurements from each side of a full-bridge circuit to separate output pins for comparison, which is very useful for transformer flux balancing applications. Eliminates a second CT in a full-bridge application.
- **Leading edge noise suppression:** Filters out reflected noise due to long reverse recovery time of output rectifier. Eliminates the need for external leading edge blanking circuit.
- **High common mode voltage:** The Si85xx offers up to 1,000 VDC of isolation making it useful over a very wide voltage range.

- **$\overline{\text{FAULT}}$ output (Si8517/8/9):** goes low when external reset timing is in error.
- **Ease-of-use:** Other than conventional power and grounding techniques, no special board layout considerations are required. Built-in timing interface circuits allow already available system switching signals to be used for reset—no external circuits required.

2.1. Under Voltage Lockout (UVLO)

UVLO is provided to prevent erroneous operation during device start-up and shutdown, or when VDD is significantly below specified operating range. The Si85xx is in UVLO state when VDD ≤ V_{UVLO} (Figure 3). During UVLO, the output(s) are held at minimum value regardless of the amount of current flowing from IIN to IOUT and signals on integrator reset inputs R1-R4 are ignored. The Si85xx exits UVLO when VDD ≥ (V_{UVLO} + V_{HYST}).

2.2. Device Start-Up

Upon exit from UVLO, the Si85xx performs a voltage offset and temperature self-calibration cycle. During this time, output(s) are held at minimum value and reset inputs (R1-R4) are ignored. The reset inputs are enabled at the end of the self-calibration cycle, and an integrator reset cycle is initiated on the first occurrence of active signals on R1-R4. A current measurement is initiated immediately after the completion of the integrator reset cycle, and the resulting current waveforms appear on the output pins. This "reset-measure-reset" pattern repeats throughout steady-state operation.

2.3. Integrator Reset and Current Measurement

The Si85xx measures current flowing from the IIN to IOUT terminals. Current is allowed to flow in the opposite direction, but will not be measured (OUT1 and OUT 2 remain at their minimum values during reverse current flow. Reverse current flow will not damage the Si85xx).

To achieve specified accuracy, the integrator capacitor must be discharged (reset) for time period t_R prior to the start of every measurement cycle. This cycle-by-cycle reset is implemented by connecting existing system gate control signals to the R1–R4 inputs in a way that resets the integrator when no current is flowing from IIN to IOUT. To achieve rated accuracy, the reset cycle must be completed prior to the start of the measurement cycle. For maximum flexibility, integrator reset operation can be configured in one of two ways:

Option 1: The start and duration of reset is determined by the states of the timing signals applied to R1-R4.

Option 2: The timing signals applied to R1-R4 trigger the start of reset, and the duration of the reset is determined by an on-board programmable reset timer.

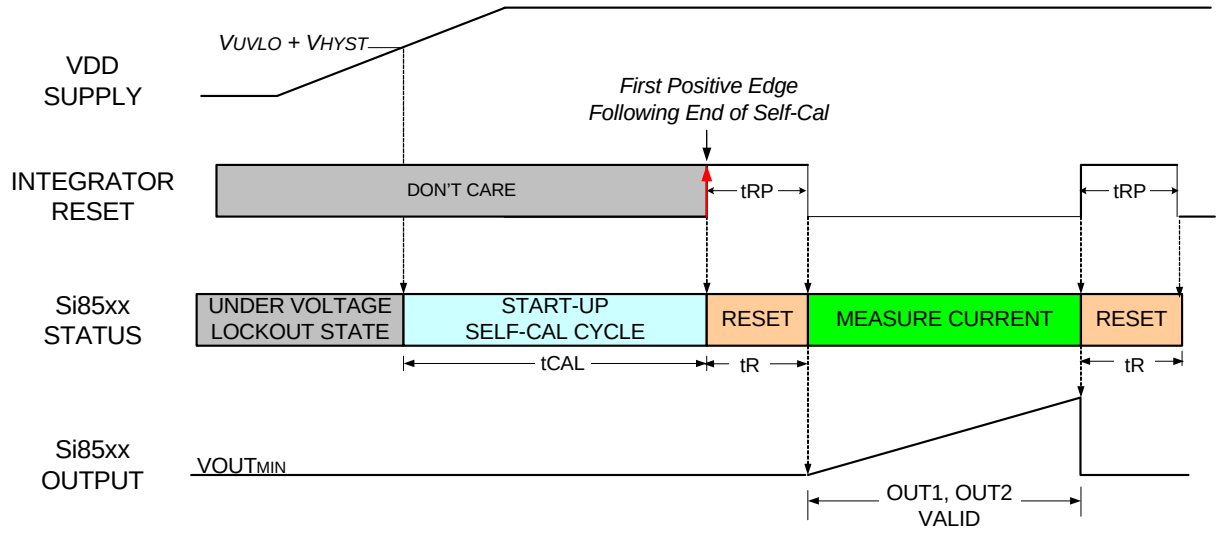


Figure 3. Si85xx Startup and Control Timing

Integrator reset option 1 is selected by connecting T_{RST} to VDD. In this mode, the Si85xx is held in reset as long as the signals on R1-R4 satisfy the logic equations of Tables 3 and 4. It is typically used in applications where the gate drivers are external to the system controller I.C. (the gate driver delay ensures reset is completed prior to the start of measurement).

Reset option 2 is selected by connecting a timing resistor (R_{TRST} in Figure 4) from the TRST input to ground. It is typically used in applications where the gate drivers are on-board the controller. In this mode, the on-chip reset timer is triggered when the signals on R1-R4 satisfy the logic equations of Tables 3 and 4. Once triggered, the timer maintains integrator in reset for time duration t_R as programmed by the value of resistor R_{TRST}. The user must select the value of resistor R_{TRST} to terminate the reset cycle prior to the start of measurement under worst-case timing conditions. Note that values of t_R below the specified value in Section "1. Electrical Specifications" results in increased integrator output offset error and increased output noise on VOUT. Moreover, t_R's time is summarized by the following equation:

$$t_R = 10\ ns/k\Omega$$

where values of R_{TRST} that produce a reset time less than 200 ns ($R_{TRST} \leq 20\ k\Omega$) should not be used.

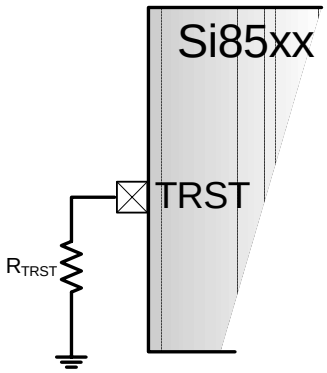


Figure 4. Programming Reset Time (t_R)

2.4. Effect of Operating Frequency on Output Accuracy

The Si85xx includes a built-in watchdog timer that disables measurement and holds OUT or OUT1 and OUT2 at their minimum values when the timer's preset limit is exceeded. This timer limits the operation of the Si85xx in dc measurement applications. As Figure 5 illustrates, the Si85xx operates down to about 10 kHz with the nominal measurement error doubling to about 10 percent.

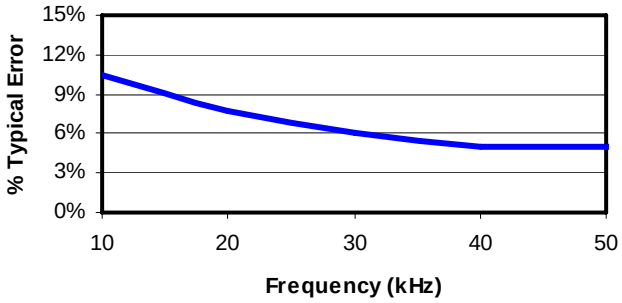


Figure 5. Full-Scale Error vs. Frequency

2.5. Effect of Temperature on Accuracy

Offset voltage present at the Si85xx output terminals (output offset voltage) is calibrated out each time VDD is applied to the Si85xx; so, its error contribution is minimized when the temperature at which calibration occurred is at or near the steady-state operating temperature of the Si85xx. For example, applying VDD at 25 °C (offset cal is performed) and operating at 85 °C will result in a larger offset error than operating at 50 ºC. The effect of this error is summarized in Figure 6. The chart is referenced to 25 °C. If the Si85xx is powered up at 25 °C and then operated at 125 °C with no auto-calibration performed (i.e., the power is not cycled at 125 °C, which causes an auto-calibration), a 3 percent measurement error can be expected.

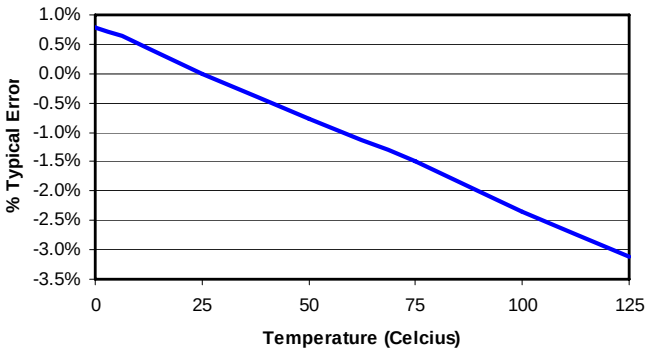


Figure 6. Differential Temperature Calibration Error

Figure 7 shows the Si85xx thermal characteristics over the temperature range of –40 to +125 ºC. Series inductance is constant at 2 nH (max) across this same temperature range.

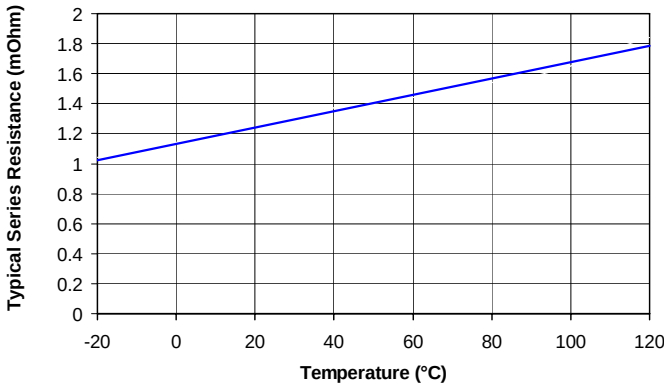


Figure 7. Series Resistance Thermal Characteristics

2.6. Leading Edge Noise Suppression

High-amplitude spikes on the leading edge of the primary switching waveforms can cause the PWM latch to be erroneously reset at the start of the switching cycle when operating in current mode control. To prevent this problem, leading edge blanking is commonly used to disable the current comparator during the early portion of the primary-side switching cycle. The Si85xx eliminates leading-edge noise spikes by including them in the signal integration. As shown in the output waveform of Figure 8, noise present in the input waveform is eliminated without the use of blanking.

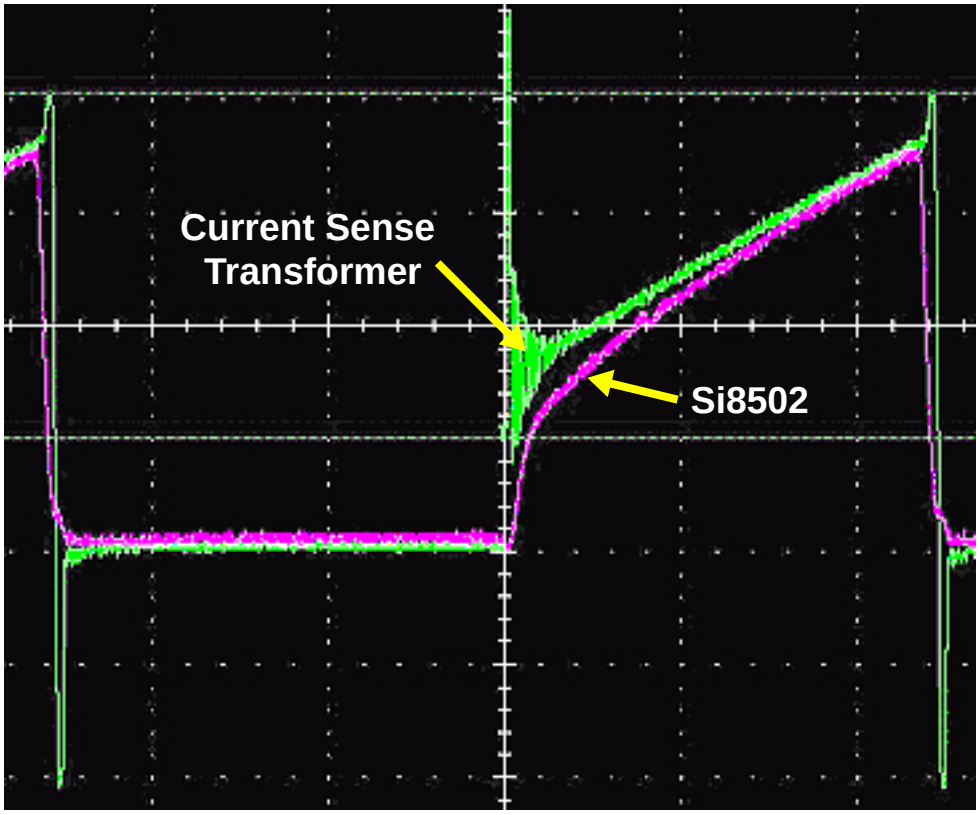


Figure 8. Leading-Edge Noise Suppression Waveforms (200 kHz, 9.3A Load)
(Si8502 waveform measured directly on OUT pin with no external filter)

2.7. $\overline{\text{FAULT}}$ Output

The $\overline{\text{FAULT}}$ output (Si8517/8/9) guards against Si85xx output signal errors caused by missing reset cycles. $\overline{\text{FAULT}}$ is asserted when a measurement cycle exceeds the internal watchdog timer times limit of t_{WD}. $\overline{\text{FAULT}}$ can be used to alert a local microcontroller or digital power controller of a current sense failure, or initiate a system shutdown. To detect faults, tie a 200 kΩ resistor from TRST/$\overline{\text{FAULT}}$ to VDD.

3. Application Information

3.1. Board Layout

The Si85xx is connected in the series path of the current to be measured. The Si85xx must be located as far away from away from transformer and other magnetic field sources as possible. Like other analog components, the Si85xx should be powered from a low-noise DC source, and preferably connected to a low noise analog ground plane. Recommended bypass capacitors are 1 µF in parallel with a 0.1 µF, positioned as close to the Si85xx as possible. *When using the Si850x (single output versions), all 3 ground pins MUST be connected to the same ground point, and both VDD and VDD2 pins MUST be tied to VDD.*

3.2. Device Configuration

Configuring the Si85xx involves the following steps:

1. Selecting an output mode
2. Configuring integrator reset timing
3. Setting integrator reset time t_R

3.2.1. Device Selection

The Si85xx family offers three output modes: Single output (Si850x), and 2 and 4-Wire Ping Pong (Si851x). The Si851x products can be configured to operate in all three of these output modes.

The Si850x products operate ONLY in Single output mode. Most half-wave and single-phase applications require only Single output mode, and will typically use the Si850x. In Single output mode, output current always appears on the OUT pin (Si850x) or the OUT1 pin (Si851x). A single integrator reset signal is typically sufficient when operating in this mode.

Ping-Pong mode routes the current waveform to two different output pins on alternate measurement cycles. It is useful in full-wave and push-pull topologies where external circuitry can be used to monitor and/or control transformer flux balance. *(Note: The Applications section of this data sheet (Section 3) shows design examples using both output modes in various power topologies.)*

2-wire Ping-Pong mode is useful mainly in non-overlapping two-phase buck converters, but may also be used in full-bridge applications. In this output mode, reset inputs R1 and R2 are used, and input R3 is grounded. Measured current appears on OUT1 when R2 is high, and appears on OUT2 when R1 is high as shown in the full-bridge timing example of Figure 9.

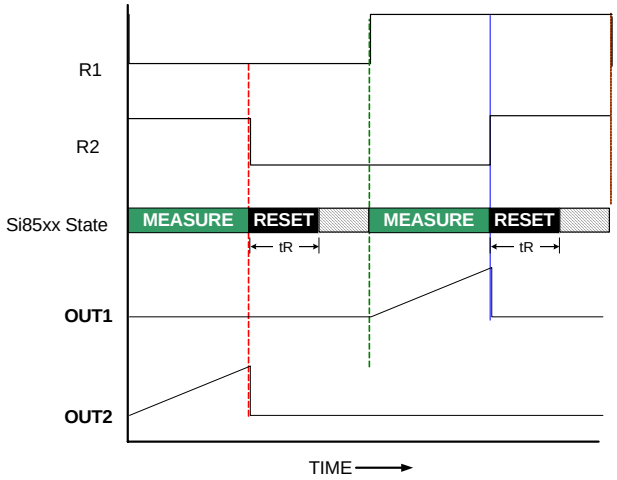


Figure 9. Full-Bridge Timing Example A

4-Wire Ping-Pong mode is recommended for full-bridge applications over 2-wire because it uses all four inputs making the reset function tolerant to single-point signal failures. In 4-Wire Ping-Pong mode, current appears on OUT2 when R1 is high and R2 is low; and appears on OUT1 when R3 is high and R4 is low as shown in the full-bridge timing example of Figure 10. Table 3 shows the states of the Mode and R4 inputs that select each output, and the resulting reset logic functions and truth tables.

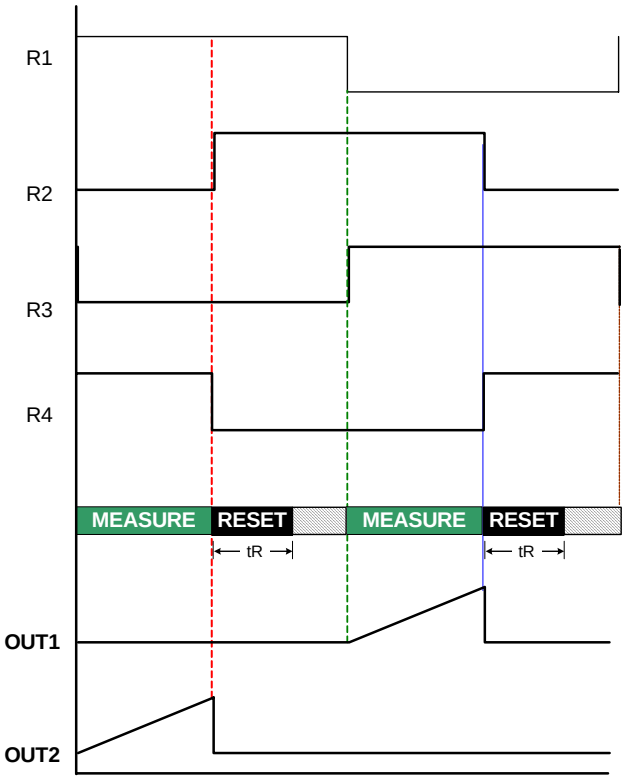


Figure 10. Full-Bridge Timing Example B

3.2.2. Selecting Reset Timing Signals

Reset timing signals should be chosen to meet the following conditions:

- Satisfy reset time t_R
- Not overlap integrator reset into the desired measurement period
- Not violate reset watchdog timeout period t_{WD}

3.2.3. Configuring Integrator Reset

Per Section “2. Functional Overview”, the integrator must be reset (zeroed) prior to the start of each measurement cycle to achieve specified measurement accuracy. This reset must be synchronized with the system switch timing signals to ensure current is measured during the appropriate time, so the Si85xx integrator reset circuitry uses system timing as its reference. Timing signals connect to reset inputs R1 through R4 where built-in logic functions allow the user to choose the conditions that cause an integrator reset event. *Important note: reset inputs R1–R4 are rated to a maximum input voltage of VDD. External resistor dividers must be used when connecting driver output signals to R1–R4 that swing beyond VDD.*

Table 3. Si850x Reset Mode Summary

Output Mode	R2	R1	Reset State*	Logic Expression
Single-Ended	0	0	0	RESET = XOR [R1, R2]
	0	1	1	
	1	0	1	
	1	1	0	
***Note:** Device is in reset when Reset State = 1.				

Table 4. Si851x Output and Reset Mode Summary

Part #	Output Mode	MODE Input	R4	R3	R2	R1	Reset State*	Logic Expression
Si850x	Single-Ended	—	—	—	0	0	0	RESET = XOR [R1, R2]
						1	1	
					1	0	1	
						1	0	
					0	0	1	
						1	0	
					1	0	1	
						1	0	
***Note:** Device is in reset when Reset State = 1.								

Table 4. Si851x Output and Reset Mode Summary (Continued)

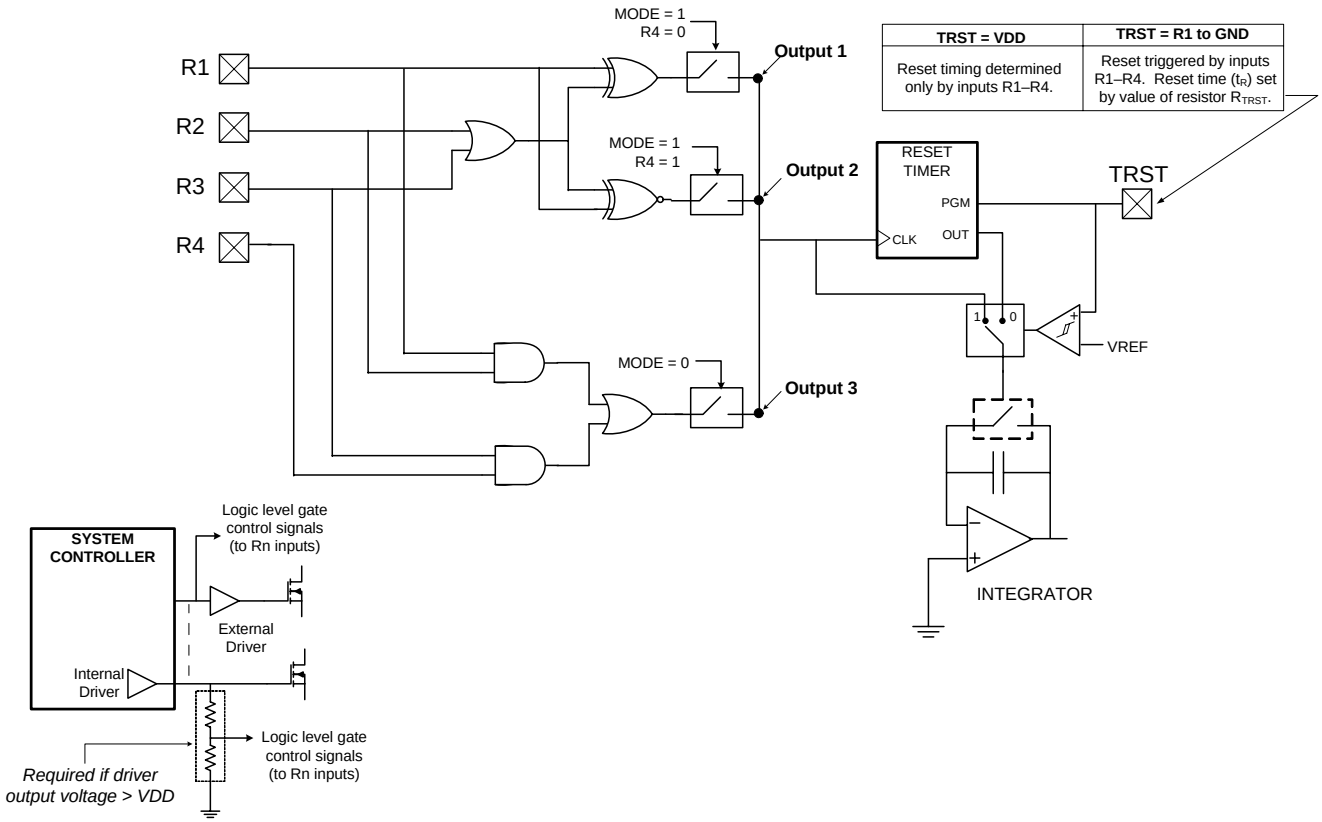
Part #	Output Mode	MODE Input	R4	R3	R2	R1	Reset State*	Logic Expression
Si851x	Single-Ended	1	0	0	0	0	0	RESET = XOR [R1, R2]
						1	1	
					1	0	1	
						1	0	
				1	0	0	1	RESET = XNOR [R1, R2]
						1	0	
					1	0	1	
						1	0	
	2-Wire Ping Pong	1	1	0	0	0	1	
						1	0	
					1	0	0	
						1	1	
	4-Wire Ping Pong	0	0	0	0	0	0	RESET = [R1 & R2] | [R3 & R4]
						1	0	
					1	0	0	
						1	1	
				1	0	0	0	
						1	0	
					1	0	0	
						1	1	
			1	0	0	0	0	
						1	0	
					1	0	0	
						1	1	
				1	0	0	1	
						1	1	
					1	0	1	
						1	1	

***Note:** Device is in reset when Reset State = 1.

As shown in Table 3, the Si850x integrator reset logic is a simple XOR gate where reset is maintained (or triggered, depending on use of the TRST input) when states of reset inputs R1 and R2 are not equal.

Figure 11 shows the logic for the Si851x products, where any one of three reset logic functions can cause integrator reset. The output mode (Si851x) is determined by the states of the Mode and R4 inputs, as shown in Table 4.

As explained in Section 2.3, the signals applied to R1-R4 can control integrator reset in real time (option 1), or can trigger a reset event of programmable duration (option 2). Referring to Figure 11, reset timing is exclusively a function of the signals applied to R1-R4 when TRST is tied to VDD. If not connected to VDD, the reset timer is enabled and TRST MUST be connected through a resistor to ground to set the reset duration (t_R). Note the reset timer is retriggerable, and generates a timed integrator discharge pulse whenever the reset logic output transitions from low to high.



TRST = VDD	TRST = R1 to GND
Reset timing determined only by inputs R1–R4.	Reset triggered by inputs R1–R4. Reset time (t_R) set by value of resistor R_{TRST}.

Figure 11. Si851x Integrator Reset Logic

3.2.4. Setting Reset Time t_R

The programmable reset timer is triggered when the states of the signals applied to R1–R4 cause the associated logic expression (Tables 3 and 4) to go high (transition to the TRUE state). Because this timer is re-triggerable, R1–R4 must remain TRUE for the duration of the desired t_R as shown in Figure 12. Should R1–R4 transition FALSE during t_R, integrator reset will be immediately halted resulting in lower measurement accuracy due to higher integrator offset error.

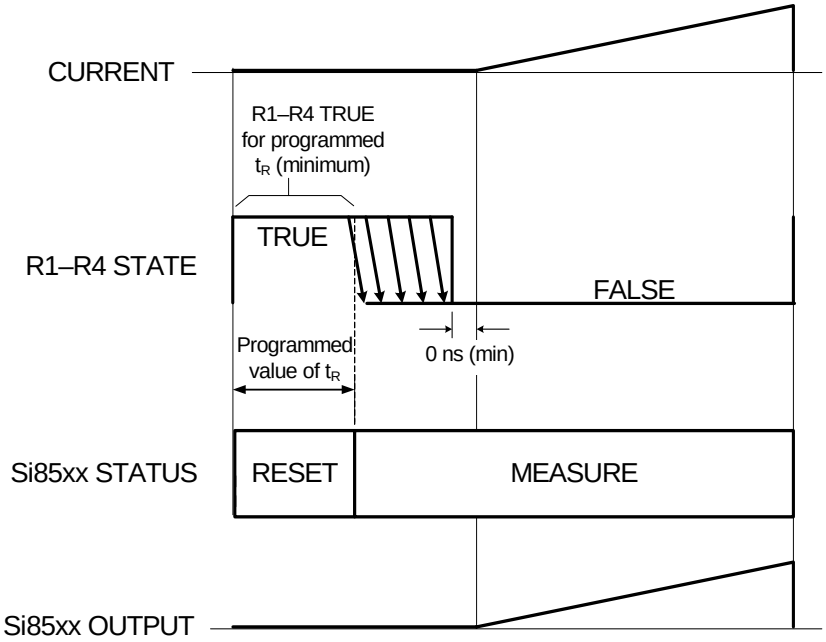


Figure 12. Correct t_R Programming Using Resistor from TRST Input to Ground

3.2.5. Measurement Watchdog Timer and $\overline{\text{FAULT}}$ Output

A built-in watchdog timer disables measurement and holds OUT or OUT1 and OUT2 at their minimum values when the time between integrator resets exceeds t_{WD}. The output signal from this watchdog is available on the $\overline{\text{FAULT}}$ output pin (Si8517/8/9 only).

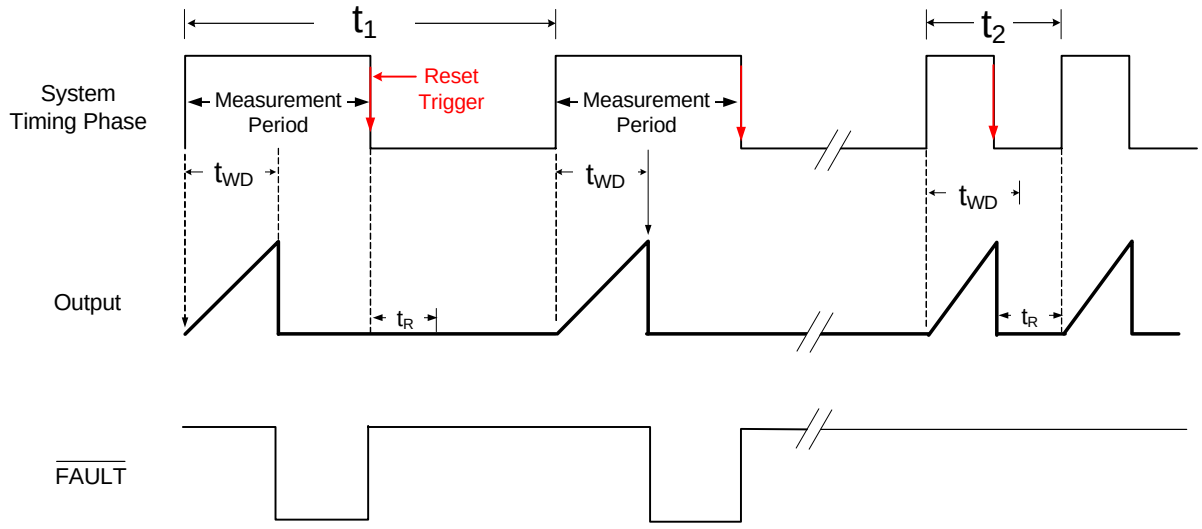


Figure 13. Measurement Watchdog Timer Operation

As shown in Figure 13, the time between integrator resets for system timing phase t_1 is greater than watchdog period t_{WD}. As a result, measurement occurs until t_{WD} is exceeded, at which time the output is immediately forced to minimum value and $\overline{\text{FAULT}}$ transitions low. Further measurements are inhibited until the application of another integrator reset, which also resets the watchdog driving $\overline{\text{FAULT}}$ high, and enables another measurement cycle. This process continues until t_{WD} is no longer violated, as shown in period t_2 where normal operation is restored. The current measurements made in period t1 will have reduced accuracy versus those made within the specified operating frequency range.

3.3. Single-Phase Buck Converter Example

In this example, the Si850x is configured to operate in a single-phase synchronous buck converter (Figure 14). This converter has a PWM frequency of 1 MHz, and a maximum duty cycle of 80%.

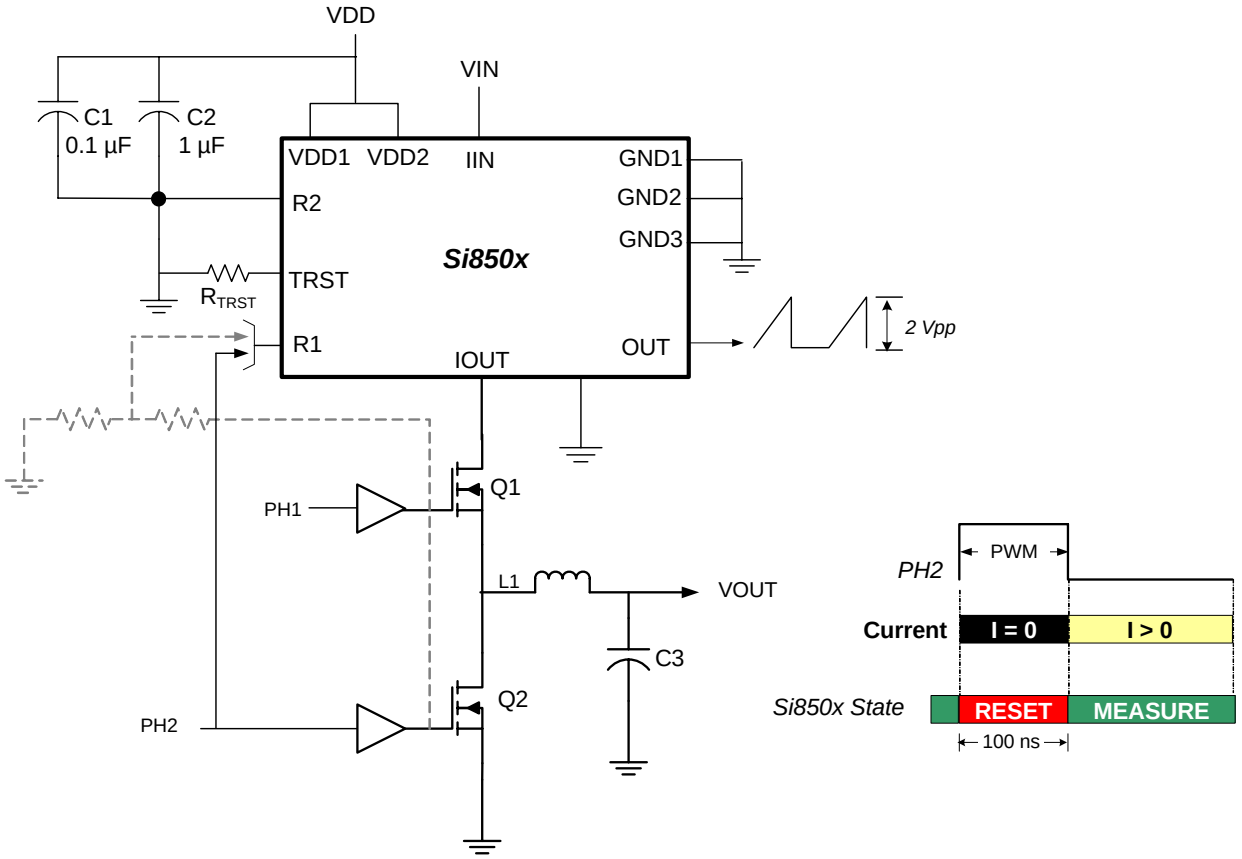


Figure 14. Si850x Single-Phase Buck Converter

This is an example of a half-wave application that can be addressed with Single-Ended output mode. The PWM period is calculated to be $1/10^{-6}$ = 1.0 µs, and the worst-case value t_R is 0.2 x 1.0 x 10^{-6} = 200 ns at 80% maximum duty cycle (R_{TRST} = 20 kΩ). In this example, the current measurement is made when the buck switch is on, so PH2 is chosen as the reset signal by connecting PH2 to R1 and grounding the R2 and R3. The PH2 signal can be obtained at the input of the driver external to the PWM controller, or the output of the controller's internal driver (through a resistor divider if the driver output swings beyond the device VDD range).

3.4. Full-Bridge Converter Example

The full-bridge circuit of Figure 15 uses an Si851x configured in 4-Wire Ping-Pong output mode. The switching frequency of this phase-shifted full-bridge is 150 kHz, and the maximum control phase overlap is 70%.

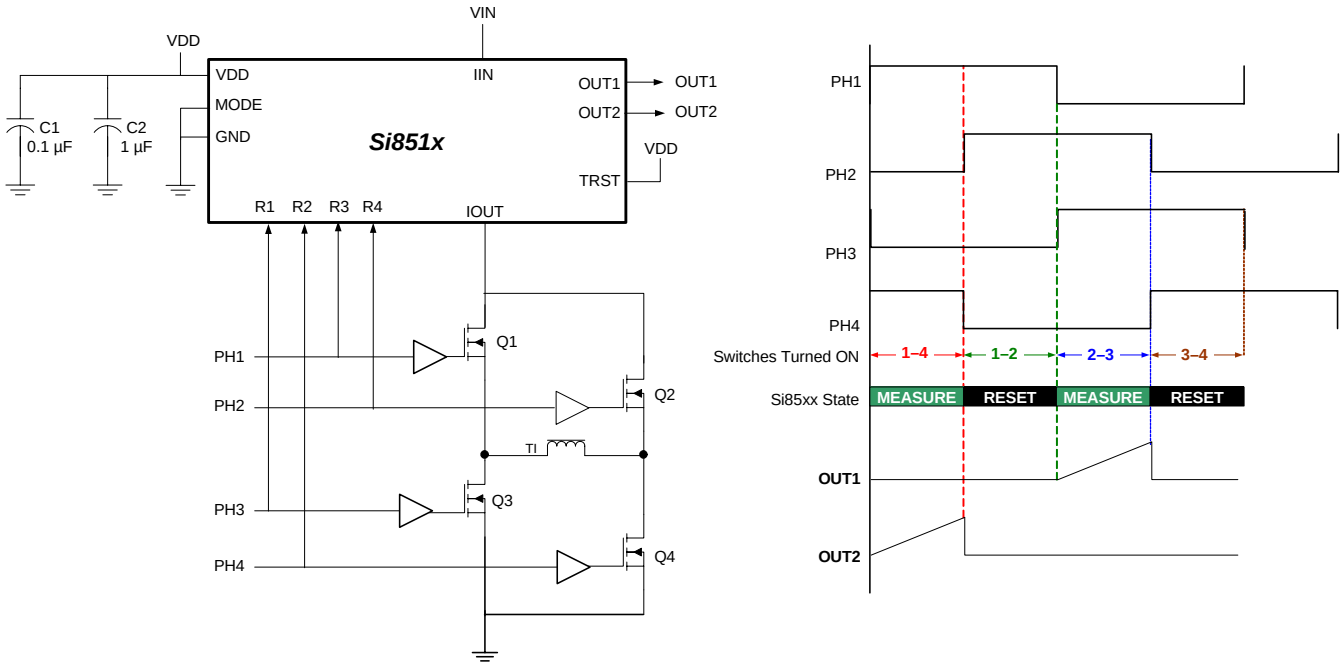


Figure 15. Full-Bridge Converter

Given the 150 kHz switching frequency (duty cycle fixed at 50%), the equivalent period is $1/150 \times 10^3 = 6.6$ µs. At 70% maximum overlap, this equates to a worst-case t_R value of is $0.3 \times 6.6 \times 10^{-6} = 1.98$ µs; the default value for t_R can therefore be used, and is selected by connecting TRST to VDD. As shown in the timing diagram of Figure 15, integrator reset occurs when current circulates between Q1 and Q2, and between Q3 and Q4 (i.e. when current is not being sourced from VIN). The external driver delay ensures reset is complete prior to the start of measurement.

3.5. Push-Pull Converter Example

The Push-Pull converter of Figure 16 uses 2-Wire Ping Pong output mode. As shown in the timing diagram, the integrator reset occurs when the inputs of both the PH1 and PH2 drivers are low. As shown, TRST is connected to VDD, selecting the default value of t_R (250 ns). Assuming an 80% maximum duty cycle, this value of t_R would deliver specified accuracy over a PWM frequency range of 50 to 400 kHz. Frequencies above 400 kHz would require the selection of a lower t_R value by connecting a resistor from TRST to ground.

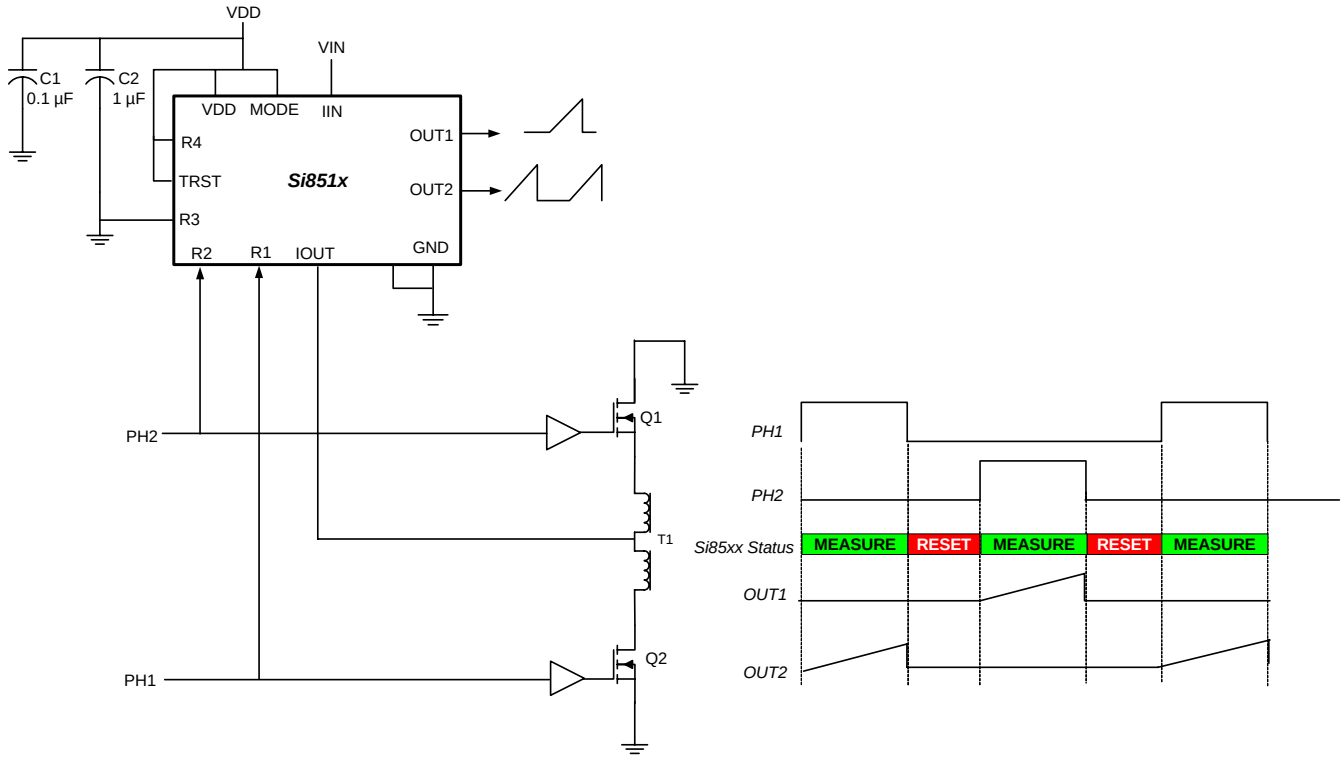


Figure 16. Push-Pull Example Using Default t_R Value

4. Pin Descriptions—Si85xx

12-Pin QFN

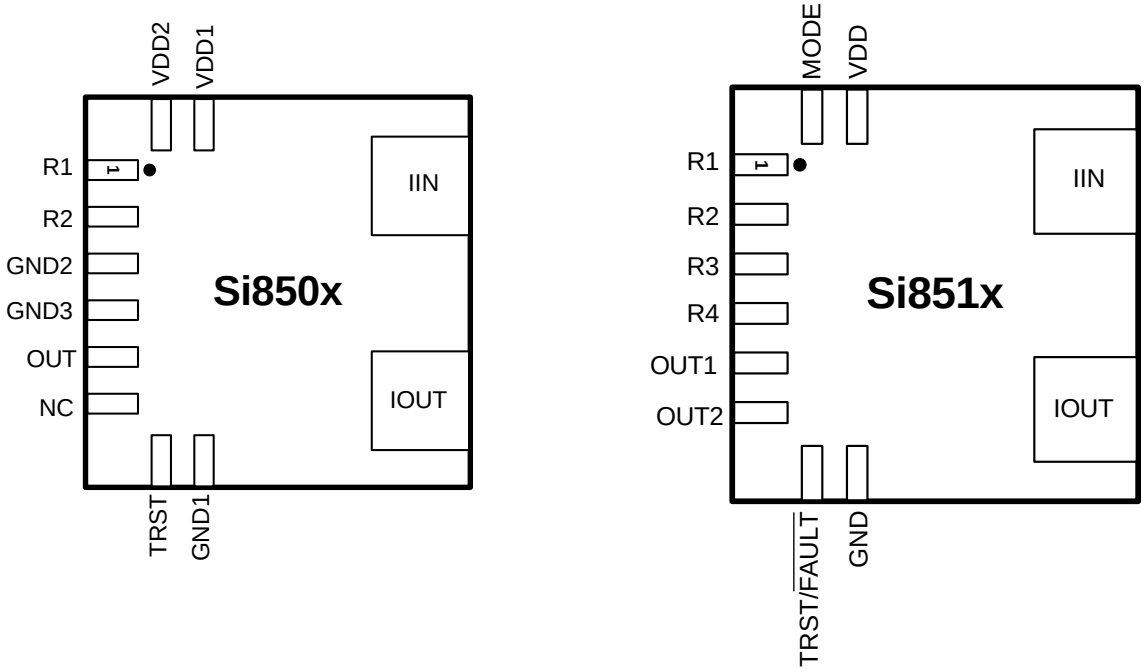


Figure 17. Example Pin Configurations

Table 5. Si85xx Family Pin Descriptions

Pin#	Si850x Pin Name	Description	Si851x Pin Name	Description
1	R1	Integrator reset input 1	R1	Integrator reset input 1
2	R2	Integrator reset input 2	R2	Integrator reset input 2
3	GND2	Ground	R3	Integrator reset input 3
4	GND3		R4	Integrator reset input 4
5	OUT	Output	OUT1	Output in single-ended output mode, or one of two outputs in Ping-Pong mode.
6	NC	No connect	OUT2	Second of two Ping-Pong mode outputs
7	TRST	Reset time control	TRST	Reset time control
8	GND1	Ground	GND	Ground
9	IOUT	Current output terminal	IOUT	Current output terminal
10	IIN	Current input terminal	IIN	Current input terminal
11	VDD1	Power supply input	VDD	Power supply input
12	VDD2		MODE	Mode control input

5. Ordering Guide

P/N	Full Scale Current (A)	Full Scale Error (% of Reading)	Temp Range (°C)	Pin 7 Function	Output Mode	Package
Si8501-B-GM	5	±5	–40 to +85	Integrator Reset Time Programming Input	Single	4x4 mm QFN
Si8502-B-GM	10					
Si8503-B-GM	20					
Si8504-B-IM	5	±20	–40 to +125	Integrator Reset Time Programming Input		
Si8505-B-IM	10					
Si8506-B-IM	20					
Si8511-B-GM	5	±5	–40 to +85	Integrator Reset Time Programming Input	Ping-Pong	
Si8512-B-GM	10					
Si8513-B-GM	20					
Si8514-B-IM	5	±20	–40 to +125	Integrator Reset Time Programming Input		
Si8515-B-IM	10					
Si8516-B-IM	20					
Si8517-B-GM	5	±5	–40 to +85	$\overline{\text{FAULT}}$ Output		
Si8518-B-GM	10					
Si8519-B-GM	20					

Note: All packages are Pb-free and RoHS compliant. Moisture Sensitivity level is MSL2 with peak reflow temperature of 260 ºC according to the JEDEC industry classification, and peak solder temperature.

6. Package Outline—12-Pin QFN

Figure 18 illustrates the package details for the Si85xx. Table 6 lists the values for the dimensions shown in the illustration.

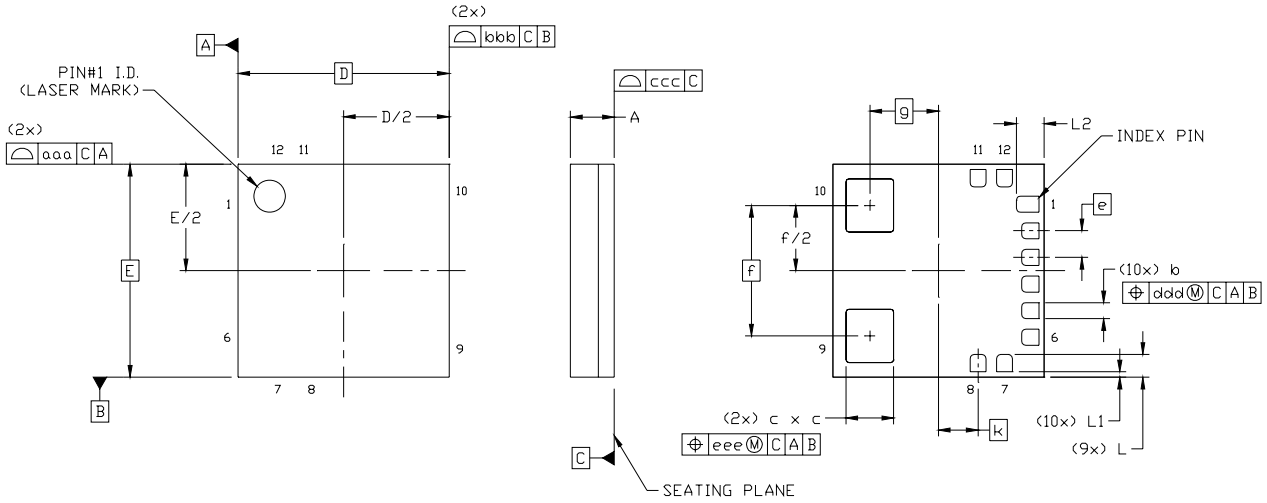


Figure 18. 12-Pin QFN Package Diagram

Table 6. QFN-12 Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
b	0.25	0.30	0.35
c	0.85	0.90	0.95
D	4.00 BSC.		
e	0.50 BSC.		
E	4.00 BSC.		
f	2.45 BSC.		
g	1.30 BSC.		
k	0.75 BSC.		
L	0.35	0.40	0.45
L1	0.03	0.05	0.08
L2	0.45	0.50	0.55
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.05
eee	—	—	0.05

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: PowerProducts@silabs.com
Internet: www.silabs.com