PI74FCT646T/648T/651T/652T
(25Ω Series PI74FCT2646T/2652T

Fast CMOS Octal Registered Transceivers

Product Features:

- PI74FCT646T/648T/651T/652T/2646T/2652T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 24-pin 300 mil wide plastic DIP (P)
  – 24-pin 150 mil wide plastic QSOP (Q)
  – 24-pin 150 mil wide plastic TQSOP (R)
  – 24-pin 300 mil wide plastic SOIC (S)
- Device models available upon request

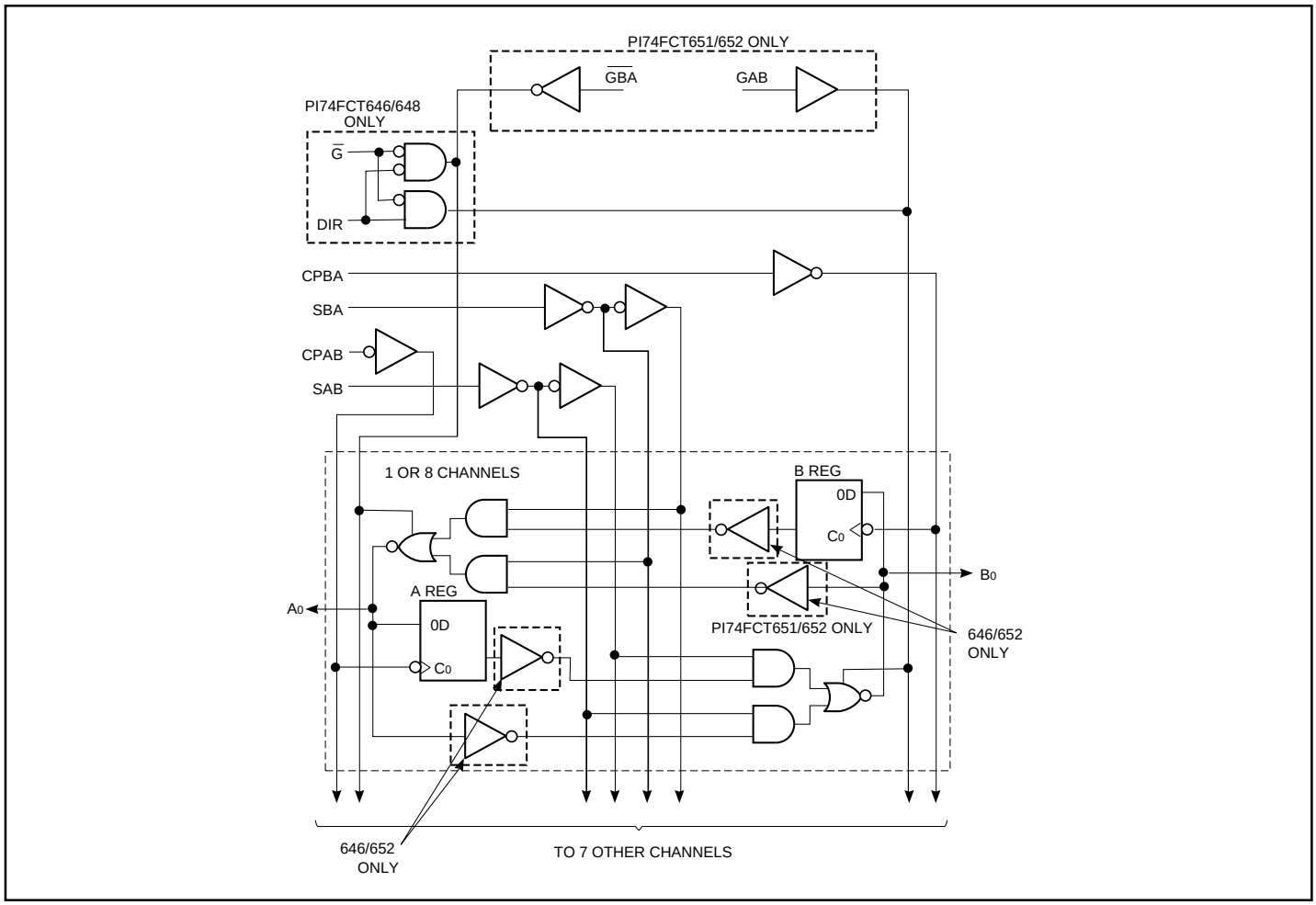
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6/0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25-ohm series resistor on all outputs to reduce noise because of reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT646T/648T/651T/652T and PI74FCT2646T/2652T are designed with a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The PI74FCT651/652T/2652T utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The PI74FCT646/2646T/648T utilize the enable control ($\overline{G}$) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74FCT646T is a non-inverting option of the PI74FCT648T. The PI74FCT652T is a non-inverting option of the PI74FCT651T.

Logic Block Diagram



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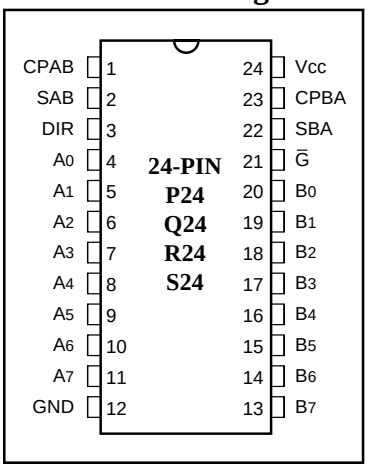
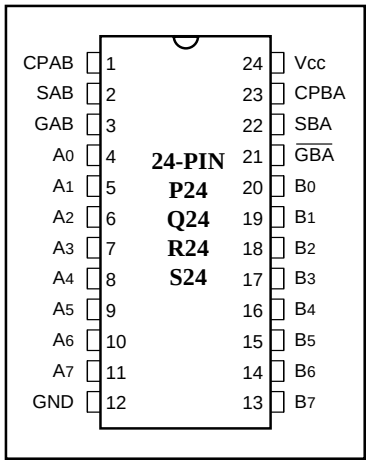
PI74FCT646/648T Product Pin Configuration



PI74FCT651/652T Product Pin Configuration



Product Pin Description

Pin Name	Description
A0-A7	Data Register A Inputs Data Register B Outputs
B0-B7	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (646/648/2646)
GAB, $\overline{GBA}$	Output Enable Inputs (651/652/2652)
GND	Ground
V_{CC}	Power

PI74FCT646/648/2646T Truth Table

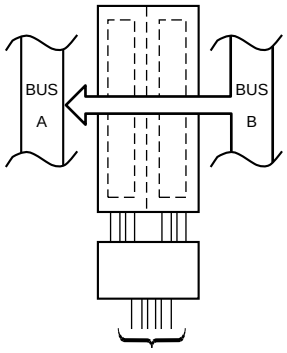
PI74FCT646/2646T	PI74FCT648T	Inputs						DATA I/O[2]	
Function/Operation	**Function/Operation**	$\overline{G}$	**DIR**	**CPAB**	**CPBA**	**SAB**	**SBA**	**A0-A7**	**B0-B7**
Isolation Store A and B Data	Isolation Store A and B Data	H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input
Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus	L L	H H	X H or L	X X	L H	X X	Input	Output

PI74FCT651/652/2652T Truth Table

PI74FCT651T	PI74FCT652/2652T	Inputs						DATA I/O[2]	
Function/Operation	**Function/Operation**	**GAB**	$\overline{GBA}$	**CPAB**	**CPBA**	**SAB**	**SBA**	**A0-A7**	**B0-B7**
Isolation Store A and B Data	Isolation Store A and B Data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B Store A in Both Registers[3]	Store A, Hold B Store A in Both Registers	X H	H H	↑ ↑	H or L ↑	X X[2]	X X	Input Input	Unspecified[1] Output
Hold A, Store B Store B in Both Registers[4]	Hold A, Store B Store B in Both Registers	L L	X L	H or L ↑	↑ ↑	X X	X X[2]	Unspecified[1] Output	Input Input
Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus	Real Time B Data to A Bus Stored B Data to A Bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus	Real Time A Data to B Bus Stored A Data to B Bus	H H	H H	X H or L	X X	L H	X X	Input	Output
Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

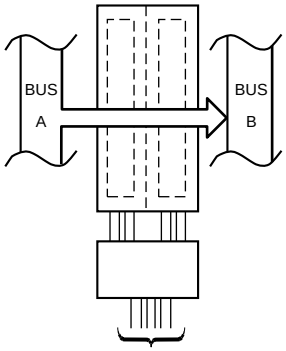
1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
3. $\overline{A}$ in B Register
4. $\overline{B}$ in A Register

REAL-TIME TRANSFER
BUS B TO A



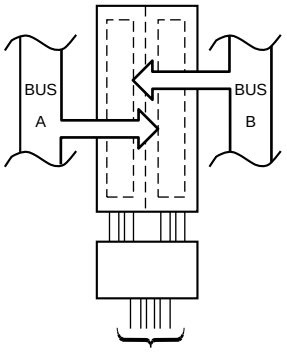
646/648/ 2646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
651/652/ 2652	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	L	L	X	X	X	L

REAL-TIME TRANSFER
BUS A TO B



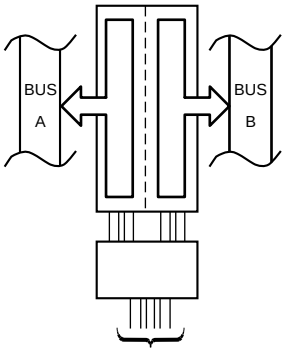
646/648/ 2646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X
651/652/ 2652	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	H	H	X	X	L	X

STORAGE FROM
A AND/OR B



646/648/ 2646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
651/652/ 2652	**GAB**	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

TRANSFER STORES
DATA TO A AND/OR B



646/648[1] 2646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
651/652/ 2652	**GAB**	**GBA**	**CPAB**	**CPBA**	**SAB**	**SBA**
	H	L	H or L	H or L	H	H

1. Note: The FCT646/2646 cannot transfer data to A bus and B bus simultaneously.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64 mA		0.3	0.55	V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA (25Ω Series)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = MAX.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current		V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.,	V_{IN} = 3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND f_I = 5 MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		1.5	3.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		2.0	5.5[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND Eight Bits Toggling f_I = 2.5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND		6.0	16.3[5]	

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT646/2646T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	646T/2646T Com. Min	646T/2646T Com. Max	646AT/2646AT Com. Min	646AT/2646AT Com. Max	646CT Com. Min	646CT Com. Max	646DT Com. Min	646DT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50 pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{G}$, DIR to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{G}$, DIR to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
t_{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width[3] HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

PI74FCT648T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	648T Com. Min	648T Com. Max	648AT Com. Min	648AT Com. Max	648CT Com. Min	648CT Com. Max	648DT Com. Min	648DT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50 pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{G}$, DIR to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{G}$, DIR to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
t_{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width[3] HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not production tested.

PI74FCT651T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	651T Com. Min	651T Com. Max	651AT Com. Min	651AT Com. Max	651CT Com. Min	651CT Com. Max	651DT Com. Min	651DT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$, GAB to Bus		2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{GBA}$, GAB to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
t_{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width[3] HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

PI74FCT652/2652T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	652T/2652T Com. Min	652T/2652T Com. Max	652AT/2652AT Com. Min	652AT/2652AT Com. Max	652CT Com. Min	652CT Com. Max	652DT Com. Min	652DT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$, GAB to Bus		2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{GBA}$, GAB to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
t_{SU}	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width[3] HIGH or LOW		6.0	—	5.0	—	5.0	—	5.0	—	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.