2.5GHz ANY DIFF. IN-TO-LVPECL PROGRAMMABLE CLOCK DIVIDER/ FANOUT BUFFER WITH INTERNAL TERMINATION

Precision Edge® SY89874U

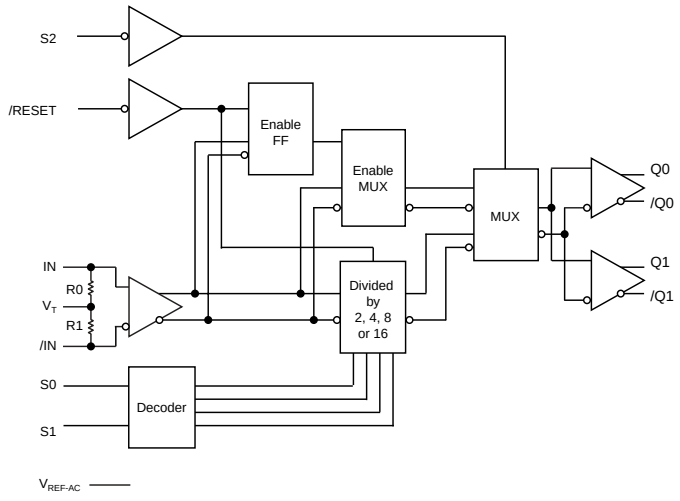
FEATURES

- Integrated programmable clock divider and 1:2 fanout buffer
- Guaranteed AC performance over temperature and voltage:
  - > 2.5GHz f_{MAX}
  - < 250ps t_r/t_f
  - < 15ps within device skew
- Low jitter design:
  - < $10ps_{PP}$ total jitter
  - < $1ps_{RMS}$ cycle-to-cycle jitter
- Unique input termination and V_T pin for DC-coupled and AC-coupled Inputs; CML, PECL, LVDS and HSTL
- TTL/CMOS inputs for select and reset
- 100k EP compatible LVPECL outputs
- Parallel programming capability
- Programmable divider ratios of 1, 2, 4, 8 and 16
- Low voltage operation 2.5V or 3.3V
- Output disable function
- –40°C to 85°C temperature range
- Available in 16-pin (3mm × 3mm) MLF® package

APPLICATIONS

- SONET/SDH line cards
- Transponders
- High-end, multiprocessor sensors

FUNCTIONAL BLOCK DIAGRAM



Precision Edge®

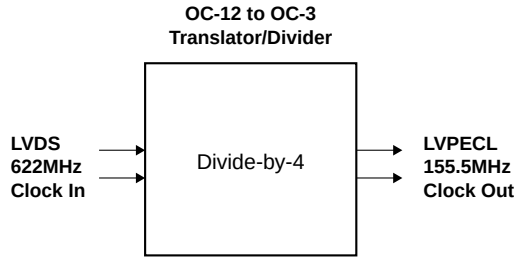
DESCRIPTION

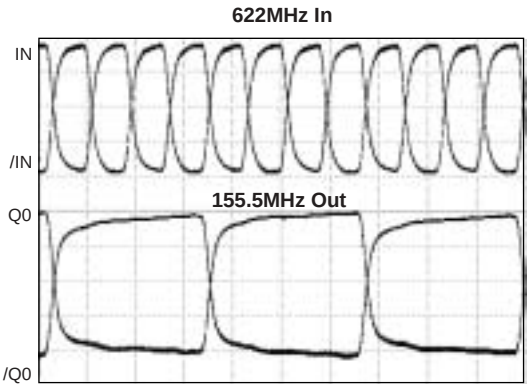
This low-skew, low-jitter device is capable of accepting a high-speed (e.g., 622MHz or higher) CML, LVPECL, LVDS or HSTL clock input signal and dividing down the frequency using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock. Available divider ratios are 2, 4, 8 and 16, or straight pass-through. In a typical 622MHz clock system this would provide availability of 311MHz, 155MHz, 77MHz or 38MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

The /RESET input asynchronously resets the divider. In the pass-through function (divide by 1) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /N).

TYPICAL PERFORMANCE





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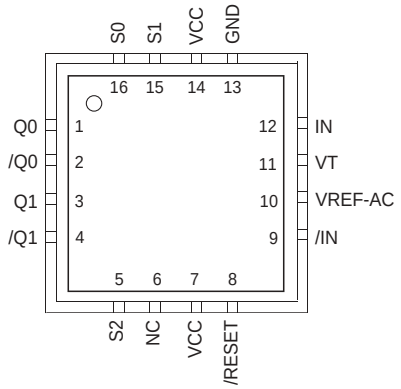
*Micro*LeadFrame and MLF are trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



16-Pin MLF® (MLF-16)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89874UMI	MLF-16	Industrial	874U	Sn-Pb
SY89874UMITR[2]	MLF-16	Industrial	874U	Sn-Pb
SY89874UMG[3]	MLF-16	Industrial	874U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89874UMGTR[2, 3]	MLF-16	Industrial	874U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
12, 9	IN, /IN	Differential Input: Internal 50Ω termination resistors to V_T input. Flexible input accepts any differential input. See "Input Interface Applications" section.
1, 2, 3, 4	Q0, /Q0 Q1, /Q1	Differential Buffered LVPECL Outputs: Divided by 1, 2, 4, 8 or 16. See "Truth Table." Unused PECL outputs may be left floating with no impact on jitter performance.
16, 15, 5	S0, S1, S2	Select Pins: See "Truth Table." LVTTL/CMOS logic levels. Internal 25kΩ pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode.) Input threshold is V_{CC}/2.
6	NC	No Connect.
8	/RESET /DISABLE	LVTTL/CMOS Logic Levels: Internal 25kΩ pull-up resistor. Logic HIGH if left unconnected. Apply LOW to reset the divider (divided by 2, 4, 8 or 16 mode). Also acts as a synchronous disable/enable function. The reset and disable function occurs on the next high-to-low clock input transition. Input threshold is V_{CC}/2.
10	VREF-AC	Reference Voltage: Equal to V_{CC}–1.4V (approx.). Used for AC-coupled applications only. Decouple the V_{REF-AC} pin with a 0.01μF capacitor. See "Input Interface Applications" section.
11	VT	Termination Center-Tap: For CML or LVDS inputs, leave this pin floating. Otherwise, see Figures 2a to 2f "Input Interface Applications" section.
7, 14	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitor.
13	GND	Ground.

TRUTH TABLE

/RESET[1]	S2	S1	S0	Outputs
1	0	X	X	Reference Clock (pass through)
1	1	0	0	Reference Clock ÷2
1	1	0	1	Reference Clock ÷4
1	1	1	0	Reference Clock ÷8
1	1	1	1	Reference Clock ÷16
0[1]	1	X	X	Q = LOW, /Q = HIGH Clock Disable

Note 1. Reset/Disable function is asserted on the next clock input (IN, /IN) high-to-low transition.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}+0.3
ECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current IN, /IN (I_{IN}) ..... ±50mA
V_T Current (I_{VT}) ..... ±100mA
V_{REF-AC} Sink/Source Current ($I_{VREF-AC}$), **Note 3** ..... ±2mA
Lead Temperature (soldering 20 sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage (V_{CC}) ..... +3.3V ±10% or +2.5V ±5%
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
  MLF® (θ_{JA})
    Still-Air ..... 60°C/W
    500lfpm ..... 54°C/W
  MLF® (ψ_{JB}), **Note 4**
    Junction-to-Board ..... 32°C/W

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Note 2. **The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.**

Note 3. **Due to the limited drive capability use for input of the same package only.**

Note 4. **Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the pcb.**

DC ELECTRICAL CHARACTERISTICS(Notes 1, 2)

T_A= –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375		3.63	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		50	75	mA
R_{IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)	**Note 3**	0.1	–	V_{CC}+0.3	V
V_{IL}	Input Low Voltage (IN, /IN)	**Note 3**	–0.3	–	V_{CC}+0.2	V
V_{IN}	Input Voltage Swing	**Notes 3, 4**	0.1	–	3.6	V
V_{DIFF_IN}	Differential Input Voltage Swing	**Notes 3, 4, 5**	0.2	–		V
$\|I_{IN}\|$	Input Current (IN, /IN)	**Note 3**	–	–	45	mA
V_{REF-AC}	Reference Voltage	**Note 6**	V_{CC}–1.525	V_{CC}–1.425	V_{CC}–1.325	V

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

Note 3. Due to the internal termination (see *"Input Structures"*) the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

Note 4. See *"Timing Diagram"* for V_{IN} definition. V_{IN} (Max) is specified when V_T is floating.

Note 5. See *"Typical Operating Characteristics"* section for V_{DIFF} definition.

Note 6. Operating using V_{IN} is limited to AC-coupled PECL or CML applications only. Connect directly to V_T pin.

(100KEP) LVPECL DC ELECTRICAL CHARACTERISTICS(Notes 1, 2)

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C, R_L = 50Ω to V_{CC} –2V; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output High Voltage		V_{CC}–1.145	V_{CC}–1.020	V_{CC}–0.895	V
V_{OL}	Output Low Voltage		V_{CC}–1.945	V_{CC}–1.820	V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing		550	800	1050	mV
V_{DIFF_OUT}	Differential Output Voltage Swing		1.10	1.60	2.10	V

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS(Notes 1, 2)

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		20	µA
I_{IL}	Input LOW Current				–300	µA

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

AC ELECTRICAL CHARACTERISTICS[Notes 1, 2]

V_{CC} = 3.3V ±10% or 2.5V ±5%; T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Output Toggle Frequency	Output Swing ≥ 400mV	2.5			GHz
	Maximum Input Frequency	Divide by 2, 4, 8, 16	3.2			GHz
t_{PD}	Differential Propagation Delay IN to Q	Input Swing < 400mV	540	650	790	ps
		Input Swing ≥ 400mV	480	600	730	ps
t_{SKEW}	Within-Device Skew (diff.) Q0–Q1	**Note 3**		7	15	ps
	Part-to-Part Skew (diff.)	**Note 3**			250	ps
t_{RR}	Reset Recovery Time	**Note 4**	600			ps
T_{jitter}	Cycle-to-Cycle Jitter	**Note 5**			1	ps_{RMS}
	Total Jitter	**Note 6**			10	ps_{PP}
t_r,t_f	Rise/Fall Time (20% to 80%)		70	150	250	ps

Note 1. Measured with 400mV input signal, 50% duty cycle, all outputs loaded with 50Ω to V_{CC}–2V, unless otherwise stated.

Note 2. Specification for packaged product only.

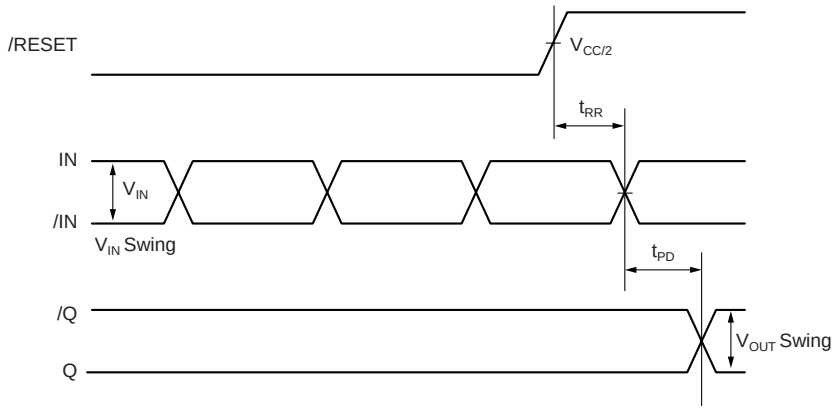
Note 3. Skew is measured between outputs under identical transitions.

Note 4. See *"Timing Diagram."*

Note 5. Cycle-to-cycle jitter definition: the variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{jitter\_cc}=T_n–T_{n+1}$, where T is the time between rising edges of the output signal.

Note 6. Total jitter definition: with an ideal clock input, of frequency ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

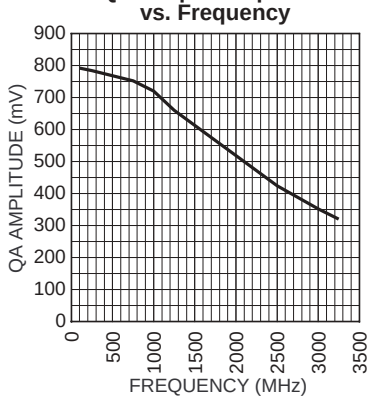
TIMING DIAGRAM



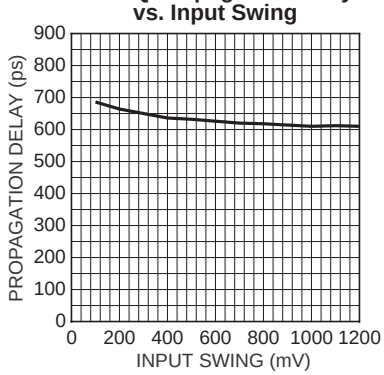
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{IN} = 400mV, T_A = 25°C, unless otherwise stated.

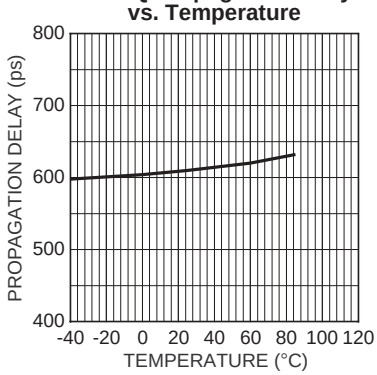
QA Output Amplitude vs. Frequency



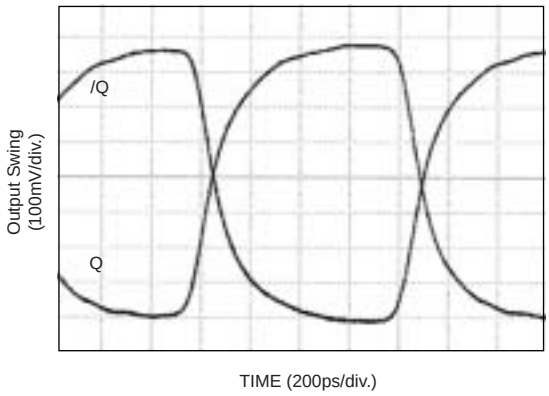
IN to Q Propagation Delay vs. Input Swing



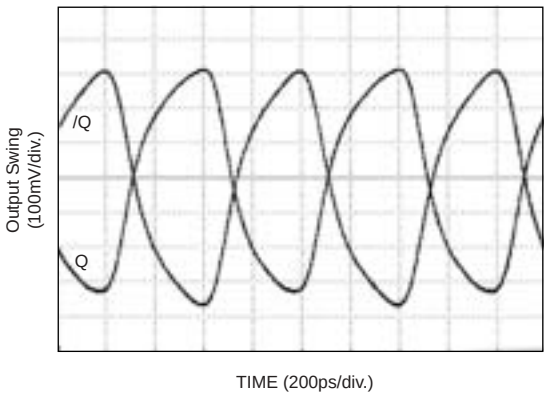
IN to Q Propagation Delay vs. Temperature



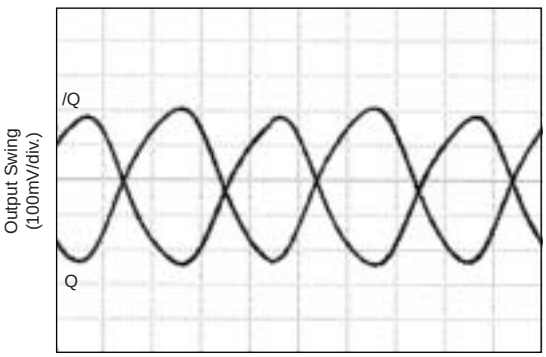
622MHz Output



1.25GHz Output



2.5GHz Output



DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

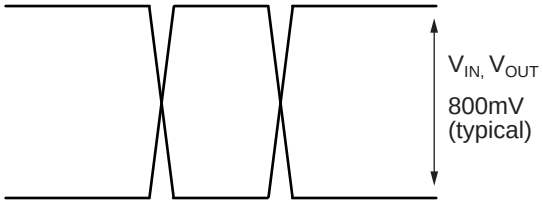


Figure 1a. Single-Ended Swing

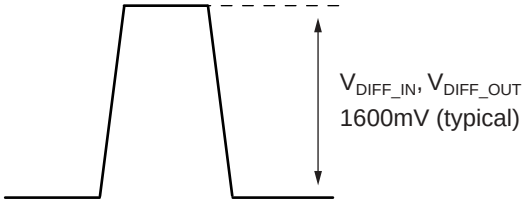


Figure 1b. Differential Swing

INPUT BUFFER STRUCTURE

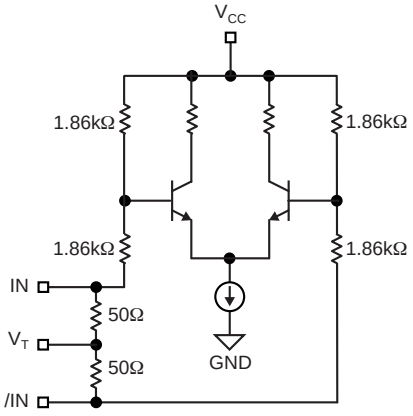


Figure 2a. Simplified Differential Input Buffer

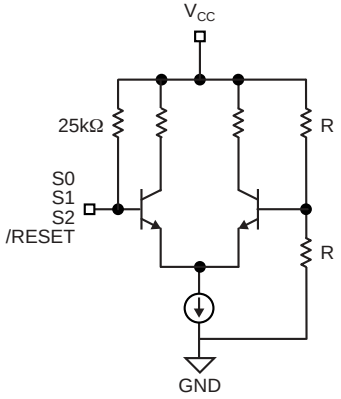


Figure 2b. Simplified TTL/CMOS Input Buffer

INPUT INTERFACE APPLICATIONS

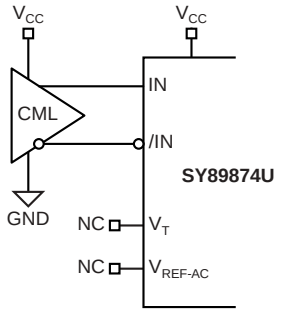


Figure 3a. DC-Coupled CML Input Interface

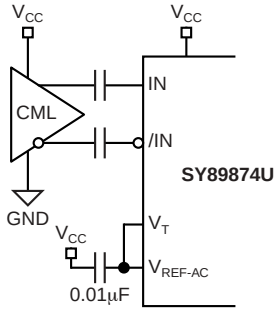


Figure 3b. AC-Coupled CML Input Interface

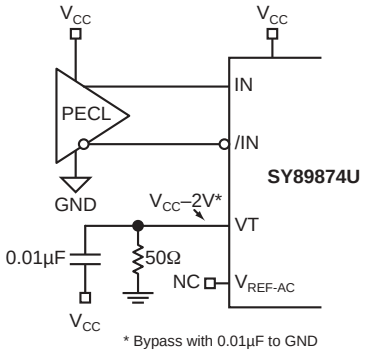


Figure 3c. DC-Coupled PECL Input Interface

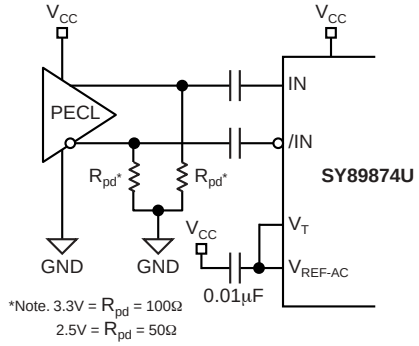


Figure 3d. AC-Coupled PECL Input Interface

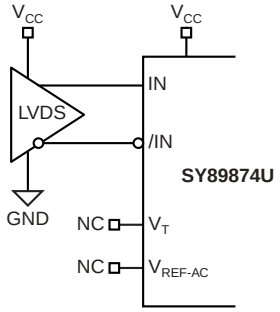


Figure 3e. LVDS Input Interface

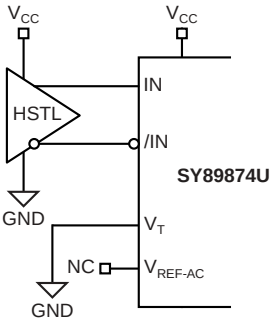


Figure 3f. HSTL Input Interface

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89871U	2.5GHz Any Diff. In-to-LVPECL Programmable Clock Divider/Fanout Buffer w/Internal Termination	http://www.micrel.com/product-info/products/sy89871u.shtml
	MLF® Application Note	http://www.amkor.com/products/notes_papers/mlf_appnote_0902.pdf
HBW Solutions	New Products and Applications	http://www.micrel.com/product-info/products/solutions.shtml

LVPECL OUTPUT TERMINATION RECOMMENDATIONS

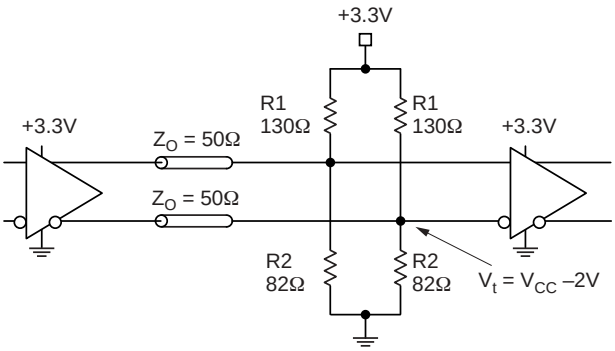


Figure 4a. Parallel Termination–Thevenin Equivalent

Note 1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω

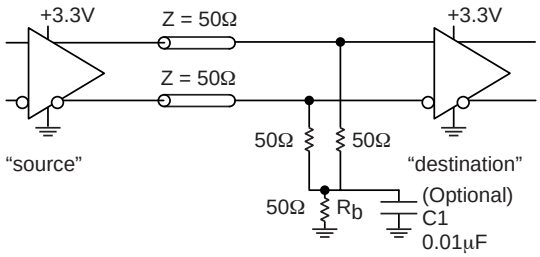


Figure 4b. Three-Resistor "Y–Termination"

Note 1. Power-saving alternative to Thevenin termination.

Note 2. Place termination resistors as close to destination inputs as possible.

Note 3. R_b resistor sets the DC bias voltage, equal to V_t. For +3.3V systems R_b = 46Ω to 50Ω. For +2.5V systems R_b = 39Ω

Note 4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

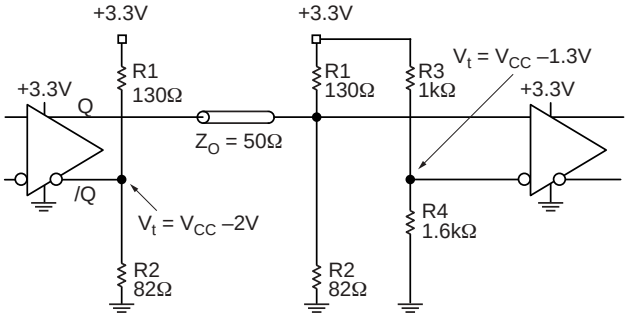
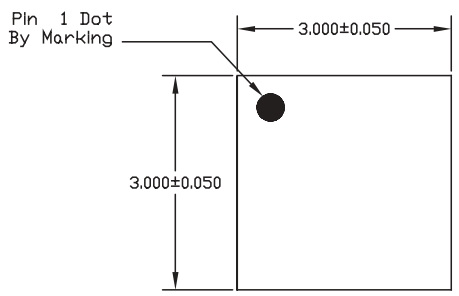


Figure 4d. Terminating Unused I/O

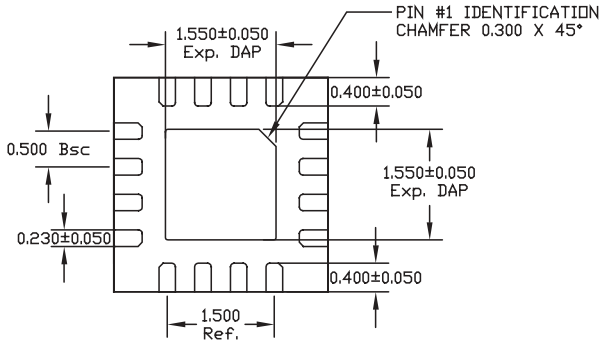
Note 1. Unused output (/Q) must be terminated to balance the output.

Note 2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.

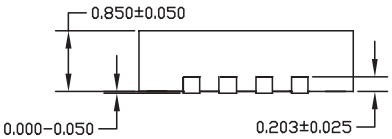
16-PIN *Micro*LeadFrame® (MLF-16)



TOP VIEW

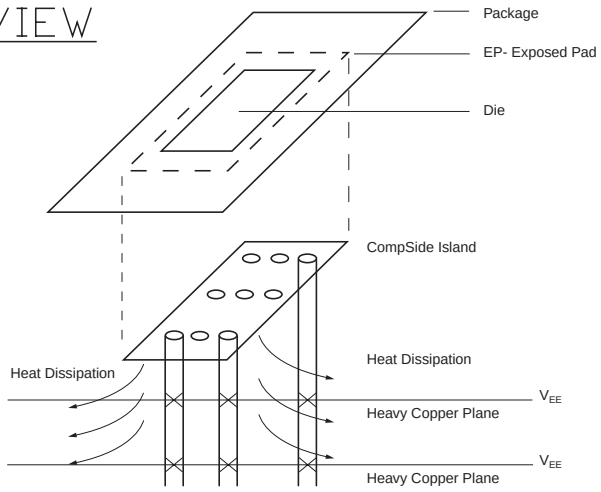


BOTTOM VIEW



SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.

Note 2. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

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