intersil™

# HFA1100/883

July 1994

## 850MHz Current Feedback Amplifier

### Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Distortion (HD3, 30MHz) . . . . . . . . . . -84dBc (Typ)**
- **Wide -3dB Bandwidth . . . . . . . . . . . . . . . 850MHz (Typ)**
- **Very High Slew Rate . . . . . . . . . . . . . . . 2300V/μs (Typ)**
- **Fast Settling (0.1%) . . . . . . . . . . . . . . . . . . . . 11ns (Typ)**
- **Excellent Gain Flatness (to 50MHz) . . . . . 0.05dB (Typ)**
- **High Output Current . . . . . . . . . . . . . . . . . . 65mA (Typ)**
- **Fast Overdrive Recovery . . . . . . . . . . . . . . <10ns (Typ)**

### Applications

- **Video Switching and Routing**
- **Pulse and Video Amplifiers**
- **Wideband Amplifiers**
- **RF/IF Signal Processing**
- **Flash A/D Driver**
- **Medical Imaging Systems**

### Description

The HFA1100/883 is a high speed, wideband, fast settling current feedback amplifier. Built with Intersil' proprietary, complementary bipolar UHF-1 process, it is the fastest monolithic amplifier available from any semiconductor manufacturer.

The HFA1100/883's wide bandwidth, fast settling characteristic, and low output impedance, make this amplifier ideal for driving fast A/D converters.

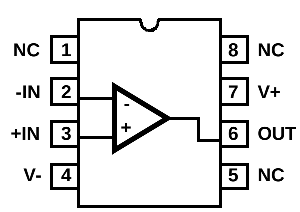
Component and composite video systems will also benefit from this amplifier's performance, as indicated by the excellent gain flatness, and 0.03%/0.05 Deg. Differential Gain/Phase specifications ($R_L = 75\Omega$).

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE |
|---|---|---|
| HFA1100MJ/883 | -55°C to +125°C | 8 Lead CerDIP |

### Pinout

**HFA1100/883**
**(CERDIP)**
TOP VIEW



## Absolute Maximum Ratings

Voltage Between V+ and V- . . . . . . . . . . . . . . . . . . . . . . . . . . . . 12V
Differential Input Voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5V
Voltage at Either Input Terminal . . . . . . . . . . . . . . . . . . . . . . V+ to V-
Output Current (50% Duty Cycle) . . . . . . . . . . . . . . . . . . . . . . ±55mA
Junction Temperature. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $+175^oC$
ESD Rating. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . < 2000V
Storage Temperature Range . . . . . . . . . . . . . . $-65^oC \le T_A \le +150^oC$
Lead Temperature (Soldering 10s). . . . . . . . . . . . . . . . . . . . $+300^oC$

## Thermal Information

| Thermal Resistance | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| CerDIP Package . . . . . . . . . . . . . . . . . | $115^oC/W$ | $30^oC/W$ |

Maximum Package Power Dissipation at $+75^oC$
CerDIP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.87W
Package Power Dissipation Derating Factor above $+75^oC$
CerDIP Package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $8.7mW/^oC$

*CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Operating Conditions

Operating $V_{SUPPLY}$ ($\pm V_S$) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±5V
Operating Temperature Range. . . . . . . . . . . . . $-55^oC \le T_A \le +125^oC$
$R_L \ge 50\Omega$

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Tested at: $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_{SOURCE} = 0\Omega$, $R_L = 100\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

| PARAMETERS | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $V_{IO}$ | $V_{CM} = 0V$ | 1 | $+25^oC$ | -6 | 6 | mV |
| | | | 2, 3 | $+125^oC, -55^oC$ | -10 | 10 | mV |
| Common Mode Rejection Ratio | CMRR | $\Delta V_{CM} = \pm2V$<br>V+ = 3V, V- = -7V<br>V+ = 7V, V- = -3V | 1 | $+25^oC$ | 40 | - | dB |
| | | | 2, 3 | $+125^oC, -55^oC$ | 38 | - | dB |
| Power Supply Rejection Ratio | PSRRP | $\Delta V_{SUPPLY} = \pm1.25V$<br>V+ = 6.25V, V- = -5V<br>V+ = 3.75V, V- = -5V | 1 | $+25^oC$ | 45 | - | dB |
| | | | 2, 3 | $+125^oC, -55^oC$ | 42 | - | dB |
| | PSRRN | $\Delta V_{SUPPLY} = \pm1.25V$<br>V+ = 5V, V- = -6.25V<br>V+ = 5V, V- = -3.75V | 1 | $+25^oC$ | 45 | - | dB |
| | | | 2, 3 | $+125^oC, -55^oC$ | 42 | - | dB |
| Non-Inverting Input (+IN) Current | $I_{BSP}$ | $V_{CM} = 0V$ | 1 | $+25^oC$ | -40 | 40 | μA |
| | | | 2, 3 | $+125^oC, -55^oC$ | -65 | 65 | μA |
| +IN Current Common Mode Sensitivity | $CMS_{IBP}$ | $\Delta V_{CM} = \pm2V$<br>V+ = 3V, V- = -7V<br>V+ = 7V, V- = -3V | 1 | $+25^oC$ | - | 40 | μA/V |
| | | | 2, 3 | $+125^oC, -55^oC$ | - | 50 | μA/V |
| +IN Resistance | $+R_{IN}$ | Note 1 | 1 | $+25^oC$ | 25 | - | kΩ |
| | | | 2, 3 | $+125^oC, -55^oC$ | 20 | - | kΩ |
| Inverting Input (-IN) Current | $I_{BSN}$ | $V_{CM} = 0V$ | 1 | $+25^oC$ | -50 | 50 | μA |
| | | | 2, 3 | $+125^oC, -55^oC$ | -75 | 75 | μA |
| -IN Current Common Mode Sensitivity | $CMS_{IBN}$ | $\Delta V_{CM} = \pm2V$<br>V+ = 3V, V- = -7V<br>V+ = 7V, V- = -3V | 1 | $+25^oC$ | - | 7 | μA/V |
| | | | 2, 3 | $+125^oC, -55^oC$ | - | 10 | μA/V |
| -IN Current Power Supply Sensitivity | $PPSS_{IBN}$ | $\Delta V_{SUPPLY} = \pm1.25V$<br>V+ = 6.25V, V- = -5V<br>V+ = 3.75V, V- = -5V | 1 | $+25^oC$ | - | 15 | μA/V |
| | | | 2, 3 | $+125^oC, -55^oC$ | - | 27 | μA/V |
| | $NPSS_{IBN}$ | $\Delta V_{SUPPLY} = \pm1.25V$<br>V+ = 5V, V- = -6.25V<br>V+ = 5V, V- = -3.75V | 1 | $+25^oC$ | - | 15 | μA/V |
| | | | 2, 3 | $+125^oC, -55^oC$ | - | 27 | μA/V |
| Output Voltage Swing | $V_{OP100}$ | $A_V = -1$, $R_L = 100\Omega$, $V_{IN} = -3.5V$ | 1 | $+25^oC$ | 3 | - | V |
| | | $V_{IN} = -3V$ | 2, 3 | $+125^oC, -55^oC$ | 2.5 | - | V |
| | $V_{ON100}$ | $A_V = -1$, $R_L = 100\Omega$, $V_{IN} = +3.5V$ | 1 | $+25^oC$ | - | -3 | V |
| | | $V_{IN} = +3V$ | 2, 3 | $+125^oC, -55^oC$ | - | -2.5 | V |

**TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

Device Tested at: $V_{SUPPLY}$ = ±5V, $A_V$ = +1, $R_F$ = 510Ω, $R_{SOURCE}$ = 0Ω, $R_L$ = 100Ω, $V_{OUT}$ = 0V, Unless Otherwise Specified.

| PARAMETERS | SYMBOL | CONDITIONS | | GROUP A SUBGROUPS | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| Output Voltage Swing | $V_{OP50}$ | $A_V$ = -1, $R_L$ = 50Ω | $V_{IN}$ = -3V | 1, 2 | +25°C, +125°C | 2.5 | - | V |
| | | | $V_{IN}$ = -2V | 3 | -55°C | 1.5 | - | V |
| | $V_{ON50}$ | $A_V$ = -1, $R_L$ = 50Ω | $V_{IN}$ = +3V | 1, 2 | +25°C, +125°C | - | -2.5 | V |
| | | | $V_{IN}$ = +2V | 3 | -55°C | - | -1.5 | V |
| Output Current | $+I_{OUT}$ | Note 2 | | 1, 2 | +25°C, +125°C | 50 | - | mA |
| | | | | 3 | -55°C | 30 | - | mA |
| | $-I_{OUT}$ | Note 2 | | 1, 2 | +25°C, +125°C | - | -50 | mA |
| | | | | 3 | -55°C | - | -30 | mA |
| Quiescent Power Supply Current | $I_{CC}$ | $R_L$ = 100Ω | | 1 | +25°C | 14 | 26 | mA |
| | | | | 2, 3 | +125°C, -55°C | - | 33 | mA |
| | $I_{EE}$ | $R_L$ = 100Ω | | 1 | +25°C | -26 | -14 | mA |
| | | | | 2, 3 | +125°C, -55°C | -33 | - | mA |

NOTES:

1. Guaranteed from +IN Common Mode Rejection Test, by: $+R_{IN} = 1/CMS_{IBP}$ .
2. Guaranteed from $V_{OUT}$ Test with $R_L$ = 50Ω, by: $I_{OUT} = V_{OUT}/50Ω$.

**TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS**

Table 2 Intentionally Left Blank. See AC Specifications in Table 3

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS**

Device Characterized at: $V_{SUPPLY}$ = ±5V, $A_V$ = +2, $R_F$ = 360Ω, $R_L$ = 100Ω, Unless Otherwise Specified.

| PARAMETERS | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| -3dB Bandwidth | BW(-1) | $A_V$ = -1, $R_F$ = 430Ω<br>$V_{OUT}$ = 200m$V_{P-P}$ | 1 | +25°C | 300 | - | MHz |
| | BW(+1) | $A_V$ = +1, $R_F$ = 510Ω<br>$V_{OUT}$ = 200m$V_{P-P}$ | 1 | +25°C | 550 | - | MHz |
| | BW(+2) | $A_V$ = +2,<br>$V_{OUT}$ = 200m$V_{P-P}$ | 1 | +25°C | 350 | - | MHz |
| Gain Flatness | GF30 | $A_V$ = +2, $R_F$ = 510Ω, f ≤ 30MHz<br>$V_{OUT}$ = 200m$V_{P-P}$ | 1 | +25°C | - | ±0.04 | dB |
| | GF50 | $A_V$ = +2, $R_F$ = 510Ω, f ≤ 50MHz<br>$V_{OUT}$ = 200m$V_{P-P}$ | 1 | +25°C | - | ±0.10 | dB |
| | GF100 | $A_V$ = +2, $R_F$ = 510Ω, f ≤ 100MHz<br>$V_{OUT}$ = 200m$V_{P-P}$ | 1 | +25°C | - | ±0.30 | dB |

**TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)**

Device Characterized at: $V_{SUPPLY}$ = ±5V, $A_V$ = +2, $R_F$ = 360Ω, $R_L$ = 100Ω, Unless Otherwise Specified.

| PARAMETERS | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS MIN | LIMITS MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Slew Rate | +SR(+1) | $A_V$ = +1, $R_F$ = 510Ω, $V_{OUT}$ = $5V_{P-P}$ | 1, 2 | +25°C | 1200 | - | V/μs |
| | -SR(+1) | $A_V$ = +1, $R_F$ = 510Ω, $V_{OUT}$ = $5V_{P-P}$ | 1, 2 | +25°C | 1100 | - | V/μs |
| | +SR(+2) | $A_V$ = +2, $V_{OUT}$ = $5V_{P-P}$ | 1, 2 | +25°C | 1650 | - | V/μs |
| | -SR(+2) | $A_V$ = +2, $V_{OUT}$ = $5V_{P-P}$ | 1, 2 | +25°C | 1500 | - | V/μs |
| Rise and Fall Time | $T_R$ | $A_V$ = +2, $V_{OUT}$ = $0.5V_{P-P}$ | 1, 2 | +25°C | - | 1 | ns |
| | $T_F$ | $A_V$ = +2, $V_{OUT}$ = $0.5V_{P-P}$ | 1, 2 | +25°C | - | 1 | ns |
| Overshoot | +OS | $A_V$ = +2, $V_{OUT}$ = $0.5V_{P-P}$ | 1, 3 | +25°C | - | 25 | % |
| | -OS | $A_V$ = +2, $V_{OUT}$ = $0.5V_{P-P}$ | 1, 3 | +25°C | - | 20 | % |
| Settling Time | TS(0.1) | $A_V$ = +2, $R_F$ = 510Ω<br>$V_{OUT}$ = 2V to 0V, to 0.1% | 1 | +25°C | - | 20 | ns |
| | TS(0.05) | $A_V$ = +2, $R_F$ = 510Ω<br>$V_{OUT}$ = 2V to 0V, to 0.05% | 1 | +25°C | - | 33 | ns |
| 2nd Harmonic Distortion | HD2(30) | $A_V$ = +2, f = 30MHz, $V_{OUT}$ = $2V_{P-P}$ | 1 | +25°C | - | -48 | dBc |
| | HD2(50) | $A_V$ = +2, f = 50MHz, $V_{OUT}$ = $2V_{P-P}$ | 1 | +25°C | - | -45 | dBc |
| | HD2(100) | $A_V$ = +2, f = 100MHz,<br>$V_{OUT}$ = $2V_{P-P}$ | 1 | +25°C | - | -35 | dBc |
| 3rd Harmonic Distortion | HD3(30) | $A_V$ = +2, f = 30MHz, $V_{OUT}$ = $2V_{P-P}$ | 1 | +25°C | - | -65 | dBc |
| | HD3(50) | $A_V$ = +2, f = 50MHz, $V_{OUT}$ = $2V_{P-P}$ | 1 | +25°C | - | -60 | dBc |
| | HD3(100) | $A_V$ = +2, f = 100MHz,<br>$V_{OUT}$ = $2V_{P-P}$ | 1 | +25°C | - | -40 | dBc |

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot-to-lot and within lot variation.
2. Measured between 10% and 90% points.
3. For 200ps input transition times. Overshoot decreases as input transition times increase, especially for $A_V$ = +1. Please refer to Performance Curves.

**TABLE 4. ELECTRICAL TEST REQUIREMENTS**

| MIL-STD-883 TEST REQUIREMENTS | SUBGROUPS (SEE TABLE 1) |
|---|---|
| Interim Electrical Parameters (Pre Burn-In) | 1 |
| Final Electrical Test Parameters | 1 (Note 1), 2, 3 |
| Group A Test Requirements | 1, 2, 3 |
| Groups C and D Endpoints | 1 |

NOTE:

1. PDA applies to Subgroup 1 only.

## Die Characteristics

**DIE DIMENSIONS:**
63 x 44 x 19 mils ± 1 mils
1600μm x 1130μm x 483μm ± 25.4μm

**METALLIZATION:**
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

**GLASSIVATION:**
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

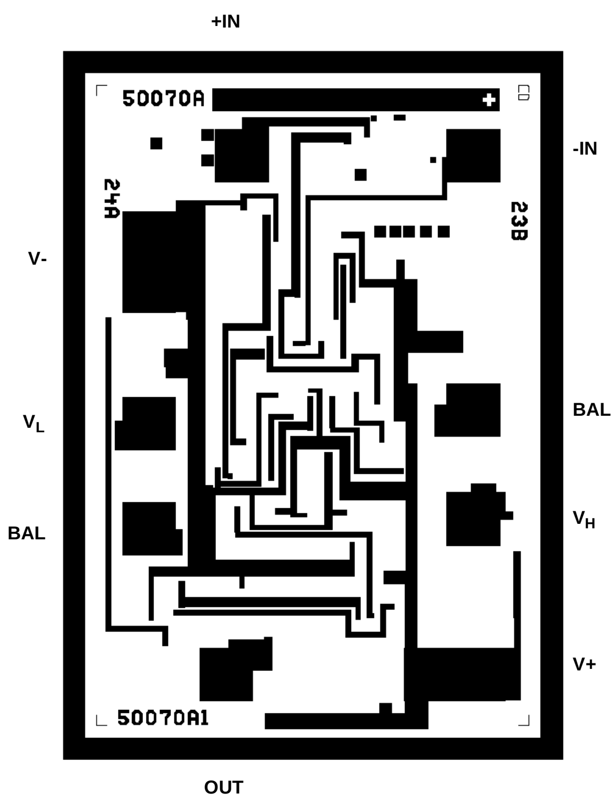
**WORST CASE CURRENT DENSITY:**
$2.0 \times 10^5$ A/cm$^2$ at 47.5mA

**TRANSISTOR COUNT:** 52

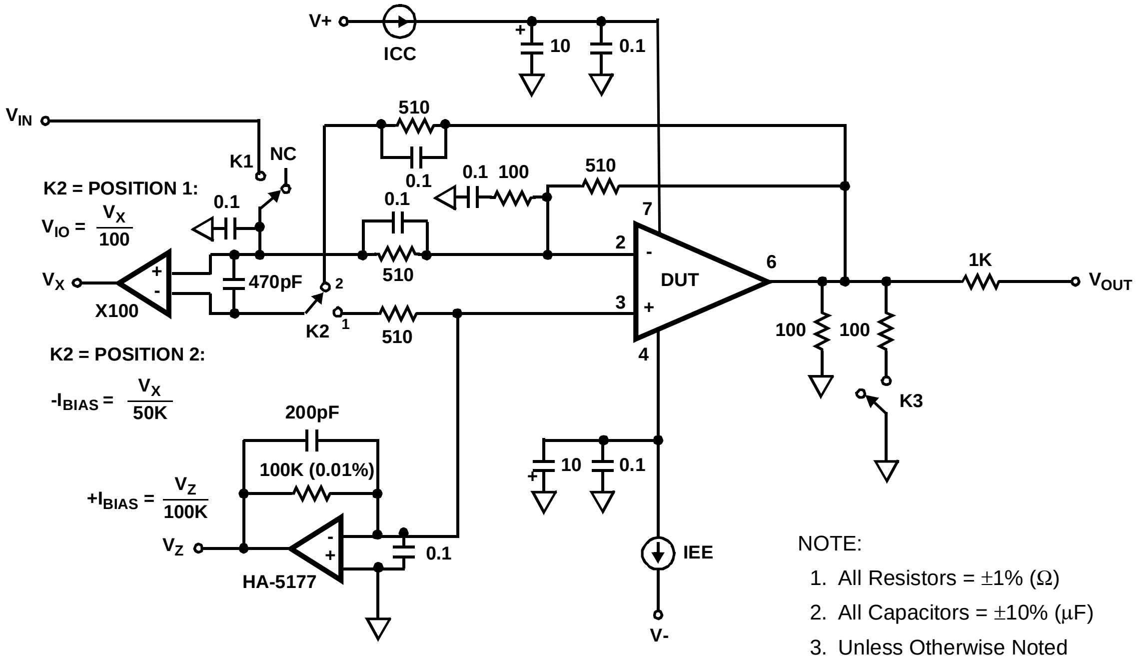
**SUBSTRATE POTENTIAL (Powered Up):** Floating (Recommend Connection to V-)

## Metallization Mask Layout

**HFA1100/883**



## *Test Circuit* (Applies to Table 1)



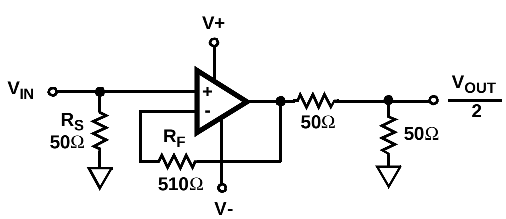

NOTE:

1. All Resistors = ±1% (Ω)
2. All Capacitors = ±10% (µF)
3. Unless Otherwise Noted
4. Chip Components Recommended

## *Test Waveforms*

**SIMPLIFIED TEST CIRCUIT FOR LARGE AND SMALL SIGNAL PULSE RESPONSE** (Applies to Table 3)

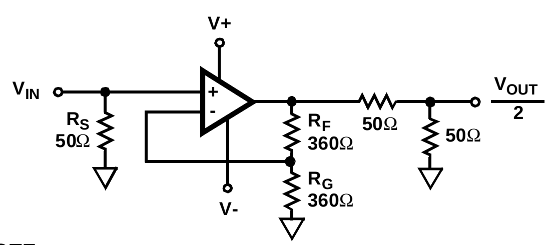
**$A_V$ = +1 TEST CIRCUIT**




NOTE:

1. $V_S$ = ±5V, $A_V$ = +1
2. $R_S$ = 50Ω
3. $R_L$ = 100Ω For Small and Large Signals

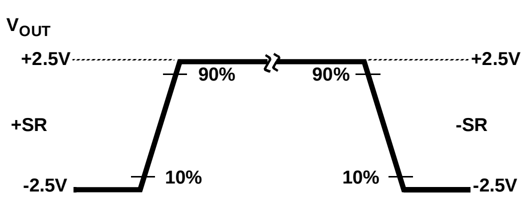
**$A_V$ = +2 TEST CIRCUIT**



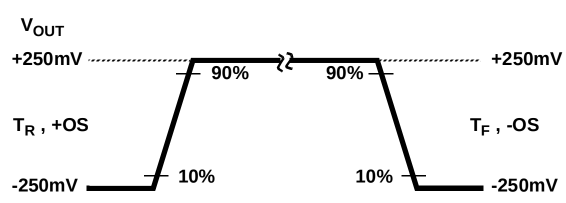

NOTE:

1. $V_S$ = ±5V, $A_V$ = +2
2. $R_S$ = 50Ω
3. $R_L$=100Ω For Small and Large Signals

**LARGE SIGNAL WAVEFORM**

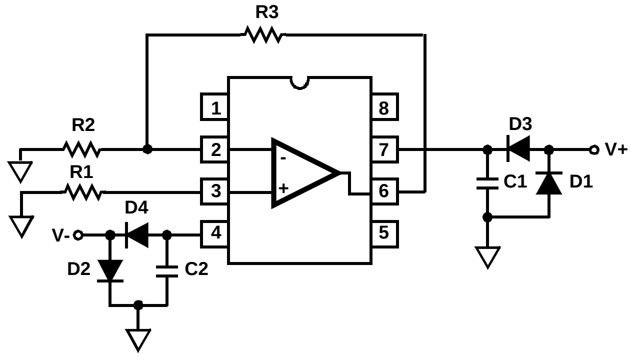



**SMALL SIGNAL WAVEFORM**



## Burn-In Circuit

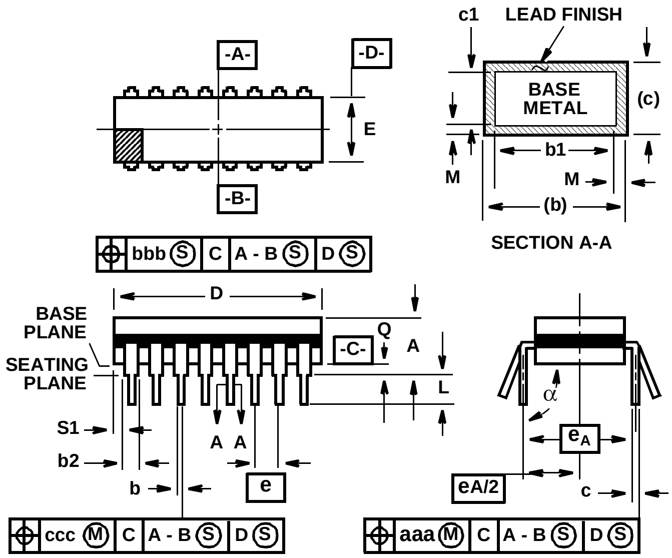
**HFA1100MJ/883 CERAMIC DIP**




NOTES:

1. R1 = R2 = 1kΩ, ±5% (Per Socket)
2. R3 = 10kΩ, ±5% (Per Socket)
3. C1 = C2 = 0.01µF (Per Socket) or 0.1µF (Per Row) Minimum
4. D1 = D2 = 1N4002 or Equivalent (Per Board)
5. D3 = D4 = 1N4002 or Equivalent (Per Socket)
6. V+ = +5.5V ± 0.5V
7. V- = -5.5V ± 0.5V

## Packaging




### F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A) 8 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.200 | - | 5.08 | - |
| b | 0.014 | 0.026 | 0.36 | 0.66 | 2 |
| b1 | 0.014 | 0.023 | 0.36 | 0.58 | 3 |
| b2 | 0.045 | 0.065 | 1.14 | 1.65 | - |
| b3 | 0.023 | 0.045 | 0.58 | 1.14 | 4 |
| c | 0.008 | 0.018 | 0.20 | 0.46 | 2 |
| c1 | 0.008 | 0.015 | 0.20 | 0.38 | 3 |
| D | - | 0.405 | - | 10.29 | 5 |
| E | 0.220 | 0.310 | 5.59 | 7.87 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| eA | 0.300 BSC | | 7.62 BSC | | - |
| eA/2 | 0.150 BSC | | 3.81 BSC | | - |
| L | 0.125 | 0.200 | 3.18 | 5.08 | - |
| Q | 0.015 | 0.060 | 0.38 | 1.52 | 6 |
| S1 | 0.005 | - | 0.13 | - | 7 |
| S2 | 0.005 | - | 0.13 | - | - |
| $\alpha$ | $90^o$ | $105^o$ | $90^o$ | $105^o$ | - |
| aaa | - | 0.015 | - | 0.38 | - |
| bbb | - | 0.030 | - | 0.76 | - |
| ccc | - | 0.010 | - | 0.25 | - |
| M | - | 0.0015 | - | 0.038 | 2 |
| N | 8 | | 8 | | 8 |

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: Inch.
11. Lead Finish: Type A.
12. Materials: Compliant to MIL-I-38535.

## DESIGN INFORMATION

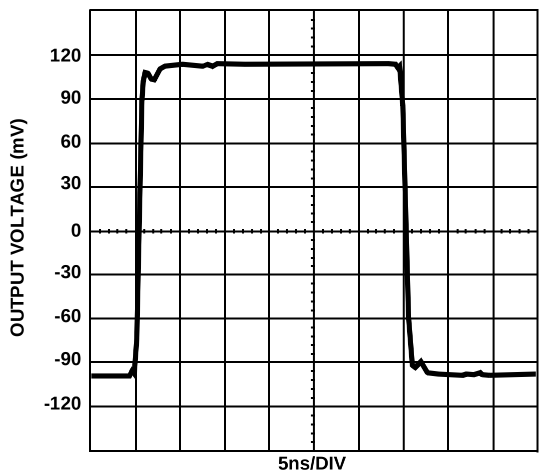
February 2002

**Ultra High Speed Current Feedback Amplifier**

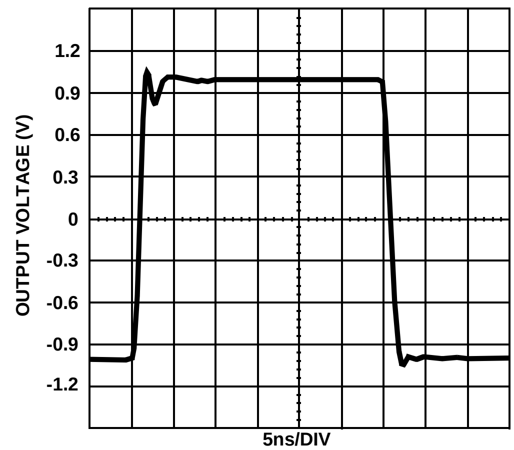
*The information contained in this section has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.*

***Typical Performance Curves*** $V_{SUPPLY}$ = ±5V, $R_F$ = 510Ω, $R_L$ = 100Ω, $T_A$ = +25°C, Unless Otherwise Specified

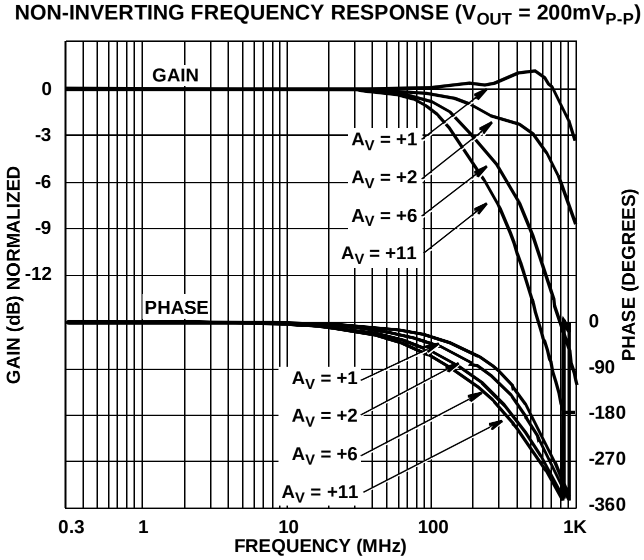
**SMALL SIGNAL PULSE RESPONSE ($A_V$ = +2)**



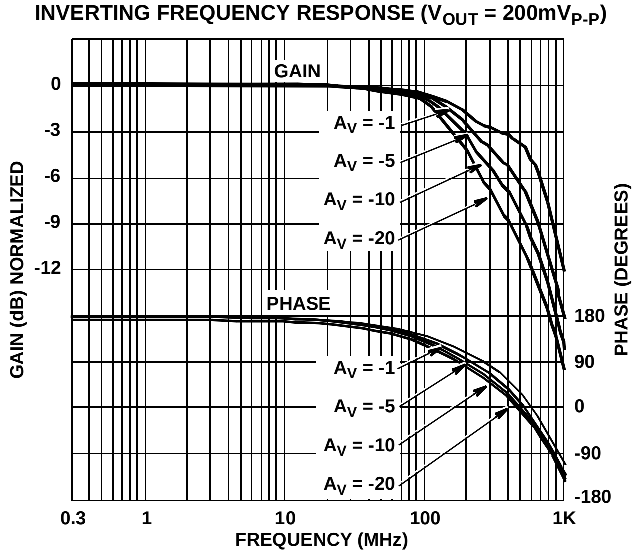

**LARGE SIGNAL PULSE RESPONSE ($A_V$ = +2)**




**NON-INVERTING FREQUENCY RESPONSE ($V_{OUT}$ = 200mV$_{P-P}$)**




**INVERTING FREQUENCY RESPONSE ($V_{OUT}$ = 200mV$_{P-P}$)**



# DESIGN INFORMATION (Continued)

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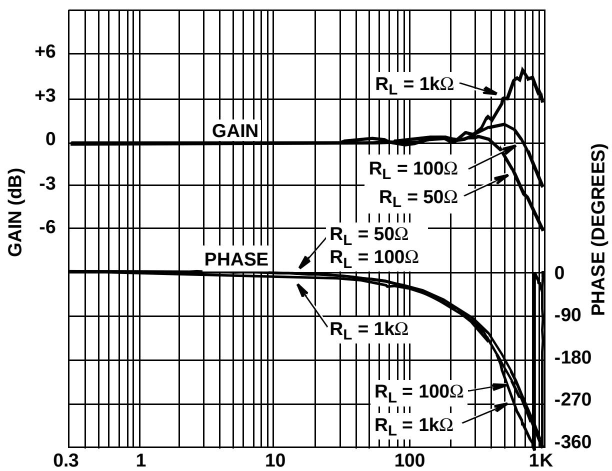
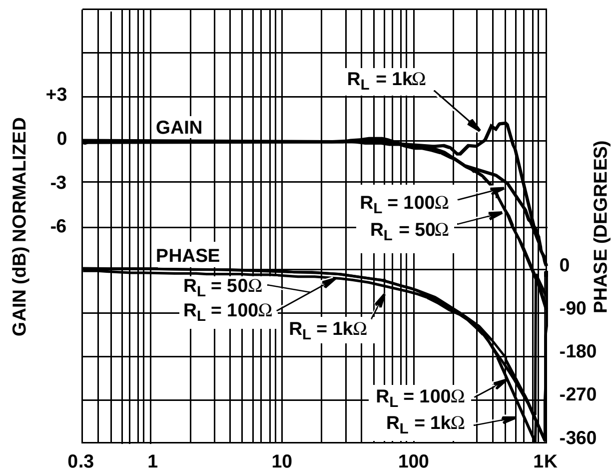
## *Typical Performance Curves* $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $R_L = 100\Omega$, $T_A = +25°C$, Unless Otherwise Specified

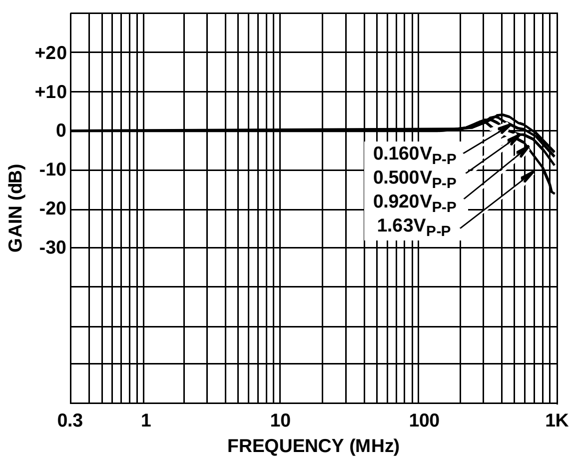
**FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS ($A_V = +1$, $V_{OUT} = 200mV_{P-P}$)**



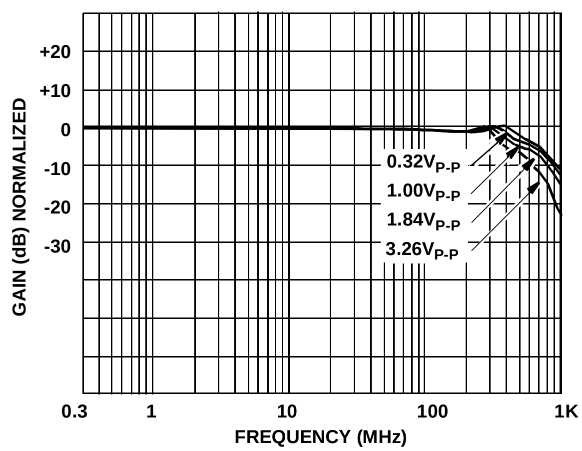

**FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS ($A_V = +2$, $V_{OUT} = 200mV_{P-P}$)**



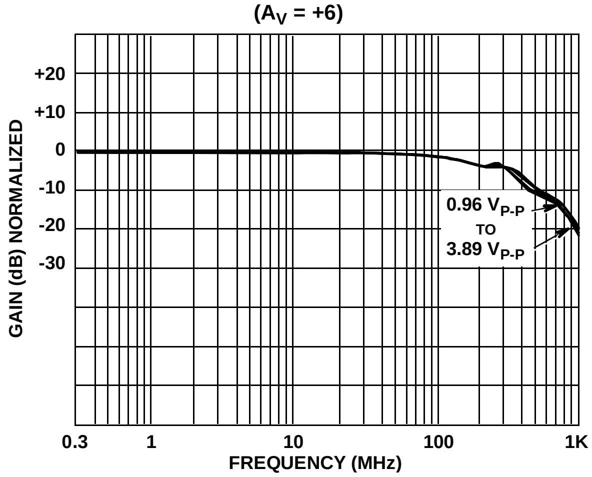

**FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +1$)**



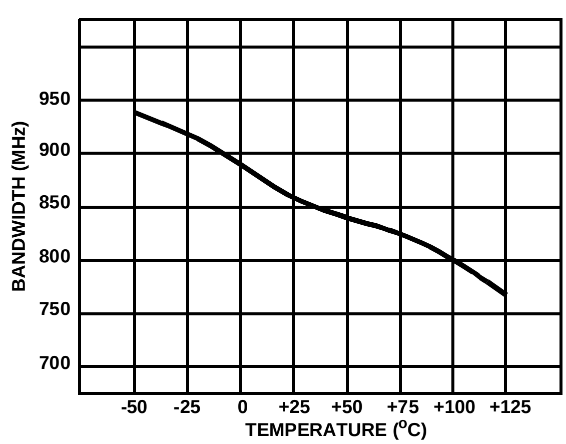

**FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +2$)**




**FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES ($A_V = +6$)**




**-3dB BANDWIDTH vs TEMPERATURE ($A_V = +1$)**



# DESIGN INFORMATION (Continued)

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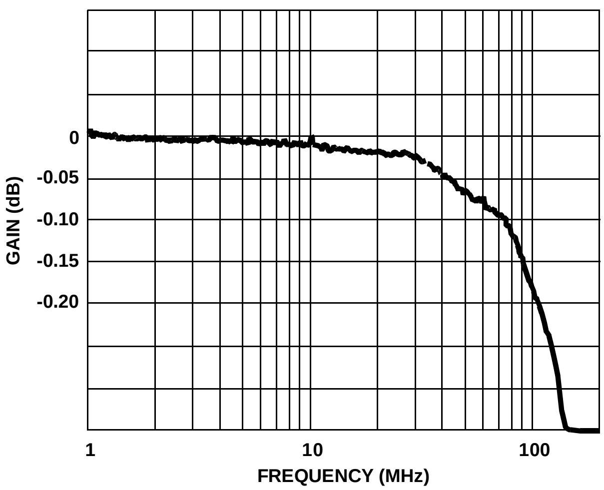
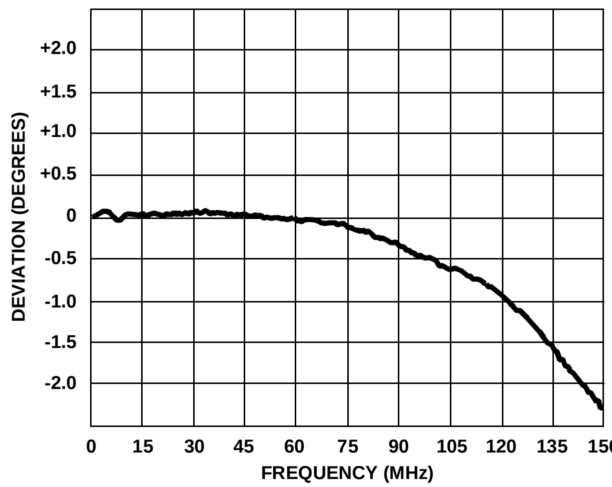
## Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $R_L = 100\Omega$, $T_A = +25°C$, Unless Otherwise Specified

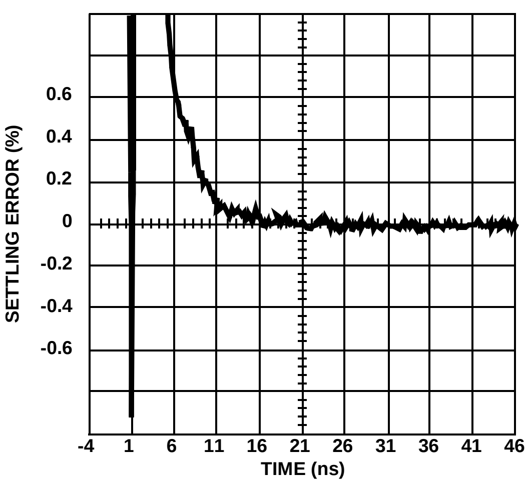
**GAIN FLATNESS ($A_V$ = +2)**



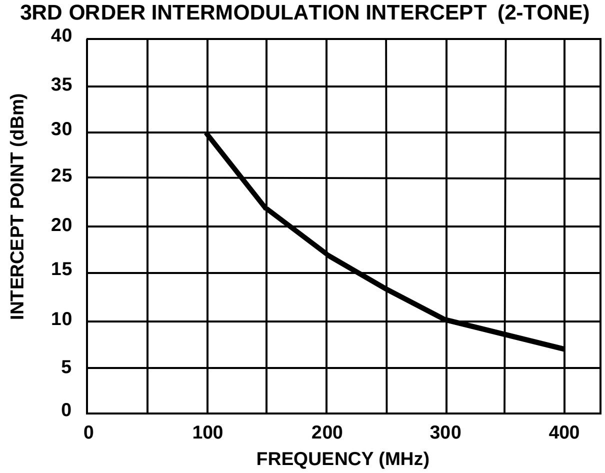

**DEVIATION FROM LINEAR PHASE ($A_V$ = +2)**



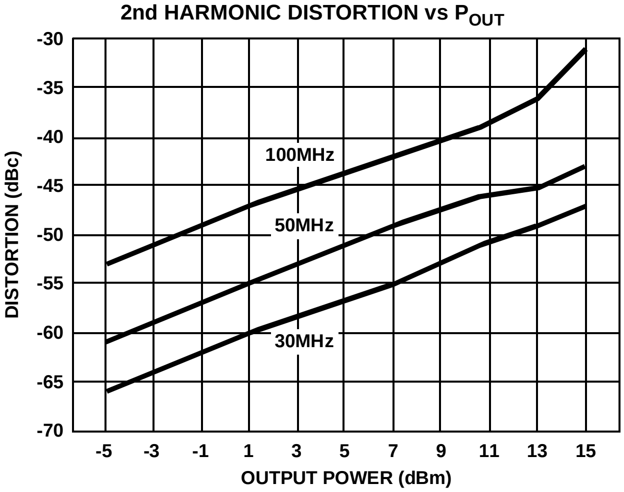

**SETTLING RESPONSE ($A_V$ = +2, $V_{OUT}$ = 2V)**



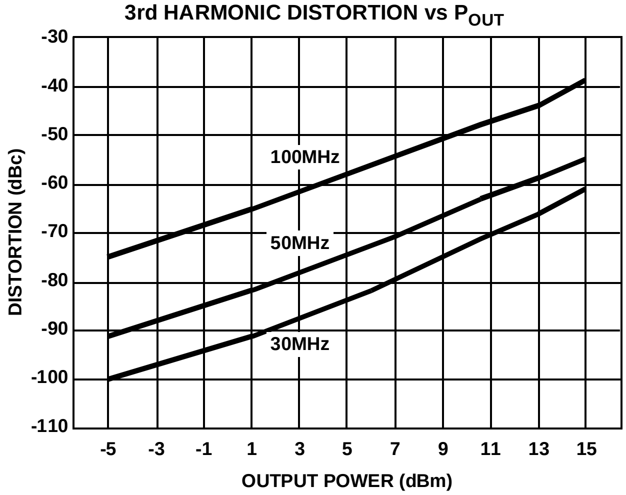

**3RD ORDER INTERMODULATION INTERCEPT (2-TONE)**




**2nd HARMONIC DISTORTION vs $P_{OUT}$**




**3rd HARMONIC DISTORTION vs $P_{OUT}$**



# DESIGN INFORMATION (Continued)

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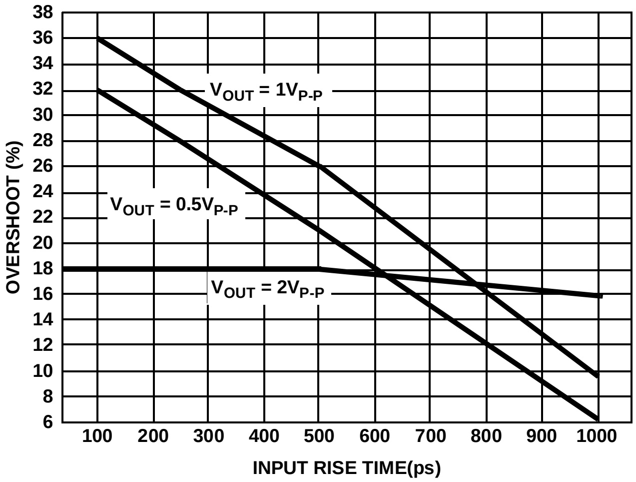
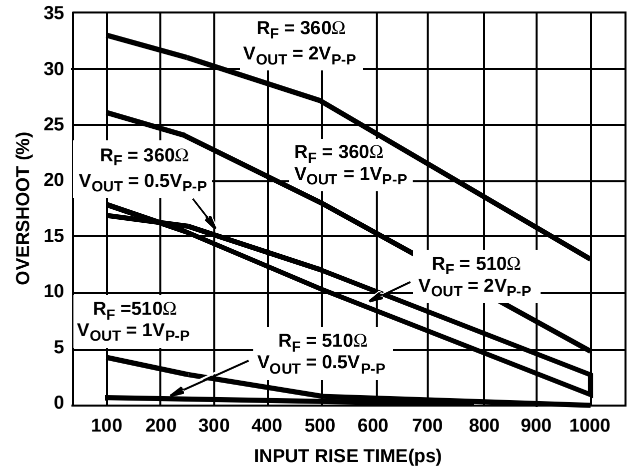
## *Typical Performance Curves* $V_{SUPPLY}$ = ±5V, $R_F$ = 510Ω, $R_L$ = 100Ω, $T_A$ = +25°C, Unless Otherwise Specified

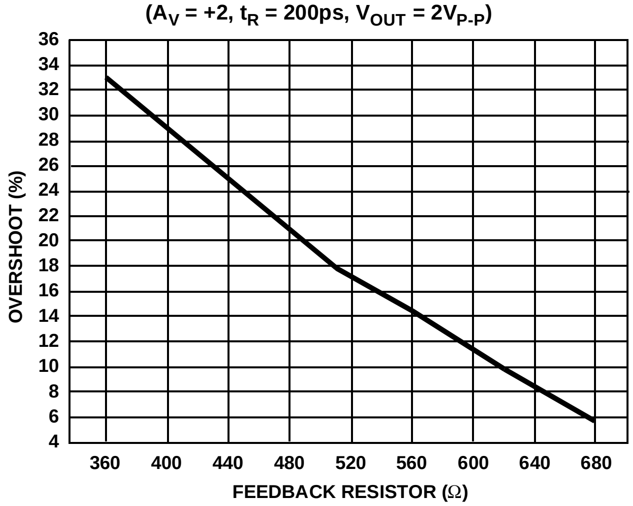
**OVERSHOOT vs INPUT RISE TIME ($A_V$ = +1)**



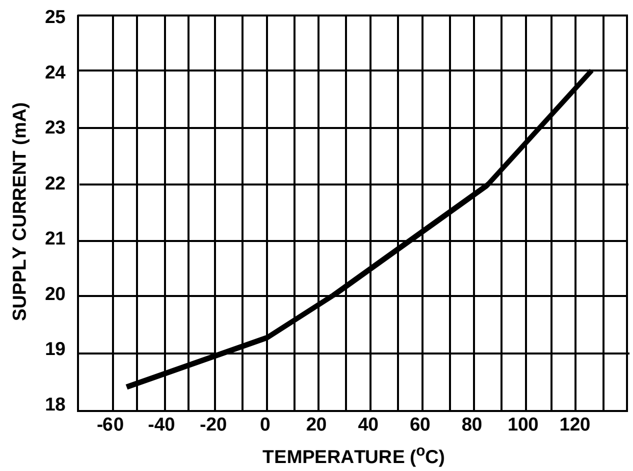

**OVERSHOOT vs INPUT RISE TIME ($A_V$ = +2)**



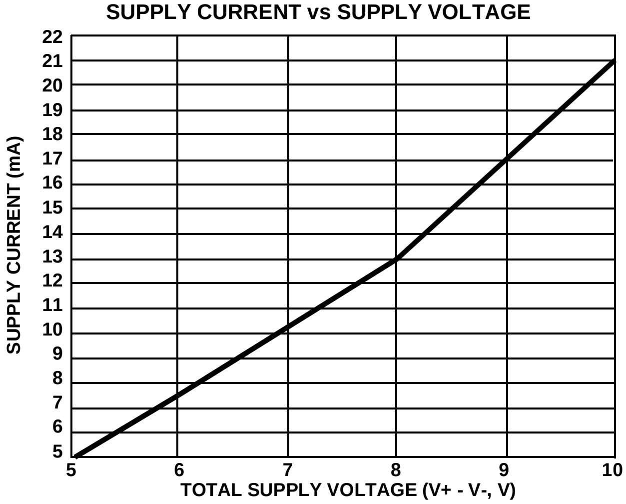

**OVERSHOOT vs FEEDBACK RESISTOR**
**($A_V$ = +2, $t_R$ = 200ps, $V_{OUT}$ = 2$V_{P-P}$)**



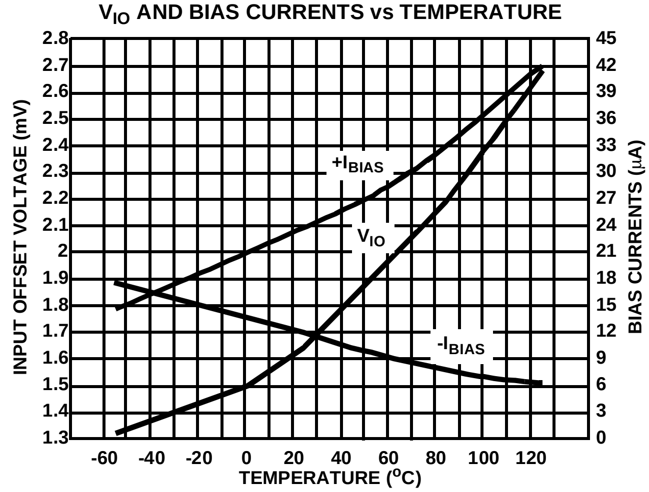

**SUPPLY CURRENT vs TEMPERATURE**




**SUPPLY CURRENT vs SUPPLY VOLTAGE**




**$V_{IO}$ AND BIAS CURRENTS vs TEMPERATURE**



# DESIGN INFORMATION (Continued)

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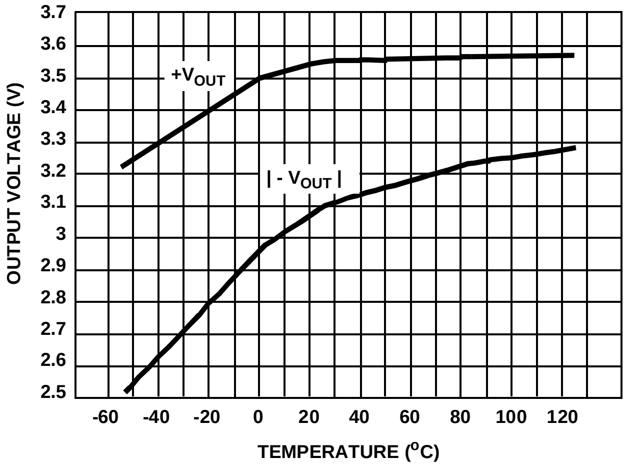
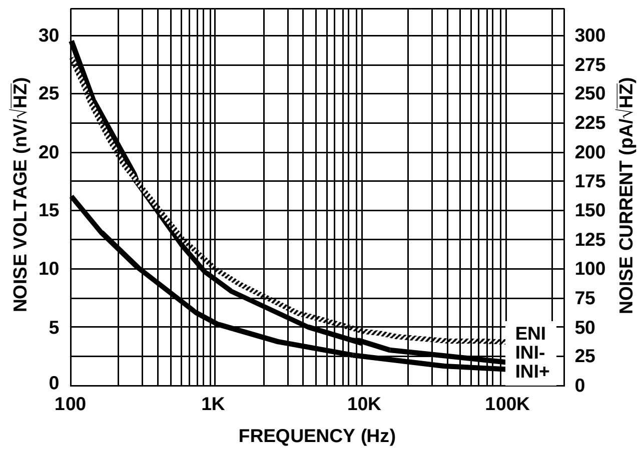
## *Typical Performance Curves* $V_{SUPPLY}$ = ±5V, $R_F$ = 510Ω, $R_L$ = 100Ω, $T_A$ = +25°C, Unless Otherwise Specified

**OUTPUT VOLTAGE vs TEMPERATURE**
($A_V$ = -1, $R_L$ = 50Ω)




**INPUT NOISE vs FREQUENCY**




## *Application Information*

**Optimum Feedback Resistor**

The enclosed plots of inverting and non-inverting frequency response illustrate the performance of the HFA1100 in various gains. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and $R_F$. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and $R_F$, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to $R_F$. The HFA1100 design is optimized for a 510Ω $R_F$ at a gain of +1. Decreasing $R_F$ in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so $R_F$ can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended $R_F$ values for various gains, and the expected bandwidth.

| GAIN ($A_{CL}$) | $R_F$ (Ω) | BANDWIDTH (MHz) |
|---|---|---|
| -1 | 430 | 580 |
| +1 | 510 | 850 |
| +2 | 360 | 670 |
| +5 | 150 | 520 |
| +10 | 180 | 240 |
| +19 | 270 | 125 |

## *PC Board Layout*

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

# DESIGN INFORMATION (Continued)

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Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

## *Driving Capacitive Loads*

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor ($R_S$) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the $R_S$ and $C_L$ combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

$R_S$ and $C_L$ form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing $R_S$ as $C_L$increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at $A_V = +1$, $R_S = 50\Omega$, $C_L = 30pF$, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at $A_V = +1$, $R_S = 5\Omega$, $C_L = 340pF$.

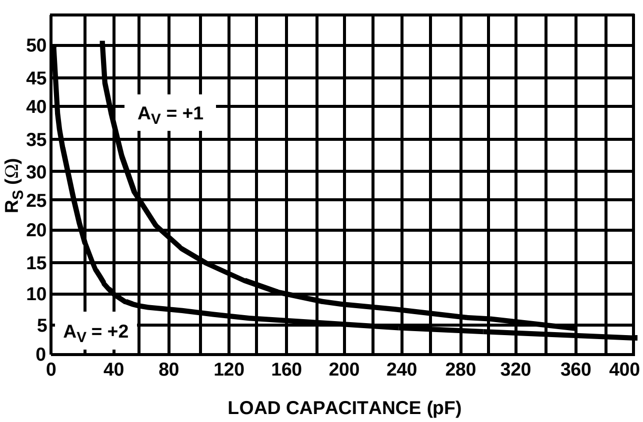


**FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE**

## *Evaluation Board*

The performance of the HFA1100 may be evaluated using the HFA11XX Evaluation Board.

The layout and schematic of the board are shown in Figure 2. To order evaluation boards, please contact your local sales office.

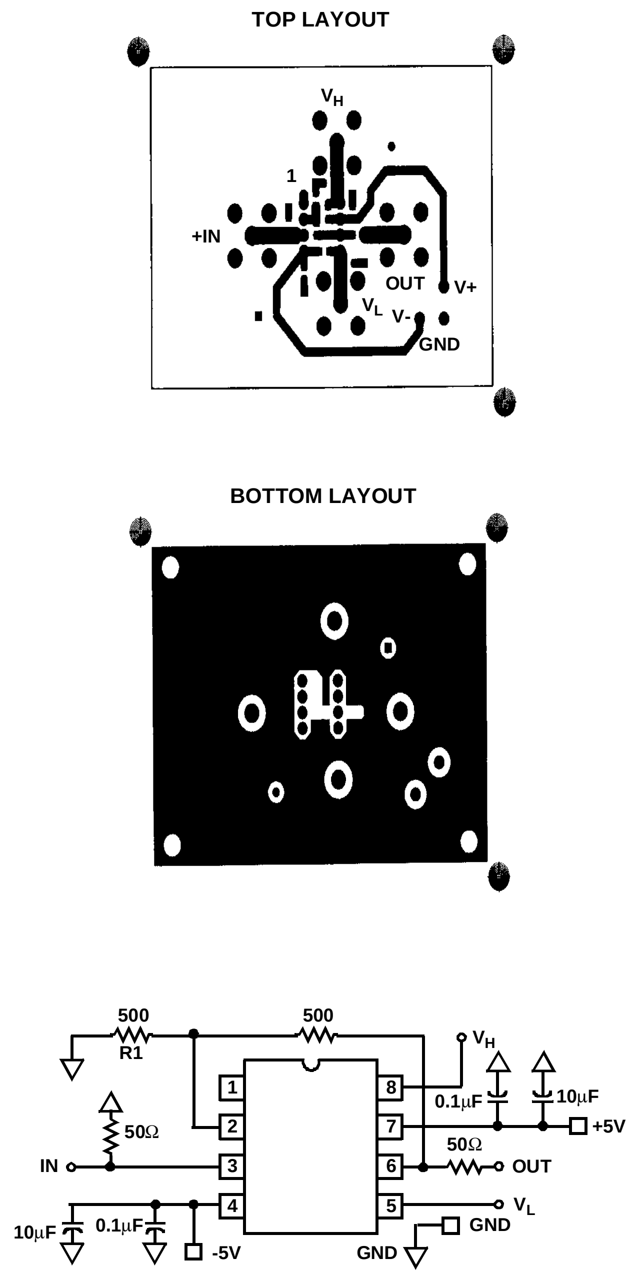


**FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT**

# DESIGN INFORMATION (Continued)

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**TYPICAL PERFORMANCE CHARACTERISTICS**

Device Characterized at: $V_{SUPPLY}$ = ±5V, $R_F$ = 360Ω, $A_V$ = +2V/V, $R_L$ = 100Ω, Unless Otherwise Specified

| PARAMETERS | CONDITIONS | TEMPERATURE | TYPICAL | UNITS |
|---|---|---|---|---|
| Input Offset Voltage * | $V_{CM}$ = 0V | +25°C | 2 | mV |
| Average Offset Voltage Drift | Versus Temperature | Full | 10 | μV/°C |
| $V_{IO}$ CMRR | $\Delta V_{CM}$ = ±2V | +25°C | 46 | dB |
| $V_{IO}$ PSRR | $\Delta V_S$ = ±1.25V | +25°C | 50 | dB |
| +Input Current * | $V_{CM}$ = 0V | +25°C | 25 | μA |
| Average +Input Current Drift | Versus Temperature | Full | 40 | nA/°C |
| - Input Current * | $V_{CM}$ = 0V | +25°C | 12 | μA |
| Average -Input Current Drift | Versus Temperature | Full | 40 | nA/°C |
| +Input Resistance | $\Delta V_{CM}$ = ±2V | +25°C | 50 | kΩ |
| - Input Resistance | | +25°C | 16 | Ω |
| Input Capacitance | | +25°C | 2.2 | pF |
| Input Noise Voltage * | f = 100kHz | +25°C | 4 | nV/√Hz |
| +Input Noise Current * | f = 100kHz | +25°C | 18 | pA/√Hz |
| -Input Noise Current * | f = 100kHz | +25°C | 21 | pA/√Hz |
| Input Common Mode Range | | Full | ±3.0 | V |
| Open Loop Transimpedance | $A_V$ = -1 | +25°C | 500 | kΩ |
| Output Voltage | $A_V$ = -1, $R_L$ = 100Ω | +25°C | ±3.3 | V |
| | $A_V$ = -1, $R_L$ = 100Ω | Full | ±3.0 | V |
| Output Current * | $A_V$ = -1, $R_L$ = 50Ω | +25°C to +125°C | ±65 | mA |
| | $A_V$ = -1, $R_L$ = 50Ω | -55°C to 0°C | ±50 | mA |
| DC Closed Loop Output Resistance | | +25°C | 0.1 | Ω |
| Quiescent Supply Current * | $R_L$ = Open | Full | 24 | mA |
| -3dB Bandwidth * | $A_V$ = -1, $R_F$ = 430Ω, $V_{OUT}$ = 200m$V_{P-P}$ | +25°C | 580 | MHz |
| | $A_V$ = +1, $R_F$ = 510Ω, $V_{OUT}$ = 200m$V_{P-P}$ | +25°C | 850 | MHz |
| | $A_V$ = +2, $R_F$ = 360Ω, $V_{OUT}$ = 200m$V_{P-P}$ | +25°C | 670 | MHz |
| Slew Rate | $A_V$ = +1, $R_F$ = 510Ω, $V_{OUT}$ = 5$V_{P-P}$ | +25°C | 1500 | V/μs |
| | $A_V$ = +2, $V_{OUT}$ = 5$V_{P-P}$ | +25°C | 2300 | V/μs |
| Full Power Bandwidth | $V_{OUT}$ = 5$V_{P-P}$ | +25°C | 220 | MHz |
| Gain Flatness * | To 30MHz, $R_F$ = 510Ω | +25°C | ±0.014 | dB |
| | To 50MHz, $R_F$ = 510Ω | +25°C | ±0.05 | dB |
| | To 100MHz, $R_F$ = 510Ω | +25°C | ±0.14 | dB |
| Linear Phase Deviation * | To 100MHz, $R_F$ = 510Ω | +25°C | ±0.6 | Degrees |

# DESIGN INFORMATION (Continued)

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**TYPICAL PERFORMANCE CHARACTERISTICS**

Device Characterized at: $V_{SUPPLY}$ = ±5V, $R_F$ = 360Ω, $A_V$ = +2V/V, $R_L$ = 100Ω, Unless Otherwise Specified

| PARAMETERS | CONDITIONS | TEMPERATURE | TYPICAL | UNITS |
|---|---|---|---|---|
| 2nd Harmonic Distortion * | 30MHz, $V_{OUT}$ = $2V_{P-P}$ | +25°C | -55 | dBc |
| | 50MHz, $V_{OUT}$ = $2V_{P-P}$ | +25°C | -49 | dBc |
| | 100MHz, $V_{OUT}$ = $2V_{P-P}$ | +25°C | -44 | dBc |
| 3rd Harmonic Distortion * | 30MHz, $V_{OUT}$ = $2V_{P-P}$ | +25°C | -84 | dBc |
| | 50MHz, $V_{OUT}$ = $2V_{P-P}$ | +25°C | -70 | dBc |
| | 100MHz, $V_{OUT}$ = $2V_{P-P}$ | +25°C | -57 | dBc |
| 3rd Order Intercept * | 100MHz, $R_F$ = 510Ω | +25°C | 30 | dBm |
| 1dB Compression | 100MHz, $R_F$ = 510Ω | +25°C | 20 | dBm |
| Reverse Isolation ($S_{12}$) | 40MHz, $R_F$ = 510Ω | +25°C | -70 | dB |
| | 100MHz, $R_F$ = 510Ω | +25°C | -60 | dB |
| | 600MHz, $R_F$ = 510Ω | +25°C | -32 | dB |
| Rise & Fall Time | $V_{OUT}$ = $0.5V_{P-P}$ | +25°C | 500 | ps |
| | $V_{OUT}$ = $2V_{P-P}$ | +25°C | 800 | ps |
| Overshoot * | $V_{OUT}$ = $0.5V_{P-P}$, Input $t_R/t_F$ = 550ps | +25°C | 11 | % |
| Settling Time * | To 0.1%, $V_{OUT}$ = 2V to 0V, $R_F$ = 510Ω | +25°C | 11 | ns |
| | To 0.05%, $V_{OUT}$ = 2V to 0V, $R_F$ = 510Ω | +25°C | 19 | ns |
| | To 0.02%, $V_{OUT}$ = 2V to 0V, $R_F$ = 510Ω | +25°C | 34 | ns |
| Differential Gain | $A_V$ = +2, $R_L$ = 75Ω, NTSC | +25°C | 0.03 | % |
| Differential Phase | $A_V$ = +2, $R_L$ = 75Ω, NTSC | +25°C | 0.05 | Degrees |
| Overdrive Recovery Time | $R_F$ = 510Ω, $V_{IN}$ = $5V_{P-P}$ | +25°C | 7.5 | ns |

* See Typical Performance Curves for more information.