Dual-Channel Digital Isolator

ADuM1210

FEATURES

Narrow body, 8-lead SOIC
Low power operation
- **5 V operation**
  - **1.1 mA per channel maximum @ 0 Mbps to 2 Mbps**
  - **3.7 mA per channel maximum @ 10 Mbps**
- **3 V operation**
  - **0.8 mA per channel maximum @ 0 Mbps to 2 Mbps**
  - **2.2 mA per channel maximum @ 10 Mbps**

3 V/5 V level translation
High temperature operation: 105°C
High data rate: dc to 25 Mbps (NRZ)
Precise timing characteristics
- **3 ns maximum pulse width distortion**
- **3 ns maximum channel-to-channel matching**

High common-mode transient immunity: >25 kV/μs
Safety and regulatory approvals
- **UL recognition**
  - **2500 V rms for 1 minute per UL 1577**
- **CSA Component Acceptance Notice #5A**
- **VDE certificate of conformity**
  - **DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01**
  - **DIN EN 60950 (VDE 0805): 2001-12; DIN EN 60950: 2000**
  - **V_{IORM} = 560 V peak**

APPLICATIONS

Size-critical multichannel isolation
SPI® interface/data converter isolation
RS-232/RS-422/RS-485 transceiver isolation
Digital field bus isolation

GENERAL DESCRIPTION

The ADuM1210[1] is a dual-channel, digital isolator based on Analog Devices' *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The concerns of the typical optocoupler regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple, *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with *i*Coupler products. Furthermore, *i*Coupler devices consume one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM1210 isolator provides two independent isolation channels operable with the supply voltage on either side ranging from 2.7 V to 5.5 V. This provides compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM1210 provides low pulse-width distortion (<3 ns) and tight channel-to-channel matching (<3 ns). Unlike other optocoupler alternatives, the ADuM1210 isolator has a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions. Furthermore, as an alternative to the ADuM1200 dual-channel, digital isolator that defaults to an output high condition, the ADuM1210's outputs default to a logic low state when input power is off.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and other pending patents.

FUNCTIONAL BLOCK DIAGRAM

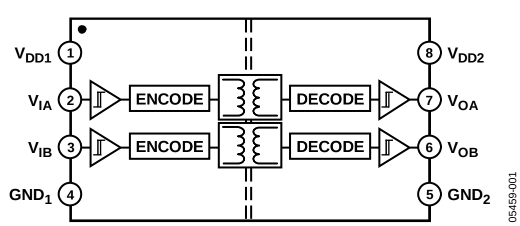

Figure 1.

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REVISION HISTORY

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7/05—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI (Q)}$		0.50	0.60	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.25	mA	
Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.1	1.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.3	5.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.3	2.0	mA	5 MHz logic signal freq.
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 ≤ V_{IA}, V_{IB} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}	0.7 V_{DD1}, V_{DD2}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DD1}, V_{DD2}	V	
Logic High Output Voltages	V_{OAH}	V_{DD1}/ V_{DD2} − 0.1	5.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
	V_{OBH}	V_{DD1}/ V_{DD2} − 0.5	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
	V_{OBL}		0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		50	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			15	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD1}, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current, per Channel[8]	$I_{DDI (D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current, per Channel[8]	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] Supply current values are for both channels running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 7 through Figure 8 for total I_{DD1} and I_{DD2} supply currents as a function of data rate.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

All voltages are relative to their respective ground. 2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.35	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.20	mA	
Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		0.6	1.0	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.2	0.6	mA	DC to 1 MHz logic signal freq.
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$		2.2	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		0.7	1.1	mA	5 MHz logic signal freq.
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 ≤ V_{IA}, V_{IB}, ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}	0.7 V_{DD1}, V_{DD2}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DD1}, V_{DD2}	V	
Logic High Output Voltages	V_{OAH}	V_{DD1}/ V_{DD2} − 0.1	3.0		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
	V_{OBH}	V_{DD1}/ V_{DD2} − 0.5	2.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
	V_{OBL}		0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	20		60	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			22	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3.0		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	V_{Ix} = V_{DD1}, V_{DD2}, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current, per Channel[8]	$I_{DDI (D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[8]	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 7 and Figure 8 for total I_{DD1} and I_{DD2} supply currents as a function of data rate.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

All voltages are relative to their respective ground. 5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5.0 V; or V_{DD1} = 5.0 V, V_{DD2} = 3.0 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI (Q)}$				mA	
5 V/3 V Operation			0.50	0.6	mA	
3 V/5 V Operation			0.26	0.35	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO (Q)}$				mA	
5 V/3 V Operation			0.11	0.20	mA	
3 V/5 V Operation			0.19	0.25	mA	
Total Supply Current, Two Channels[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.1	1.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.6	1.0	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.2	0.6	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.5	0.8	mA	DC to 1 MHz logic signal freq.
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			4.3	5.5	mA	5 MHz logic signal freq.
3 V/5 V Operation			2.2	3.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			0.7	1.1	mA	5 MHz logic signal freq.
3 V/5 V Operation			1.3	2.0	mA	5 MHz logic signal freq.
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 ≤ V_{IA}, V_{IB} ≤ V_{DD1} or V_{DD2}
Logic High Input Threshold	V_{IH}	0.7 V_{DD1}, V_{DD2}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DD1}, V_{DD2}	V	
5 V/3 V Operation		0.8			V	
3 V/5 V Operation		0.4			V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD1}/ V_{DD2} − 0.1	V_{DD1}, V_{DD2}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1}/ V_{DD2} − 0.5	V_{DD1}, V_{DD2} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[2]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[4]	t_{PHL}, t_{PLH}	15		55	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\lvert t_{PLH} - t_{PHL}\rvert$[4]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[5]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[6]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[6]	t_{PSKOD}			22	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise/Fall Time (10% to 90%)	t_R/t_f					C_L = 15 pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output[7]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}, V_{DD2}, V_{CM}$ = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[7]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel[8]	$I_{DDI (D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[8]	$I_{DDO (D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

[1] The supply current values are for both channels combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 7 and Figure 8 for total I_{DD1} and I_{DD2} supply currents as a function of data rate.
[2] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.
[3] The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.
[4] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.
[5] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[6] Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.
[7] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[8] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in the signal data rate. See Figure 4 through Figure 6 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	$θ_{JCI}$		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	$θ_{JCO}$		41		°C/W	

[1] The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM1210 is approved by the following organizations:

Table 5.

UL	CSA	VDE
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01[2]
2500 V rms isolation voltage		Basic insulation, 560 V peak
		Complies with DIN EN 60747-5-2 (VDE 0884 Part 2):2003-01, DIN EN 60950 (VDE 0805):2001-12; EN 60950:2000, Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL1577, each ADuM1210 is proof-tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).
[2] In accordance with DIN EN 60747-5-2, each ADuM1210 is proof-tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN EN 60747-5-2 (VDE 0884 PART 2) INSULATION CHARACTERISTICS

Table 7.

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110			
For Rated Mains Voltage ≤ 150 V rms		I–IV	
For Rated Mains Voltage ≤ 300 V rms		I–III	
For Rated Mains Voltage ≤ 400 V rms		I–II	
Climatic Classification		40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method b1	V_{PR}	1050	V peak
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC			
Input-to-Output Test Voltage, Method a	V_{PR}		
After Environmental Tests Subgroup 1			
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC		896	V peak
After Input and/or Safety Test Subgroup 2/3			
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC		672	V peak
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	4000	V peak
Safety-Limiting Values (maximum value allowed in the event of a failure; also see Figure 2)			
Case Temperature	T_S	150	°C
Side 1 Current	I_{S1}	160	mA
Side 2 Current	I_{S2}	170	mA
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

Note that the "*" marking on the package denotes DIN EN 60747-5-2 approval for a 560 V peak working voltage.

This isolator is suitable for basic isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

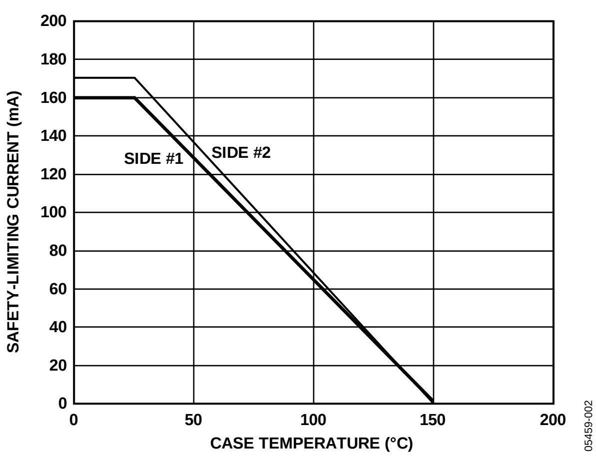


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages [1]	V_{DD1}, V_{DD2}	2.7	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	−55	150	°C
Ambient Operating Temperature	T_A	−40	105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	−0.5	7.0	V
Input Voltage[1]	V_{IA}, V_{IB}	−0.5	V_{DDI} + 0.5	V
Output Voltage[1]	V_{OA}, V_{OB}	−0.5	V_{DDO} + 0.5	V
Average Output Current, per Pin[2]	I_O	−35	35	mA
Common-Mode Transients[3]	CM_L, CM_H	−100	+100	kV/µs

[1] All voltages are relative to their respective ground.
[2] See Figure 2 for maximum rated current values for various temperatures.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10. ADuM1210 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

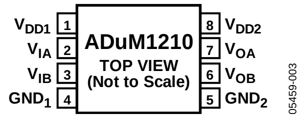


Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for isolator Side 1.
5	GND_2	Ground 2. Ground reference for isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

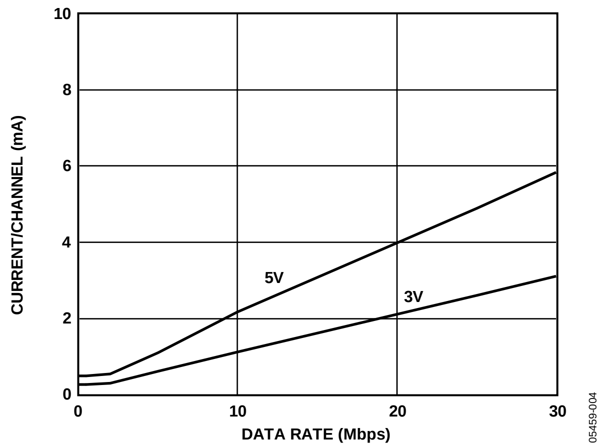


Figure 4. Typical Input Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation

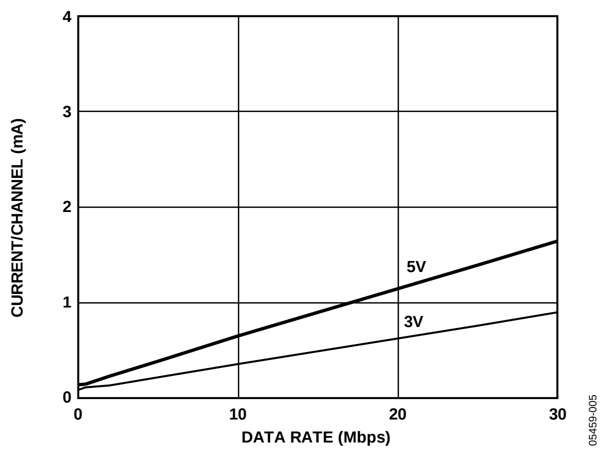


Figure 5. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

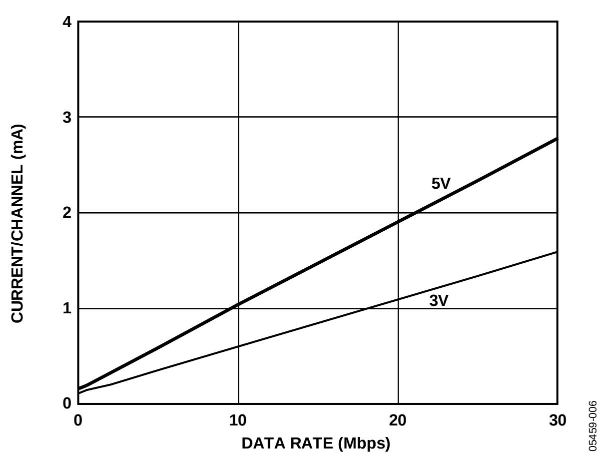


Figure 6. Typical Output Supply Current per Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

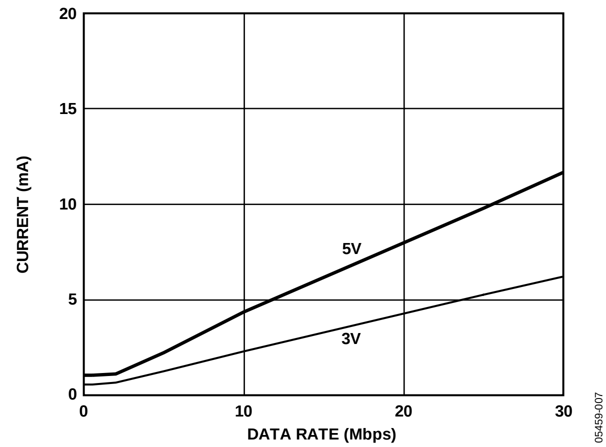


Figure 7. Typical ADuM1210 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

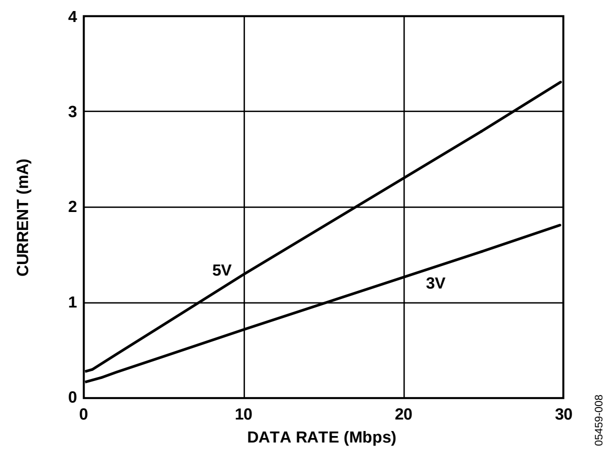


Figure 8. Typical V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation

APPLICATION INFORMATION

PC BOARD LAYOUT

The ADuM1210 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins. The capacitor value should be between 0.01 μF and 0.1 μF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output.

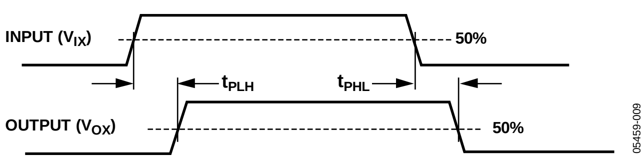


Figure 9. Propagation Delay Parameters

Pulse-width distortion is the maximum difference between the two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM1210 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM120x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 2 μs at the input, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 10) by the watchdog timer circuit.

The ADuM1210 is extremely immune to external magnetic fields. The limitation on the ADuM1210's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM1210 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta / dt)\sum \Pi r_n^2; n = 1, 2, \ldots N$$

where:

β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM1210 and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 10.

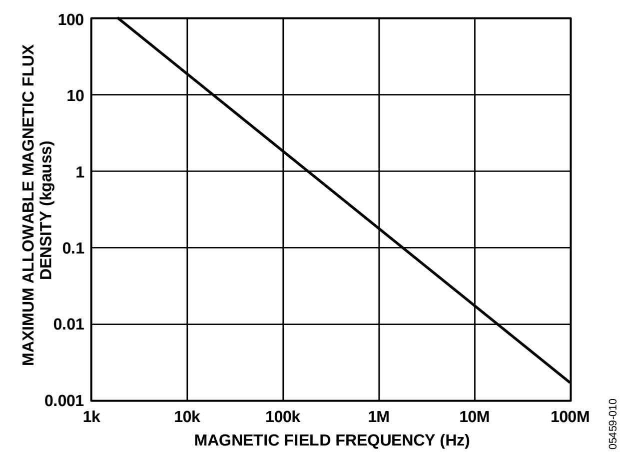


Figure 10. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and had the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1210 transformers. Figure 11 expresses these allowable current magnitudes as a function of frequency for selected distances. As seen, the ADuM1210 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example, one would have to place a 0.5 kA current 5 mm away from the ADuM1210 to affect the component's operation.

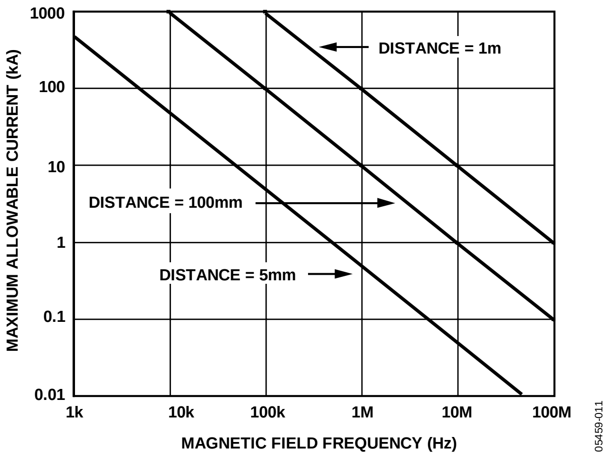


Figure 11. Maximum Allowable Current for Various Current-to-ADuM1210 Spacings

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM1210 isolator is a function of the supply voltage, the channel's data rate, and the channel's output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5f_r$$

for each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

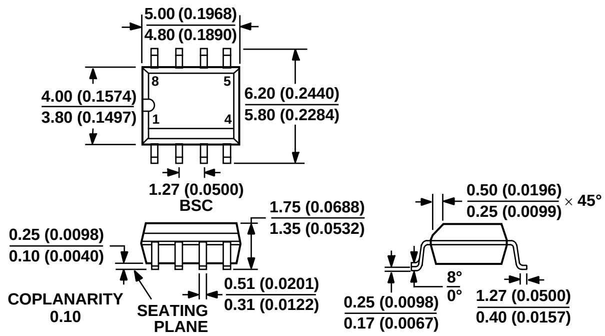
f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled. Figure 4 and Figure 5 provide per-channel supply currents as a function of data rate for an unloaded output condition. Figure 6 provides per-channel supply current as a function of data rate for a 15 pF output condition. Figure 7 and Figure 8 provide total I_{DD1} and I_{DD2} supply current as a function of data rate.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 12. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse-Width Distortion (ns)	Temperature Range (°C)	Package Option[1]
ADuM1210BRZ[2]	2	0	10	50	3	–40 to +105	R-8
ADuM1210BRZ-RL7[2]	2	0	10	50	3	–40 to +105	R-8

[1] R-8 = 8-lead, narrow body SOIC.
[2] Z = Pb-free part.

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