4-Bit Micro-Controller with LCD Driver, 2K Word

FEATURES

- Wide operating voltage range:

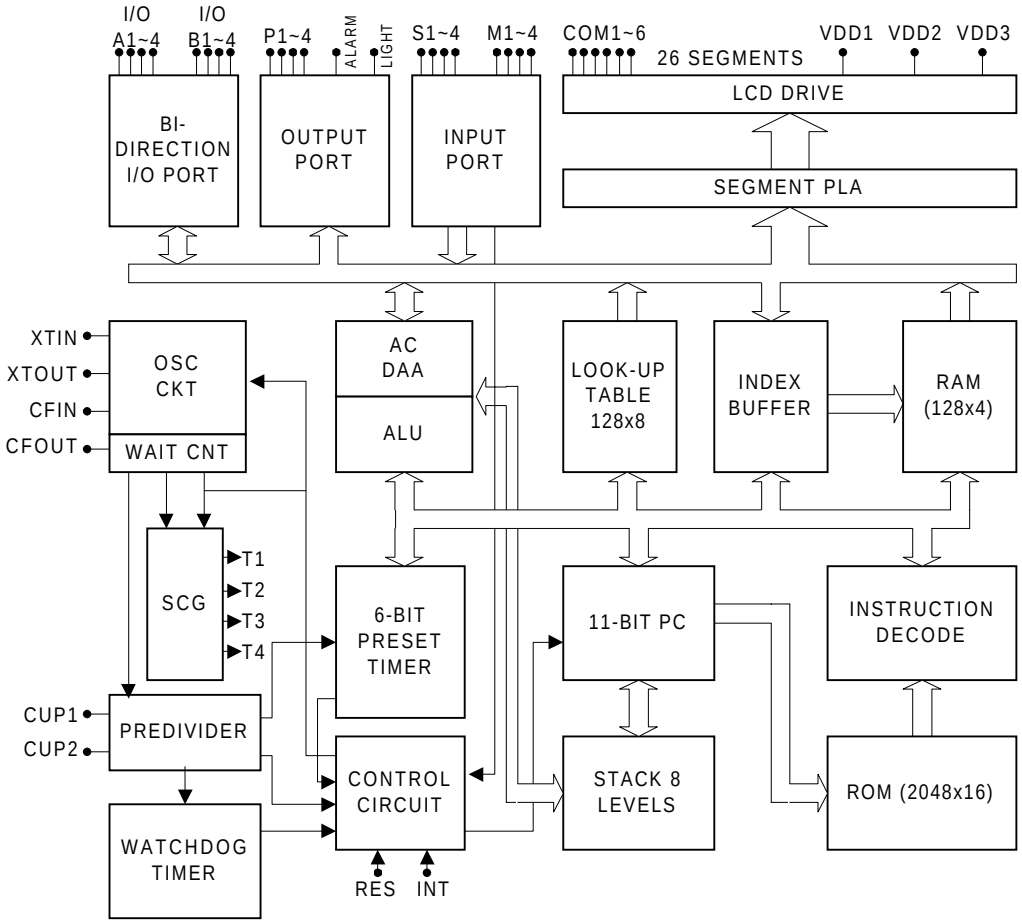
Supply Voltage	Cycle Time	Clock Usage	Remark
4.5V to 5.5V	122μs,280ns	dual clock	Max. 3.58MHz
4V to 5V	122μs,280ns	dual clock	Max. 3.58MHz
2.4V to 3.3V	122μs,2.2us	dual clock	Max. 455KHz
1.2V to 1.65V	122μs	slow clock only	32.768KHz

- 118 instruction sets:
  - Binary addition, subtraction, BCD adjustment, logical operation in direct addressing mode and index addressing mode.
  - Single-bit manipulation (set, reset, decision for branch).
  - 4-bit input/output.
  - Various conditional branches.
  - 16 working registers and manipulation.
  - LCD driver data transfer.
  - Look-up table.
  - Programmable option.
  - System clock selection.
- 8-level subroutine nesting.
- Interrupt function:
  - External factor: 2 (INT pin or ports S, M).
  - Internal factor: 2 (timer, divider).
- ROM/RAM capacity:
  - ROM capacity . . . . . 2048 x 16 bits.
  - RAM capacity . . . . . 128 x 4 bits.
- Watchdog timer.
- Input/Output ports:
  - Input ports . . . . . 2 ports/8pins (S, M).
  - Output port . . . . . 1 port/4pins (P).
  - Pseudo serial output port . . . . . Also used for output port.
  - Input/Output ports . . . . . 2 ports/8pins (I/OA, I/OB).
- 2 control outputs . . . . . light, alarm.
- LCD driver output:
  - 26 LCD driver outputs (up to 156 LCD segments are drivable).
  - Mask option is used to select static ½ duty, ½ bias ½ duty, ½ bias 1/3 duty, ½ bias ¼ duty, 1/3 bias 1/3 duty, ½ bias ¼ duty and 1/3 bias 1/6 duty drive modes of the LCD panel.
  - Mask option permits LCD driver output pins to be used for output ports.
  - Segment PLA circuit permits any layout on the LCD panel.
- Built-in doubler, halver, tripler.
- One 6-bit timer with programmable option clock.
- 128-byte look-up table for LCD display pattern or 256-nibble look-up table for general purpose.
- Halt function.
- Stop function.
- Dual clock operation.

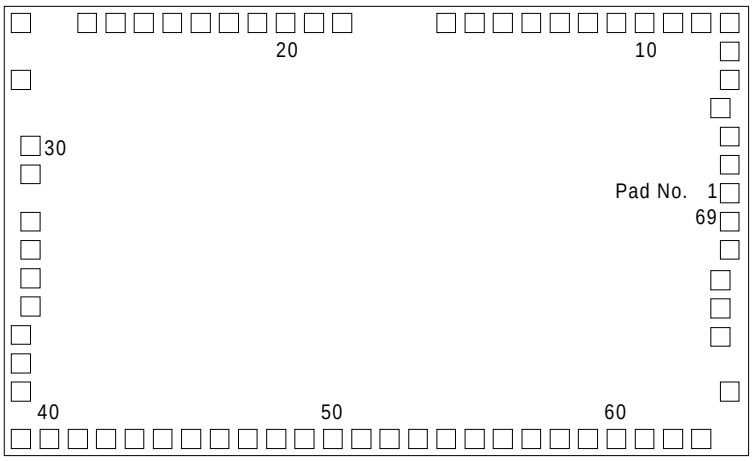
GENERAL DESCRIPTION

The MTU420 is an LCD driver with an embedded high-performance 4-bit microcomputer. It contains all the necessary functions in a single chip: dual clock, 4-bit parallel processing ALU, ROM, RAM, input/output ports, timer, clock generator, LCD driver, look-up table and watchdog timer. The set of 118 instructions includes not only 4-bit operation and manipulation instruction but also various conditional branch instructions, and LCD driver data transfer instructions that are powerful and easy to follow. The halt function stops internal operations other than the oscillator, divider and LCD driver in order to minimize power dissipation. The stop function stops all clocks in the chip.

BLOCK DIAGRAM



1.0 CONNECTION DIAGRAM



2.0 PIN ASSIGNMENT

Pin No.	Pin Name	X (um)	Y (um)	Pin No.	Pin Name	X (um)	Y (um)	Pin No.	Pin Name	X (um)	Y (um)
1	VDD	4127	1311	25	M3	742.5	2770.5	49	SEG11	1712.5	125.5
2	VDD1	4110.5	1471	26	M4	582.5	2770.5	50	SEG12	1872.5	125.5
3	VDDO	4110.5	1631	27	TESTA	422.5	2770.5	51	SEG13	2032.5	125.5
4	VDD2	4078	1791	28	CUP1	109	2757	52	SEG14	2192.5	125.5
5	ALM	4127	2142.5	29	CUP2	109	2190	53	SEG15	2352.5	125.5
6	LIGHT	4127	2440.5	30	S2	154.5	1891	54	SEG16	2512.5	125.5
7	S4	4079.5	2700.5	31	S1	154.5	1725.5	55	SEG17	2672.5	125.5
8	S3	3919.5	2770.5	32	XTIN	154.5	1460.5	56	SEG18	2832.5	125.5
9	IOA1	3759.5	2770.5	33	XTOUT	154.5	1300.5	57	SEG19	2992.5	125.5
10	IOA2	3599.5	2770.5	34	CFIN	154.5	980.5	58	SEG20	3152.5	125.5
11	IOA3	3439.5	2770.5	35	CFOUT	154.5	1140.5	59	SEG21	3312.5	125.5
12	IAO4	3279.5	2770.5	36	COM1	133	730.5	60	SEG22	3472.5	125.5
13	IOB1	3119.5	2770.5	37	COM2	133	570.5	61	SEG23	3632.5	125.5
14	IOB2	2959.5	2770.5	38	COM3	133	410.5	62	SEG24	3792.5	125.5
15	IOB3	2799.5	2770.5	39	SEG1	112.5	125.5	63	SEG25	3952.5	125.5
16	IOB4	2639.5	2770.5	40	SEG2	272.5	125.5	64	SEG26	4112.5	225.5
17	RES	2479.5	2770.5	41	SEG3	432.5	125.5	65	COM4	4092	461
18	INT	1862.5	2770.5	42	SEG4	592.5	125.5	66	COM5	4092	621
19	P1	1702.5	2770.5	43	SEG5	752.5	125.5	67	COM6	4092	781
20	P2	1542.5	2770.5	44	SEG6	912.5	125.5	68	VDD3	4127	981
21	P3	1382.5	2770.5	45	SEG7	1072.5	125.5	69	GND	4127	1151
22	P4	1222.5	2770.5	46	SEG8	1232.5	125.5				
23	M1	1062.5	2770.5	47	SEG9	1392.5	125.5				
24	M2	902.5	2770.5	48	SEG10	1552.5	125.5				

*Note: The substrate of die must connect to GND.

3.0 PIN DESCRIPTIONS

Name	Type	Description
XTIN XTOUT	I O	- Time-based counter frequency (clock specified, LCD alternating frequency, alarm signal frequency) or system clock oscillation. - 32KHz crystal oscillator. - Oscillation stops at the execution of stop instruction.
CFIN	I	- System clock oscillation.
CFOUT	O	- Connected with ceramic resonator or crystal oscillator. - Connected with RC oscillation circuit. - Oscillation stops at the execution of stop or SLOW instruction.
S1 - 4	I	- Input port. - Input pins for data storage into RAM area (with chattering prevention). - Internal chattering prevention circuit (32ms, 8ms, 2ms selectable by application program). - Internal pull-down resistor (selectable by application program). - Internal "L"-level logic holds Tr (selectable by mask option). Note: The chattering prevention circuit parameters, 32ms, 8ms and 2ms, apply to the 32.768KHz fundamental frequency input mode.
M1 - 4	I	- Input port. - Input pins for data storage into RAM area. - Internal chattering prevention circuit (32ms, 8ms, 2ms selectable by application program). - Internal pull-down resistor (selectable by application program). - Internal "L"-level logic holds Tr (selectable by mask option). Note: The chattering prevention circuit parameters, 32ms, 8ms and 2ms, apply to the 32.768KHz fundamental frequency input mode.
IOA1-4	I/O	- Input/ Output port. - Input pins for data storage into the RAM area. - Output pin for data reading from the RAM area.
IOB1-4	I/O	- Input/ Output port. - Input pins for data storage into the RAM area. - Output pin for data reading from the RAM area.
P1 - 4	O	- Output port. - Output pin for data output from the RAM area.
INT	I	- Input port. - Input pin for external request signal. - Interrupt detection signal edge selection by mask option: falling edge and rising edge. - Internal pull-down and pull-up resistor (selectable by mask option).
VDD		- Positive supply voltage. Note: When using Li version, a capacitor must be connected across GND and VDD to prevent the logic unit from malfunctioning.
LIGHT	O	- Output port.
ALM	O	- Output port. - Output alarm signal: modulated signals with a frequency of 4kHz, 2kHz or 1kHz. In this case, these modulated frequencies are generated and then outputted if the fundamental frequency is 32.768kHz.
RES	I	- Input pin from LSI reset request signal. - Internal pull-down resistor.
GND		- Negative supply voltage.
VDD3 VDD2 VDD1		- LCD drive voltage.

Name	Type	Description
VDDO		- Positive supply voltage. * For Ag version, apply positive supply voltage to VDD1. For other than Ag version, apply positive supply voltage to VDD2.
CUP1 - 2	O	- Switching pins for supplying the LCD driving voltage to the VDD1 and VDD2 pins. - Connect the CUP1 and CUP2 pins with the nonpolarized electrolytic capacitor if 1/2 or 1/3 bias mode has been selected. - In the static mode, these pins should be left open.
COM1 - 6	O	- Output pins for supplying voltage to drive the common pins of the LCD panel. - Frequency can be doubled or quadrupled with PLA.
SEG1 - 26	O	- Output pins for LCD panel segments. * Also used as output ports with mask option.
TESTA	*	- Test signal input pin.

4.0 ABSOLUTE MAXIMUM RATINGS

at GND = 0V

Name	Symbol	Condition	Range	Unit
Maximum Supply Voltage	VDD1		-0.3 to 5.5	V
	VDD2		-0.3 to 5.5	V
	VDD3		-0.3 to 8.5	V
	VDDO		-0.3 to 5.5	V
Maximum Input Voltage	Vin1		-0.3 to VDDO+0.3	V
Maximum Output Voltage	Vout1	output port	-0.3 to VDDO+0.3	V
	Vout2	LCD segment driver	-0.3 to VDD3+0.3	V
Maximum Operating Temperature	Topg		0 to +70	^{o}C
Maximum Storage Temperature	Tstg		-25 to +125	^{o}C

5.0 ALLOWABLE OPERATING CONDITIONS

at Ta = 0 to 70^{o}C, GND = 0V

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD1	External RC Mode	1.5	5.25	V
	VDD2		3.5	5.25	V
	VDD3		3.5	8.0	V
	VDDO		1.5	5.25	V
Supply Voltage	VDD1	Crystal Mode	1.2	5.25	V
	VDD2		2.4	5.25	V
	VDD3		2.4	8.0	V
Oscillator Start-Up Voltage	VDD	Crystal Mode	1.3		V
Oscillator Sustain Voltage	VDD	Crystal Mode	1.2		V
Supply Voltage	VDD1	Ag Mode	1.2	1.65	V
Supply Voltage	VDD2	EXT-V, Li	2.4	5.25	V
Input "H" Voltage	Vih1	Ag Battery Mode	VDD1-0.7	VDD1+0.7	V
Input "L" Voltage	Vil1		-0.7	0.7	V
Input "H" Voltage	Vih2	Li Battery Mode	VDD2-0.7	VDD2+0.7	V

Input "L" Voltage	Vil2		-0.7	+0.7	V
Input "H" Voltage	Vih3	OSCIN & Ag Battery Mode	0.8 x VDD1	VDD1	V
Input "L" Voltage	Vil3		0	0.2 x VDD1	V
Input "H" Voltage	Vih4	OSCIN & Li Battery Mode	0.8 x VDD2	VDD2	V
Input "L" Voltage	Vil4		0	0.2 x VDD2	V
Input "H" Voltage	Vih5	CFIN at Li Battery or EXT-V Mode	0.8 x VDD2	VDD2	V
Input "L" Voltage	Vil5		0	0.2 x VDD2	V
Input "H" Voltage	Vih6	RC Mode	0.8 x VDDO	VDDO	V
Input "L" Voltage	Vil6		0	0.2 x VDDO	V
Operating Freq.	Fopg1	Crystal Mode	32	3580	KHz
	Fopg2	External RC Mode	32	1000	KHz
	Fopg3	CF Mode	1000	3580	KHz

6.0 ELECTRICAL CHARACTERISTICS

6.1 Input Resistance

at #1: VDD1 = 1.2V (Ag); #2: VDD2 = 2.4V (Li); #3: VDD2 = 4V (ExtV).

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
"L"-Level Hold Tr	Rllh1	Vi = 0.2VDD1, #1	10	50	200	Kohm
	Rllh2	Vi = 0.2VDD2, #2	10	40	100	Kohm
	Rllh3	Vi = 0.2VDD2, #3	5	20	50	Kohm
M/S Pull-Down Tr	Rmsd1	Vi = VDD1, #1	200	700	2000	Kohm
	Rmsd2	Vi = VDD2, #2	200	500	1000	Kohm
	Rmsd3	Vi = VDD2, #3	100	250	500	Kohm
INT Pull-Up Tr	Rintu1	Vi = VDD1, #1	200	700	2000	Kohm
	Rintu2	Vi = VDD2, #2	200	500	1000	Kohm
	Rintu3	Vi = VDD2, #3	100	250	500	Kohm
INT Pull-Down Tr	Rintd1	Vi = GND, #1	200	700	2000	Kohm
	Rintd2	Vi = GND, #2	200	500	1000	Kohm
	Rintd3	Vi = GND, #3	100	250	500	Kohm
RES Pull-Down R	Rres1	Vi = GND or VDD1, #1	5	20	50	Kohm
	Rres2	Vi = GND or VDD2, #2	5	20	50	Kohm
	Rres3	Vi = GND or VDD2, #3	5	20	50	Kohm

6.2 DC Output Characteristics

at #1: VDD1 = 1.2V (Ag); #2: VDD2 = 2.4V (Li); #3: VDD2 = 4V (ExtV).

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh1a	Ioh = -200uA, #1	Alarm Light	-0.5	-0.3	-0.1	V
	Voh2a	Ioh = -1mA, #2		-1	-0.6	-0.3	V
	Voh3a	Ioh = -3mA, #3		-1.5	-1.0	-0.5	V
Output "L" Voltage	Vol1a	Iol = 400uA, #1		-1.1	-0.9	-0.7	V
	Vol2a	Iol = 2mA, #2		-2.1	-1.8	-1.4	V
	Vol3a	Iol = 6mA, #3		-3.5	-3.0	-2.5	V
Output "H" Voltage	Voh1b	Ioh = -100uA, #1	P-port IOA-n IOB-n	-0.5	-0.3	-0.1	V
	Voh2b	Ioh = -500uA, #2		-1	-0.6	-0.3	V
	Voh3b	Ioh = -1.5mA, #3		-1.5	-1.0	-0.5	V
Output "L" Voltage	Vol1b	Iol = 200uA, #1		-1.1	-0.9	-0.7	V
	Vol2b	Iol = 1mA, #2		-2.1	-1.8	-1.4	V
	Vol3b	Iol = 3mA, #3		-3.5	-3.0	-2.5	V

6.3 Segment Driver Output Characteristics

at #1: VDD1 = 1.2V (Ag); #2: VDD2 = 2.4V (Li); #3: VDD2 = 4V (ExtV).

Name	Symb.	Condition	for	Min.	Typ.	Max.	Unit
CMOS Output Mode							
Output "H" Voltage	Voh1c	Ioh = -10uA, #1	SEG-n	-0.5	-0.3	-0.1	V
	Voh2c	Ioh = -50uA, #2		-1	-0.6	-0.3	V
	Voh3c	Ioh = -200uA, #3		-1.5	-1.0	-0.5	V
Output "L" Voltage	Vol1c	Iol = 20uA, #1		-1.1	-0.9	-0.7	V
	Vol2c	Iol = 100uA, #2		-2.1	-1.8	-1.4	V
	Vol3c	Iol = 400uA, #3		-3.5	-3.0	-2.5	V
Static Display Mode							
Output "H" Voltage	Voh1d	Ioh = -1uA, #1	SEG-n	-0.2			V
	Voh2d	Ioh = -1uA, #2		-0.2			V
	Voh3d	Ioh = -1uA, #3		-0.2			V
Output "L" Voltage	Vol1d	Iol = 1uA, #1				-1.0	V
	Vol2d	Iol = 1uA, #2				-2.2	V
	Vol3d	Iol = 1uA, #3				-3.8	V
Output "H" Voltage	Voh1e	Ioh = -10uA, #1	COM-n	-0.2			V
	Voh2e	Ioh = -10uA, #2		-0.2			V
	Voh3e	Ioh = -10uA, #3		-0.2			V
Output "L" Voltage	Vol1e	Iol = 10uA, #1				-1.0	V
	Vol2e	Iol = 10uA, #2				-2.2	V
	Vol3e	Iol = 10uA, #3				-3.8	V
1/2 Bias Display Mode							
Output "H" Voltage	Voh12f	Ioh = -1uA, #1, #2	SEG-n	-0.2			V
	Voh3f	Ioh = -1uA, #3		-0.2			V
Output "L" Voltage	Vol12f	Iol = 1uA, #1, #2				-2.2	V
	Vol3f	Iol = 1uA, #3				-3.8	V
Output "H" Voltage	Voh12g	Ioh = -10uA, #1, #2	COM-n	-0.2			V
	Voh3g	Ioh = -10uA, #3		-0.2			V
Output "M" Voltage	Vom12g	Iol/h= +/-10uA, #1, #2		-1.4		-1.0	V
	Vom3g	Iol/h= +/-10uA, #3		-2.2		-1.8	V
Output "L" Voltage	Vol12g	Iol = 10uA, #1				-2.2	V
	Vol3g	Iol = 10uA, #3				-3.8	V
1/3 Bias Display Mode							
Output "H" Voltage	Voh12j	Ioh = -1uA, #1, #2	SEGn	-0.2			V
	Voh3j	Ioh = -1uA, #3		-0.2			V
Output"M1" Voltage	Vom12j	Iol/h= +/-10uA, #1, #2		-1.4		-1.0	V
	Vom13j	Iol/h= +/-10uA, #3		-2.2		-1.8	V
Output"M2" Voltage	Vom22j	Iol/h= +/-10uA, #1, #2		-2.6		-2.2	V
	Vom23j	Iol/h= +/-10uA, #3		-4.2		-3.8	V
Output "L" Voltage	Vol2j	Iol = 1uA, #1,#2				-3.4	V
	Vol3j	Iol = 1uA, #3				-5.8	V
Output "H" Voltage	Voh2k	Ioh = -10uA, #1,#2	COMn	-0.2			V
	Voh3k	Ioh = -10uA, #3		-0.2			V
Output"M1" Voltage	Vom12k	Iol/h= +/-10uA, #1, #2		-1.4		-1.0	V
	Vom13k	Iol/h= +/-10uA, #3		-2.2		-1.8	V
Output"M2" Voltage	Vom22k	Iol/h= +/-10uA, #1, #2		-2.6		-2.2	V
	Vom23k	Iol/h= +/-10uA, #3		-4.2		-3.8	V
Output "L" Voltage	Vol2k	Iol = 10uA, #1,#2				-3.4	V

	Vol3k	Iol = 10uA, #3				-5.8	V

7.0 INSTRUCTION TABLE

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Ly,Ry	0000 000L LLLL YYYY	(Ly)	• ((Ry) => decoder)	Ly=0000X No Use
LCB	Ly,Ry	0000 001L LLLL YYYY	(Ly)	• ((Ry) => decoder)	Ly=0000X No Use
LCP	Ly,Ry	0000 010L LLLL YYYY	(Ly)	• (Rx),(AC)	Ly=0000X No Use
OPA	Rx	0000 1100 0XXX XXXX	Port(IOA)	• (Rx)	IOA • O/P
OPB	Rx	0000 1110 0XXX XXXX	Port(IOB)	• (Rx)	IOB • O/P
MVH	Rx	0001 1010 0XXX XXXX	(@H)	• (Rx)	
MRA	Rx	0001 1010 1XXX XXXX	CF	• (Rx3)	CF
MVL	Rx	0001 1011 0XXX XXXX	(@L)	• (Rx)	
OPP	Rx	0001 1100 0XXX XXXX	Port(P)	• (Rx)	
OPPS	Rx,D	0001 1101 DXXX XXXX	P1,2,3,4	• (Rx0)(Rx1),D,Pulse	
INC*	Rx	0001 1110 0XXX XXXX	(AC),(Rx)	• (Rx)+1	CF
INC*	@HL	0001 1110 1000 0000	(AC),(@HL)	• (@HL)+1	CF
DEC*	Rx	0001 1111 0XXX XXXX	(AC),(Rx)	• (Rx)-1	CF
DEC*	@HL	0001 1111 1000 0000	(AC),(@HL)	• (@HL)-1	CF
ADC	Rx	0010 0000 0XXX XXXX	(AC)	• (Rx)+(AC)+(CF)	CF
ADC	@HL	0010 0000 1000 0000	(AC)	• (@HL)+(AC)+(CF)	CF
ADC*	Rx	0010 0001 0XXX XXXX	(AC),(Rx)	• (Rx)+(AC)+(CF)	CF
ADC*	@HL	0010 0001 1000 0000	(AC),(@HL)	• (@HL)+(AC)+(CF)	CF
SBC	Rx	0010 0010 0XXX XXXX	(AC)	• (Rx)+(AC)B+(CF)	CF
SBC	@HL	0010 0010 1000 0000	(AC)	• (@HL)+(AC)B+(CF)	CF
SBC*	Rx	0010 0011 0XXX XXXX	(AC),(Rx)	• (Rx)+(AC)B+(CF)	CF
SBC*	@HL	0010 0011 1000 0000	(AC),(@HL)	• (@HL)+(AC)B+(CF)	CF
ADD	Rx	0010 0100 0XXX XXXX	(AC)	• (Rx)+(AC)	CF
ADD	@HL	0010 0100 1000 0000	(AC)	• (@HL)+(AC)	CF
ADD*	Rx	0010 0101 0XXX XXXX	(AC),(Rx)	• (Rx)+(AC)	CF
ADD*	@HL	0010 0101 1000 0000	(AC),(@HL)	• (@HL)+(AC)	CF
SUB	Rx	0010 0110 0XXX XXXX	(AC)	• (Rx)+(AC)B+1	CF
SUB	@HL	0010 0110 1000 0000	(AC)	• (@HL)+(AC)B+1	CF
SUB*	Rx	0010 0111 0XXX XXXX	(AC),(Rx)	• (Rx)+(AC)B+1	CF
SUB*	@HL	0010 0111 1000 0000	(AC),(@HL)	• (@HL)+(AC)B+1	CF
ADN	Rx	0010 1000 0XXX XXXX	(AC)	• (Rx)+(AC)	
ADN	@HL	0010 1000 1000 0000	(AC)	• (@HL)+(AC)	
ADN*	Rx	0010 1001 0XXX XXXX	(AC),(Rx)	• (Rx)+(AC)	
ADN*	@HL	0010 1001 1000 0000	(AC),(@HL)	• (@HL)+(AC)	
AND	Rx	0010 1010 0XXX XXXX	(AC)	• (Rx) AND (AC)	
AND	@HL	0010 1010 1000 0000	(AC)	• (@HL) AND (AC)	
AND*	Rx	0010 1011 0XXX XXXX	(AC),(Rx)	• (Rx) AND (AC)	
AND*	@HL	0010 1011 1000 0000	(AC),(@HL)	• (@HL) AND (AC)	
EOR	Rx	0010 1100 0XXX XXXX	(AC)	• (Rx) EOR (AC)	

Instruction	Machine Code	Function	Flag/Remark
EOR @HL	0010 1100 1000 0000	(AC) • (@HL) EOR (AC)	
EOR* Rx	0010 1101 0XXX XXXX	(AC),(Rx) • (Rx) EOR (AC)	
EOR* @HL	0010 1101 1000 0000	(AC),(@HL) • (@HL) EOR (AC)	
OR Rx	0010 1110 0XXX XXXX	(AC) • (Rx) OR (AC)	
OR @HL	0010 1110 1000 0000	(AC) • (@HL) OR (AC)	
OR* Rx	0010 1111 0XXX XXXX	(AC),(Rx) • (Rx) OR (AC)	
OR* @HL	0010 1111 1000 0000	(AC),(@HL) • (@HL) OR (AC)	
ADCI Ry,D	0011 0000 DDDD YYYY	(AC) • (Ry)+D+(CF)	CF
ADCI* Ry,D	0011 0001 DDDD YYYY	(AC),(Ry) • (Ry)+D+(CF)	CF
SBCI Ry,D	0011 0010 DDDD YYYY	(AC) • (Ry)+(D)B+(CF)	CF
SBCI* Ry,D	0011 0011 DDDD YYYY	(AC),(Ry) • (Ry)+(D)B+(CF)	CF
ADDI Ry,D	0011 0100 DDDD YYYY	(AC) • (Ry)+D	CF
ADDI* Ry,D	0011 0101 DDDD YYYY	(AC),(Ry) • (Ry)+D	CF
SUBI Ry,D	0011 0110 DDDD YYYY	(AC) • (Ry)+(D)B+1	CF
SUBI* Ry,D	0011 0111 DDDD YYYY	(AC),(Ry) • (Ry)+(D)B+1	CF
ADNI Ry,D	0011 1000 DDDD YYYY	(AC) • (Ry)+D	
ADNI* Ry,D	0011 1001 DDDD YYYY	(AC),(Ry) • (Ry)+D	
ANDI Ry,D	0011 1010 DDDD YYYY	(AC) • (Ry) AND D	
ANDI* Ry,D	0011 1011 DDDD YYYY	(AC),(Ry) • (Ry) AND D	
EORI Ry,D	0011 1100 DDDD YYYY	(AC) • (Ry) EOR D	
EORI* Ry,D	0011 1101 DDDD YYYY	(AC),(Ry) • (Ry) EOR D	
ORI Ry,D	0011 1110 DDDD YYYY	(AC) • (Ry) OR D	
ORI* Ry,D	0011 1111 DDDD YYYY	(AC),(Ry) • (Ry) OR D	
IPS Rx	0100 0000 0XXX XXXX	(AC),(Rx) • Port(S)	
MSD Rx	0100 0000 1XXX XXXX	(AC),(Rx) • WDF,CSF	
IPM Rx	0100 0001 0XXX XXXX	(AC),(Rx) • Port(M)	
IPA Rx	0100 0010 0XXX XXXX	(AC),(Rx) • Port(IOA)	
IPA* Rx	0100 0010 1XXX XXXX	(AC),(Rx) • Port(IOA)	IOA • I/P
IPB Rx	0100 0011 0XXX XXXX	(AC),(Rx) • Port(IOB)	
IPB* Rx	0100 0011 1XXX XXXX	(AC),(Rx) • Port(IOB)	IOB • I/P
MSB Rx	0100 0100 0XXX XXXX	(AC),(Rx) • STS2	B0: BCF B1: SCF1(MPT) B2: SCF2(HRF) B3: SCF3(SPT)
STA Rx	0100 0101 0XXX XXXX	(Rx) • (AC)	
STA @HL	0100 0101 1000 0000	(@HL) • (AC)	
SR0 Rx	0100 0110 0XXX XXXX	ACn, Rxn • Rx(n+1) AC3, Rx3 • 0	
SR1 Rx	0100 0110 1XXX XXXX	ACn, Rxn • Rx(n+1) AC3, Rx3 • 1	
SL0 Rx	0100 0111 0XXX XXXX	ACn, Rxn • Rx(n-1) AC0, Rx0 • 0	
SL1 Rx	0100 0111 1XXX XXXX	ACn, Rxn • Rx(n-1) AC0, Rx0 • 1	
LDS Rx,D	0100 1DDD DXXX XXXX	(AC),(Rx) • D	
LDH Rx,@HL	0101 0000 0XXX XXXX	(Rx) • H(T@HL)	
DAA	0101 0100 0000 0000	(AC) • BCD(AC)	CF

Instruction	Machine Code	Function	Flag/Remark
DAA* Rx	0101 0110 0XXX XXXX	(AC),(Rx) • BCD(AC)	CF
DAA* @HL	0101 0111 0000 0000	(AC),(@HL) • BCD(AC)	CF
LDL Rx,@HL	0101 1000 0XXX XXXX	(Ry) • L(T@HL)	
DAS	0101 1100 0000 0000	(AC) • BCD(AC)	CF
DAS* Rx	0101 1110 0XXX XXXX	(AC),(Rx) • BCD(AC)	CF
DAS* @HL	0101 1111 0000 0000	(AC),(@HL) • BCD(AC)	CF
MSC Rx	0110 0000 0XXX XXXX	(AC),(Rx) • STS3	B0: SCF4(INT) B1: SCF5(TMR) B2: PH15 B3: SCF7(PDV)
MAF Rx	0110 0010 0XXX XXXX	(AC),(Rx) • STS1	TF2: AC=0 TF3: CF
LDA Rx	0110 1110 1XXX XXXX	(AC) • (Rx)	
LDA @HL	0110 1111 1000 0000	(AC) • (HL)	
MRW Ry,Rx	0111 0YYY YXXX XXXX	(AC),(Ry) • (Rx)	
MWR Rx,Ry	0111 1YYY YXXX XXXX	(AC),(Rx) • (Ry)	
JB0 X	1000 0XXX XXXX XXXX	(PC) • X	if (AC0) = 1
JB1 X	1000 1XXX XXXX XXXX	(PC) • X	if (AC1) = 1
JB2 X	1001 0XXX XXXX XXXX	(PC) • X	if (AC2) = 1
JB3 X	1001 1XXX XXXX XXXX	(PC) • X	if (AC3) = 1
JNZ X	1010 0XXX XXXX XXXX	(PC) • X	if (AC) ≠ 0
JNC X	1010 1XXX XXXX XXXX	(PC) • X	if (CF) = 0
JZ X	1011 0XXX XXXX XXXX	(PC) • X	if (AC) = 0
JC X	1011 1XXX XXXX XXXX	(PC) • X	if (CF) = 1
JMP X	1100 0XXX XXXX XXXX	(PC) • X	
CALL X	1100 1XXX XXXX XXXX	(STACK) • (PC)+1 (PC) • X	
RTS	1101 0000 0000 0000	(PC) • (STACK)	CALL Return
		(PC) • (STACK) (AC) • (ACR) CF • CFR	INT Return CF
SCC S,X	1101 0010 0000 SXXX	S: 1 / 0	
		Port select: S port / M port	
		X2,X1,X0: 1 0 0 / 0 1 0	0 0 1
		Port(M)-CK: PH6 / PH8	PH10
LCD Ly,@HL	1101 100L LLLL 0000	Ly • ((T@HL) => decoder)	Ly=000- No Use
SMS X	1110 0000 000X XXXX	SEF4 • X4 SEF0-3 • X0-3	M1-4 Enable S1-4 Enable
FAST	1110 0010 0000 0000	SCLK --> HIGH SPEED CLOCK	
SLOW	1110 0011 0000 0000	SCLK --> LOW SPEED CLOCK	
TMS C,X	1110 010C CCXX XXXX	TIMER • X0-5	
		C2,C1,C0: 1 0 0 / 0 1 0	0 0 1
		Timer-CK: PH15 / PH9	PH3

Instruction	Machine Code	Function	Flag/Remark
SF X	1110 1000 0XXX XXXX	X6 : M-PORT Pull-Low X5 : S-PORT Pull-Low X4 : WDOG Set X3 : HALT After Light X2 : LIGHT ON X1 : BCF Set X0 : CF Set	 WDOG BCF CF
RF X	1110 1100 0XXX XXXX	X6 : M-PORT Low-L-H X5 : S-PORT Low-L-H X4 : WDOG Reset X2 : LIGHT OFF X1 : BCF Reset X0 : CF Reset	 WDOG BCF CF
ALM X	1110 111X XXXX XXXX	X8,X7,X6 : 1 0 0 / X 1 0 / X 1 1 / X 1 1 / 0 0 0 Signal : DC 1 / 1K / 2K / 4K / DC 0 Xn = 1 : X5 / X4 / X3 / X2 / X1 / X0 Signal : 1 Hz / 2 Hz / 4Hz / 8Hz / 16Hz / 32Hz	
SIE X	1111 0000 XXXX XXXX	X5-7 : HEF1-3 is Enabled X0-3 : IEF0-3 is Enabled	
SIE* X	1111 0100 0000 XXXX	X0-3 : IEF0-3 is Enabled	
PLC X	1111 100X XXXX XXXX	X0-3 : Reset HRF0-3 X8 : Reset PH11-15	
SRE X	1111 0110 000X XXXX	X0 : SEF1 is Enabled X1 : SEF2 is Enabled X2 : SEF3 is Enabled X3 : SEF4 is Enabled X4 : SEF5 is Enabled	
HALT	1111 1100 0000 0000		
STOP	1111 1111 1111 1111		

Symbol Description

AC : Accumulator
ACn : Accumulator Bit N
Rx : Memory of Address X
Rxn : Memory Bit N of Address X
Ry : Memory of Working Register Y
HL : Index Register
@HL : Memory of Index Address
Tx : Data of Look-up Table
D : Immediate Data
Lx : LCD Latch
() : Content of Register
H($T_{@HL}$): High Nibble of Table ROM
WDF : Watchdog Enable Flag
PC : Program Counter
X : Address
CF : Carry Flag
BCF : Backup Flag
IEFn : Interrupt Enable Flag
HEFn : HALT Release Enable Flag
HRFn : HALT Release Flag
SEFn : Switch Enable Flag
SCFn : Start Condition Flag
SREn : Stop Release Enable Flag
()B : Complement Data of Register
L($T_{@HL}$): Low Nibble of Table ROM
CSF : Clock Source Flag