



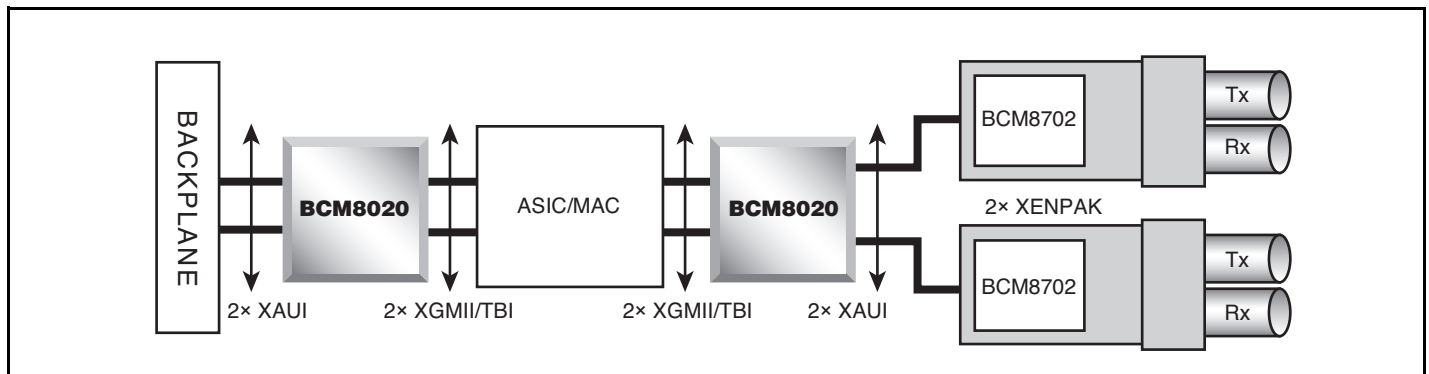
8-CHANNEL MULTIRATE 1.0–3.2-GBPS TRANSCEIVER

FEATURES

- **8 independent transceivers supporting multiple data rates from 1.0 Gbps to 3.2 Gbps including 1.06 Gbps, 1.25 Gbps, 2.12 Gbps, 2.488 Gbps, 2.5 Gbps, 2.667 Gbps, 3.125 Gbps, and 3.1875 Gbps**
- **Multiconfigurability to support various operating modes**
 - Eight Independent 1.0 to 3.2-Gbps SerDes Channels
 - Dual quad 1.0 to 3.2-Gbps SerDes with channel alignment
 - SerDes-to-SerDes retimer mode: CML and XAUI interfaces
 - Full mesh switching maps any XAUI port to any XGMII port for full redundancy on both transmitter and receiver
 - Selectable TBI DDR/RTBI or XGMII parallel interface
 - HSTL (1.8V or 1.5V) and SSTL_2 parallel interface
- **Low power dissipation**
 - Less than 300 mW per transceiver channel including I/O
- **High performance programmable Rx equalization and Tx pre-emphasis**
 - Tx pre-emphasis for interoperability with CML SerDes
 - Rx equalization for copper interconnects
- **Enhanced test capability**
 - Serial and parallel loopback, BIST, 10G BERT, and random Ethernet packet generation
 - IEEE (1149.1) JTAG
- **Compact 23-mm × 23-mm package with no external components required**
 - No requirement for heat sink or airflow

SUMMARY OF BENEFITS

- One device supports a variety of applications including Gigabit Ethernet, 1× and 2× Fibre Channel, OC-48 SONET (with/without FEC), Infiniband, 10-Gigabit Ethernet, 10-Gigabit Fibre Channel, or others.
- Flexible architecture supports programmable configurations enabling an aggregate data transfer rate of over 20 Mbps. Built-in redundancy mode provides high availability to support critical line side or backplane applications. The high-speed to high-speed retimer mode extends the use of longer traces on line card designs.
- Advanced 0.13- μ CMOS process technology provides unparalleled performance while achieving the lowest possible power consumption.
- Eases linecard designs to allow for multiple connectors or low-cost PCB materials such as FR4.
- Drive PMD devices or back-plane directly with no external clean-up circuit required.
- Simplifies manufacturability with integrated Built-in self-test (BIST), high-speed and low-speed loopbacks, and programmable PRBS generator/checker.
- Decreases complexity and reduces board space on multi-channel line-card designs.



2 Independent Quad SerDes Application Diagram