

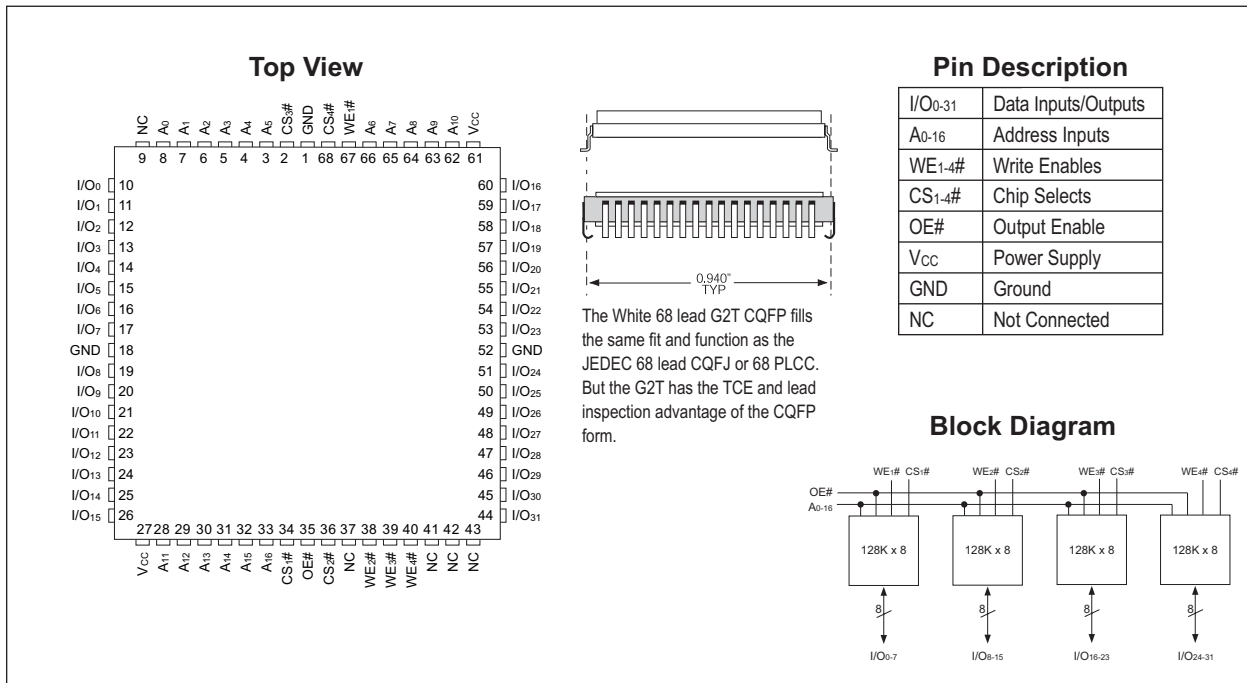
# 128Kx32 SRAM MULTICHIP PACKAGE, RADIATION TOLLERANT

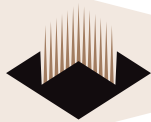
## FEATURES

- Access Times of 35, 45, 55ns
- Packaging
  - 68 lead, 22.4mm CQFP (G2T), 4.57mm (0.180"), (Package 509)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Low Power Data Retention
- Commercial, Industrial and Military Temperature Ranges
- 5V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  - WS128K32-XG2TXE – 8 grams typical
- Radiation tolerant with epitaxial layer on die.
- 6T memory cells provide excellent protection against soft errors

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

FIGURE 1 – PIN CONFIGURATION FOR WS128K32N-XG2TXE





## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

## TRUTH TABLE

CS#	OE#	WE#	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temp. (MIL)	T <sub>A</sub>	-55	+125	°C

## CAPACITANCE

T<sub>A</sub> = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF
WE1-4# capacitance CQFP G2T	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20	pF
CS1-4# capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	20	pF
Data# I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

## RADIATION CHARACTERISTICS

Total Dose (TM1019.5)			Latch-up 25°C V <sub>CC</sub> Max (MeV/mg/cm <sup>2</sup> )	SEU LET Threshold (V <sub>CC</sub> MIN) (MeV/mg/cm <sup>2</sup> )	Cross Section /BIT (E-6 cm <sup>2</sup> )
Functional (Krad)	Parametric (Krad)				
		Typical I <sub>ocsb</sub> (mA)			
30	30	1.2	>100	2	0.2

## DC CHARACTERISTICS

V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	µA
Output Leakage Current	I <sub>LO</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	µA
Operating Supply Current	I <sub>CC</sub>	CS# = V <sub>IL</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		520	mA
Standby Current	I <sub>SB</sub>	CS# = V <sub>IH</sub> , OE# = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		8	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -40mA, V <sub>CC</sub> = 4.5	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

## DATA RETENTION CHARACTERISTICS

-55°C ≤ T<sub>A</sub> ≤ +125°C

Characteristic	Sym	Conditions	Min	Max	Units
Data Retention Voltage	V <sub>CC</sub>	V <sub>CC</sub> = 2.0V	2	—	V
Data Retention Quiescent Current	I <sub>CCDR</sub>	CS ≥ V <sub>CC</sub> - 0.2V	—	1	mA
Chip Disable to Data Retention Time (1)	T <sub>CDR</sub>	V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V	0	—	ns
Operation Recovery Time (1)	T <sub>R</sub>	or V <sub>IN</sub> ≤ 0.2V	T <sub>RC</sub>	—	ns

NOTE: Parameter guaranteed, but not tested.



**AC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	35		45		55		ns
Address Access Time	t <sub>AA</sub>		35		45		55	ns
Output Hold from Address Change	t <sub>OH</sub>	3		3		3		ns
Chip Select Access Time	t <sub>ACS</sub>		35		45		55	ns
Output Enable to Output Valid	t <sub>OE</sub>		15		20		30	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	3		3		3		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		20		20		20	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		12		15		20	ns

1. This parameter is guaranteed by design but not tested.

**AC CHARACTERISTICS**

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

Parameter	Symbol	-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	35		45		55		ns
Chip Select to End of Write	t <sub>CW</sub>	25		35		45		ns
Address Valid to End of Write	t <sub>AW</sub>	25		35		45		ns
Data Valid to End of Write	t <sub>DW</sub>	20		25		25		ns
Write Pulse Width	t <sub>WP</sub>	25		35		45		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	0		0		0		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		10		15		20	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**FIGURE 2 – AC TEST CIRCUIT**

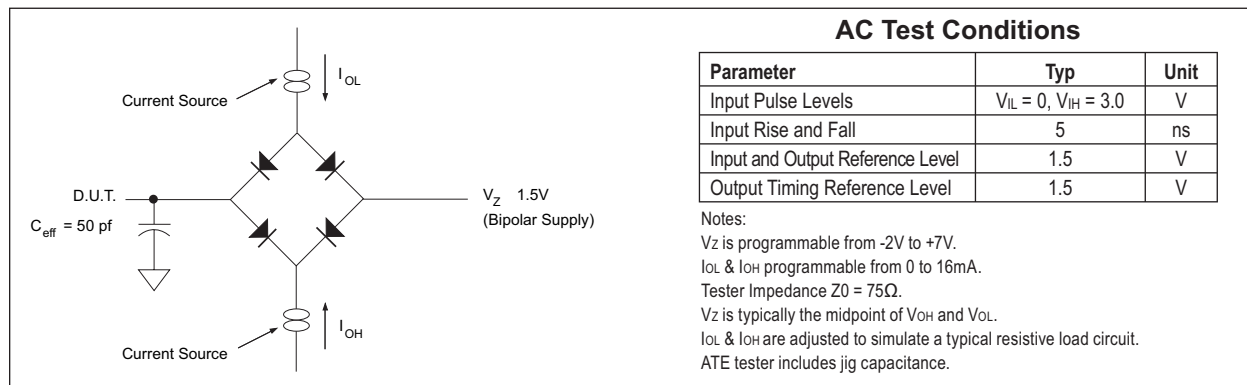




FIGURE 3 – TIMING WAVEFORM - READ CYCLE

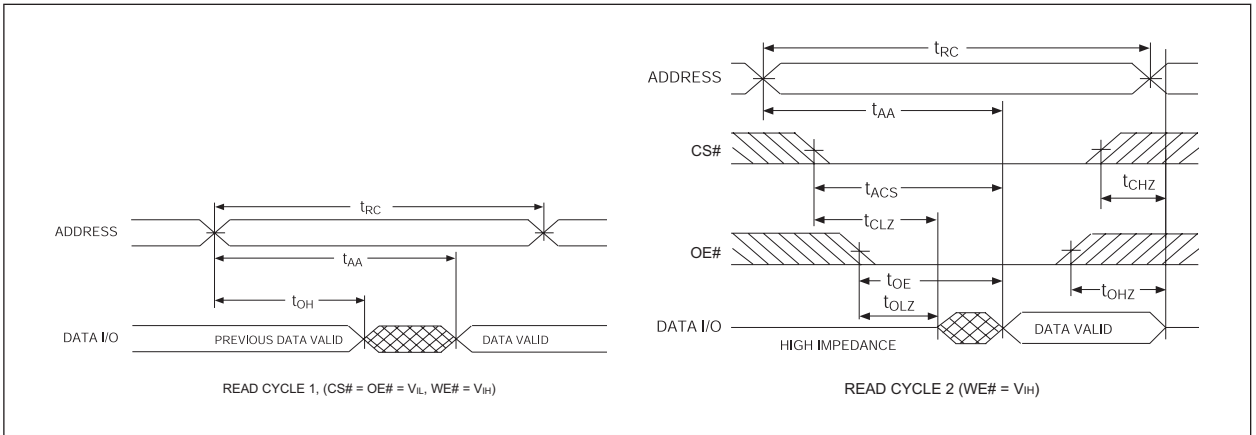


FIGURE 4 – WRITE CYCLE - WE# CONTROLLED

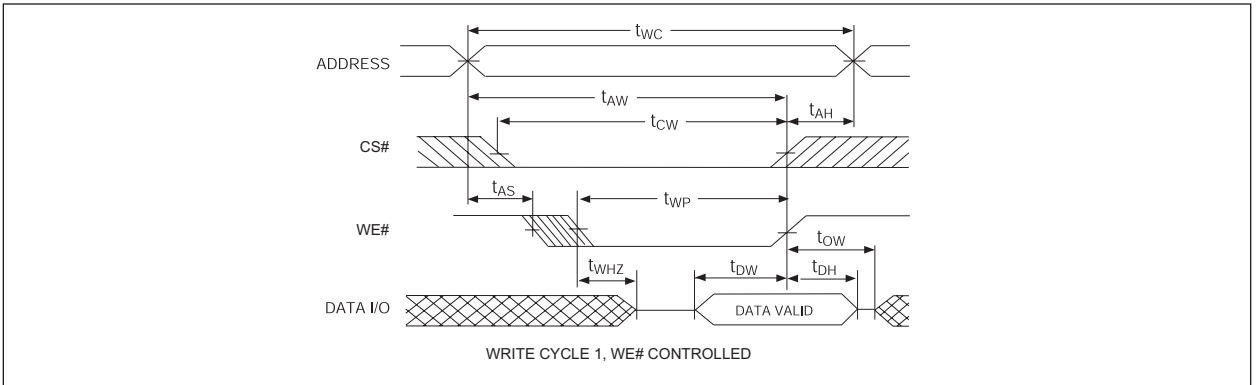
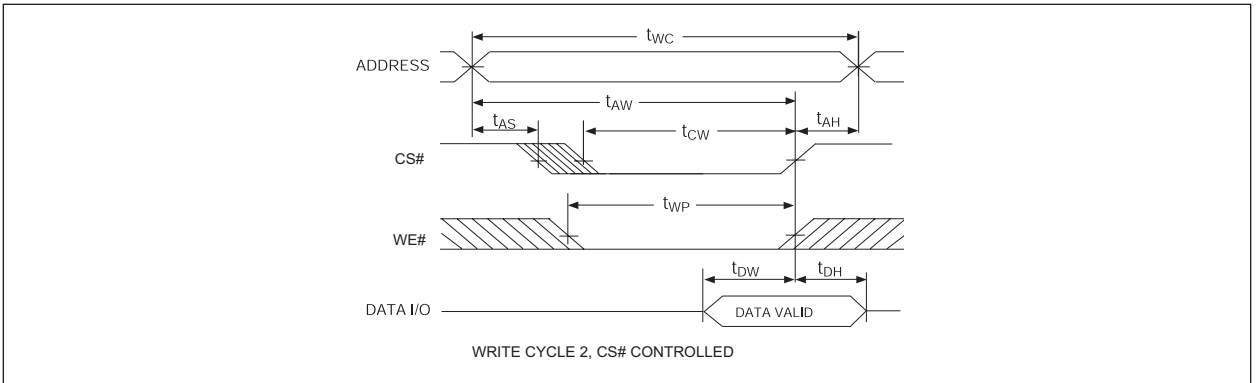
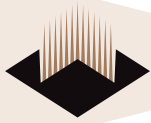
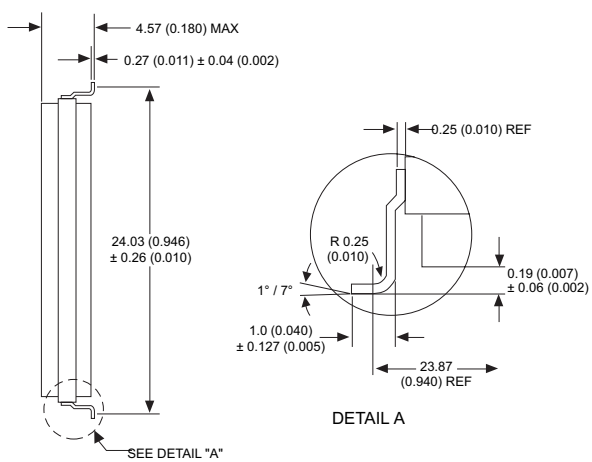
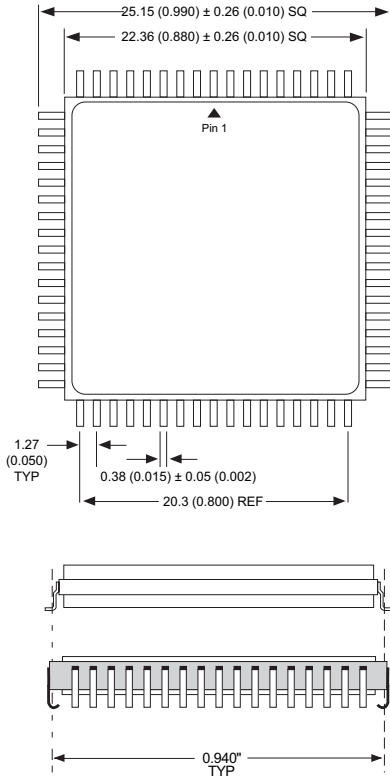


FIGURE 5 – WRITE CYCLE - CS# CONTROLLED





PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



## ORDERING INFORMATION

**W S 128K 32 X - XXX X X E X**

**LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

**E = Epitaxial Layer on die**

**DEVICE GRADE:**

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

G2T = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)

**ACCESS TIME (ns)**

**IMPROVEMENT MARK:**

N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades

**ORGANIZATION, 128Kx32**

User configurable as 256Kx16 or 512Kx8

**SRAM**

**WHITE ELECTRONIC DESIGNS CORPORATION**

\* Low Power Data Retention only available in G2T Package Type