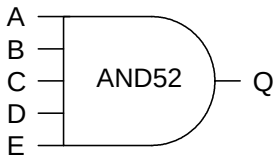
AND52 is a 5-input AND gate with 2x drive strength.

Truth Table

A	B	C	D	E	Q
L	X	X	X	X	L
X	L	X	X	X	L
X	X	L	X	X	L
X	X	X	L	X	L
X	X	X	X	L	L
H	H	H	H	H	H



Capacitance

	Ci (pF)
A	0.054
B	0.053
C	0.059
D	0.057
E	0.058

Area

0.95 $mils^2$

Power

4.05 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.2	L = 1.4	L = 2.0	L = 0.2	L = 1.4	L = 2.0
Delay A to Q	tpdar	0.55	1.91	2.64	0.60	1.96	2.65
	tpdaf	0.61	1.73	2.28	0.98	2.10	2.64
Delay B to Q	tpdbr	0.60	2.02	2.65	0.64	2.01	2.71
	tpdbf	0.70	1.84	2.37	1.07	2.18	2.72
Delay C to Q	tpdcr	0.65	2.05	2.69	0.65	2.00	2.69
	tpdcf	0.79	1.93	2.50	1.17	2.30	2.83
Delay D to Q	tpddr	0.68	2.01	2.71	0.62	1.98	2.67
	tpddf	0.89	2.03	2.61	1.24	2.41	2.93
Delay E to Q	tpder	0.68	2.07	2.74	0.59	1.94	2.63
	tpdef	0.97	2.08	2.64	1.33	2.49	3.02
Output Slope A to Q	op_slar	0.98	5.22	7.31	0.93	5.18	7.47
	op_slaf	0.71	3.62	5.26	0.71	3.68	5.25
Output Slope B to Q	op_slbr	1.00	5.30	7.46	0.93	5.27	7.31
	op_slbf	0.75	3.55	5.06	0.75	3.53	5.05
Output Slope C to Q	op_slcr	0.97	5.21	7.30	0.96	5.23	7.45
	op_slcf	0.78	3.57	5.11	0.78	3.61	5.01
Output Slope D to Q	op_sldr	0.98	5.18	7.30	0.97	5.22	7.46
	op_sldf	0.81	3.63	5.12	0.81	3.63	5.07
Output Slope E to Q	op_sler	0.98	5.27	7.37	0.96	5.22	7.43
	op_slef	0.85	3.80	5.06	0.82	3.72	5.05