# PRODUCT INFORMATION

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## Flash Memory for Portable Telephones Developed Jointly with SST

## Industry's first three-bank flash memory with on-chip EEPROM

### LE28BU166

### Overview

Due to the diversity and range of services offered and advances in the number of functions, the level of those functions, and miniaturization of the telephones themselves, the portable telephone market has continued to grow with no signs of market saturation. To respond to the needs of this expanding market, flash memory, which is one of the most important components used in portable telephones, has advanced in many ways; in increased functionality, in increased performance, in miniaturization, in reduced power consumption, and in increased capacity.

In the fall of 1997, Sanyo developed the industry's first MCP (multi-chip package) product that combined both flash memory and SRAM in a single package. This development was but one aspect of Sanyo's commitment to applying its flash memory expertise to the portable telephone market, a commitment that is a main pillar of Sanyo's flash memory business. Now, in a joint development effort with SST (Silicon Storage Technology, Inc.), Sanyo's partner in the flash memory business, Sanyo has developed the LE28BU166 (product name: Flashbank) flash memory that integrates 16M bits of flash memory and 64K bits of EEPROM on a single chip for the first time in the industry.

Up to now, portable telephones have stored both information that requires frequent updating (such as base station information and usage charge information) and information such as the product serial number in EEPROM. Previously, either that EEPROM was provided as a separate chip or part of the flash memory was used instead, with the latter technique requiring additional software support.

Other semiconductor manufacturers that have attempted to include EEPROM on the same chip have used a stacked gate cell. However, this has proved problematic when EEPROM is combined with flash memory, since a much larger chip area is required. Furthermore, this problem becomes more severe as the block erase range is reduced.

The Flashbank products that Sanyo has now developed take advantage of the feature of the split gate structure that allows the block erase range to be reduced without increasing the chip size to include EEPROM in a flash memory product. Furthermore, this product adopts a three bank structure consisting of two 8M flash memory blocks and a 64K EEPROM block. Since data can be stored or read out at the same time from these banks, end product operational response can be improved by, for example,

having the telephone read out its program while storing audio signal or other data at the same time.

Furthermore, this product takes advantage of the high-speed rewrite characteristic that is a feature of the split gate structure, and allows data that was stored in external SRAM in previous applications to be stored in flash memory. This allows end product manufacturers to reduce the SRAM capacity and simplify circuit designs.

The Sanyo Flashbank product can provide increased reliability and miniaturization in portable telephones by allowing circuits that previously required two chips, a flash memory chip and an EEPROM chip, to be implemented with a single chip.


Earlier Two-Chip Structure　　Single-Chip Flashbank

The Flashbank device operates on a power supply voltage of between 2.2 and 2.8 V, and provides high-speed readout at either 90 or 120 ns. Furthermore, it achieves the low current drain required in portable telephones, namely 10 mA (typical) in readout mode and 2 μA (typical) in standby mode. Furthermore, it takes advantage of the features of the split gate structure to provide an extensive set of attractive features, including a small sector size (1K words), a short erase time (about 1/100 of that required by flash memory products from other companies), and does not require verification of write and erase operations.

The Flashbank device is available in both 48-pin TSOP (10 × 14 mm) and 48-pin FBGA (10 × 8 mm) packages to contribute to end product miniaturization.

The Flashbank product will be available in sample quantities from mid-July this year. Future plans include an MCP product that combines this chip with SRAM in a single package. This product is under development now, and we plan on providing it in sample quantities by the end of the year. We are also developing a 32M Flashbank product jointly with SST, and plan on providing this product in sample quantities by the end of the year as well.

## Functions and Specifications

- Integrates a 3-bank 16.064 megabit memory system (8M flash + 8M flash + 64K EEPROM) on a.single chip. Provides circuit simplification for earlier systems that used an external EEPROM, and provides easier software development and improved performance in systems that used software processing for this function.

- High-speed rewrite that only requires 30 ms per flash memory sector. This allows audio data to be stored in a flash memory bank and thus allows the capacity of external SRAM to be reduced.
- Low supply voltage: 2.2 to 2.8 V single-voltage power supply
- Fast read access: 90 or 120 ns
- Low power: 10 mA (typical) read current, 2 μA (typical) standby mode current
- High-speed chip erase: 300 ms
- OTP (one-time programmable) function for the EEPROM block
- FBGA package adopted (10 × 8 mm)
- Small sector size: 1K words
- EEPROM can be rewritten in word units.
- Supports the industry standard Common Flash Memory Interface.

## Sample Availability

Sample of the LE28BU166 will be available in the middle of June 1999; production quantities will be anticipated in the spring of 2000.

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