

Specification Update

1. Revision History

Date of revision	Version	Description
August 23, 1999	Rev. A	Creation

World Wide Web: <http://www.temic-semi.de/>

Product Hotline: C251@temic.fr

Tools Hotline: x51_tools@temic.fr

2. Preface

This document is an update to the specifications contained in Table 1.

Table 1. Affected Documents/Related Documents

Title	Reference
TSC8x251G2D Datasheet	Rev. A - May 7, 1999
TSC80251G1D Design Guide - October 1998	Rev. C - October 8, 1998
TSC80251 Programmer's Guide 1996	Rev. B - October 23, 1996

3. Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specifications (see Table 1).

Table 2. Codes Used in Summary Table

Page	
(Page)	Page location of item in this document.
Status	
Doc	Document change or update will be implemented.
Fix	This erratum is intended to be fixed in a future version of the component.
No Fix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.

4. Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to TSC8x251G2D derivatives. TEMIC may fix some of the errata in a future version of the component, and account for the other outstanding issues through documentation or specification changes as noted.

Table 3. Errata List

TEMIC Reference	Mask Number	Page	Status	Errata
C251G2D-01	5142A	3	Eval	Power Down Mode Current out of Specification in Romless Mode
C251G2D-02	5142A	3	Eval	Power-Fail Threshold out of Specification
C251G2D-03	5142A	4	Eval	I2C Data Transmission in Slave Transmitter Mode

Table 4. Specification Changes

TEMIC Reference	Mask Number	Page	Status	Specification Changes
				None

Table 5. Specification Clarifications

TEMIC Reference	Mask Number	Page	Status	Specification Clarifications
				None

Table 6. Documentation Changes

TEMIC Reference	Mask Number	Page	Status	Documentation Changes
				None

5. Errata

Reference	Erratum
C251G2D-01	Power Down Mode Current out of Specification in Romless Mode

Problem

I_{PD} is out of specification when EA# pin is tied to a low level.

Implication

The ROMless products and EPROM and ROM products used as ROMless (EA#=0) are consuming extra current in Power Down mode. Table 7 shows the Power Down current maximum value and specification for High Speed and Low Voltage versions.

Table 7. DC Characteristics; $T_A = -40$ to $+85^\circ\text{C}$

Symbol	Parameter	Max Spec	Max Value	Units	Test Conditions
I_{PD}	Power-Down Current	20	35	μA	$V_{RET} < V_{DD} < 5.5 \text{ V}$
I_{PD}	Power-Down Current	10	20	μA	$V_{RET} < V_{DD} < 3.6 \text{ V}$

Workaround

No workaround is proposed.

Affected Products

All TSC8x251G2D are affected.

Reference	Erratum
C251G2D-02	Power-Fail Threshold out of Specification

Problem

The tolerance on the power fail reset voltage thresholds is out of specification.

Implication

The device may never exit reset at power-up when power fail reset is enabled.

Workaround

Some devices may need a higher voltage to exit reset. Then RSTD bit has to be set in POWM register to disable the Power-Fail Reset detector before the voltage is reduced.

Affected Products

This feature has been removed from ROMless, Mask ROM and OTP devices which are then not affected.

All TSC87251G2D EPROM devices are affected.

Reference	Erratum
C251G2D-03	I ² C Data Transmission in Slave Transmitter Mode

Problem

When in slave transmitter mode, if the slave transmits a data starting with a low level on the bus (MSB is logic 0), data set-up time is not respected and leads to a bus error.

Implication

When this errata appears, a START condition is delivered on the bus during the transfer leading to a bus error (state 00). The transfer is then interrupted and slave does not continue to transmit the data to the master.

Workaround

The workaround proposed consist in removing the set-up violation by stretching the SDA line (P1.7) when the MSB of the data to transmit is logic 0. This workaround must be implemented in states A8h, B0h, and B8h when a data is written to the serial data register (SSDAT).

In assembler the workaround is:

```

mov     A,data           ; read data to transmit
mov     SSDAT,A          ; load transmit buffer
jnb     ACC.7,Msb_tst    ; test MSB
clr     SDA              ; stretch data line (P1.7) to low level
Msb_tst: mov     SCON,#40h ; or 44h: clear SSI flag
setb    SDA              ; data line is now driven by controller

```

In C language, the workaround becomes:

```

SSDAT = data;           // load transmit buffer
if (!(data & 0x80))      // test MSB
{
    SDA = 0;            // stretch data line (P1.7) to low level
}
SSCON = 0x40;           // or 0x44: clear SSI flag
SDA = 1;                // data line is now driven by controller

```

Affected Products

All TSC8x251G2D are affected.

6. Specification Changes

This section is intentionally left blank.

7. Specification Clarifications

This section is intentionally left blank.

8. Documentation Changes

This section is intentionally left blank.