- CMOS
- Mini Mold Package
- Highly Accurate : ±2%
- Built-In Delay Circuit (1ms to 50ms)
  (50ms to 200ms)
  (80ms to 400ms)
- Low Power Consumption : 1.0μA (VIN = 2.0V)

■ Applications

- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors
- Delay circuitry

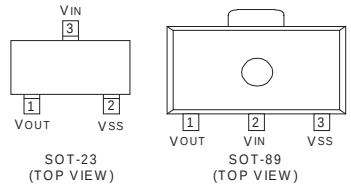
■ General Description

The XC61F series are highly accurate, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. A delay circuit is built-in to each detector.
Detect voltage is extremely accurate with minimal temperature drift. Both CMOS and N channel open drain output configurations are available.
Since the delay circuit is built-in, peripherals are unecessary and high density mounting is possible.

■ Features

Highly Accurate : Detect voltage ± 2%
Low Power Consumption : TYP 1.0μA [VIN=2.0V]
Detect Voltage Range : 1.6V to 6.0V in 0.1V increments
Operating Voltage Range : 0.7V to 10.0V
Detect Voltage Temperature Characteristics : TYP± 100ppm/°C
Built-In Delay Circuit : 1ms to 50ms, 50ms to 200ms, 80ms to 400ms
Output Configuration : N-channel open drain or CMOS
Ultra Small Packages : SOT-23 (150mW) mini-mold
SOT-89 (500mW) mini-power mold
*** No parts are available with an accuracy of ± 1%**

■ Pin Configuration

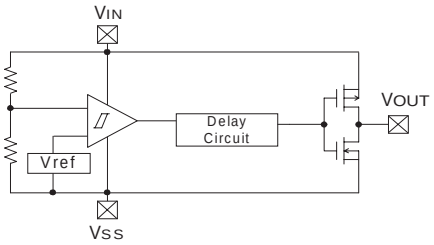


■ Pin Assignment

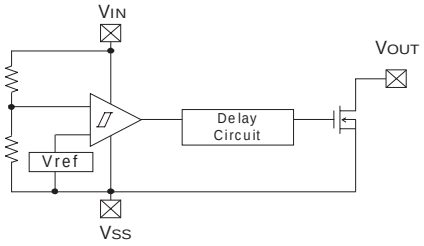
PIN NUMBER		PIN NAME	FUNCTION
SOT-23	SOT-89		
3	2	VIN	Supply Voltage Input
2	3	VSS	Ground
1	1	VOUT	Output

■ Block Diagram

(1) CMOS output



(2) N-channel open drain output



■ Absolute Maximum Ratings

Ta = 25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		VIN	12	V
Output Current		IOUT	50	mA
Output Voltage	CMOS	VOUT	VSS -0.3 ~ VIN +0.3	V
	Nch open drain		VSS -0.3 ~ 9	
Continuous Total Power Dissipation	SOT-23	Pd	150	mW
	SOT-89		500	
Operating Ambient Temperature		Topr	-30 ~ +80	°C
Storage Temperature		Tstg	-40 ~ +125	°C

■ Electrical Characteristics

Ta = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage	VDF		VDF x 0.98	VDF	VDF x 1.02	V	1
Hysteresis Range	VHYS		VDF x 0.02	VDF x 0.05	VDF x 0.08	V	1
Supply Current	ISS	VIN = 1.5V		0.9	2.6	µA	2
		=2.0V		1.0	3.0		
		=3.0V		1.3	3.4		
		=4.0V		1.6	3.8		
		=5.0V		2.0	4.2		
Operating Voltage	VIN	VDF=1.6V to 6.0V	0.7		10.0	V	1
Output Current	IOUT	Nch VDS=0.5V VIN=1.0V		2.2		mA	3
		=2.0V		7.7			
		=3.0V		10.1			
		=4.0V		11.5			
		=5.0V		13.0			
		Pch VDS=2.1V VIN=8.0V (CMOS output)		-10.0			4
Detect Voltage Temperature Characteristics	$\frac{\Delta VDF}{\Delta Topr \cdot VDF}$			±100		ppm/°C	-
Transient Delay Time (VDR→VOUT inversion)	tDLY *	VIN changes from 0.6V to 10V	50		200	ms	5

VDF (T) : established detect voltage value

Release Voltage : VDR = VDF + VHYS

* Transient Delay Time : 1ms to 50ms & 80ms to 400ms versions are also available.

Note :

The power consumption during power-start to output being stable (release operation) is 2 µA greater than it is after that period (completion of release operation) because of delay circuit through current.

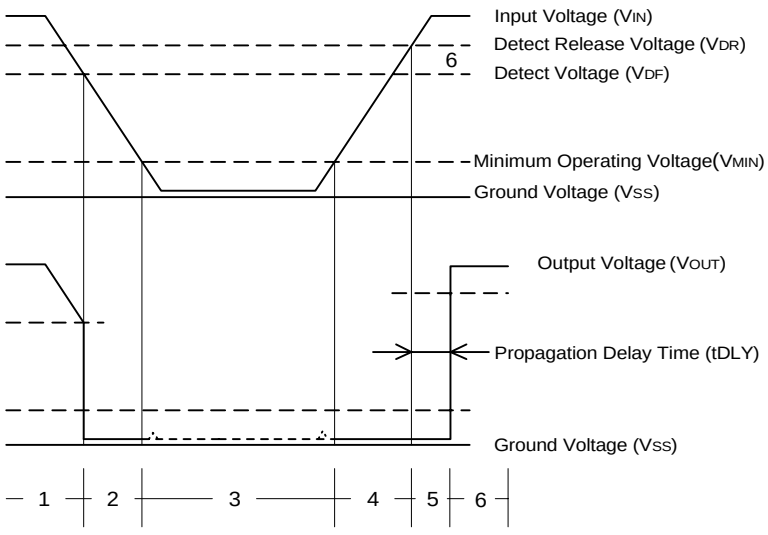
■ Functional Description (CMOS output)

1. When a voltage higher than the release voltage (V_{DR}) is applied to the voltage input pin (V_{IN}), the voltage will gradually fall. When a voltage higher than the detect voltage (V_{DF}) is applied to V_{IN}, output (V_{OUT}) will be equal to the input at V_{IN}.
   Note that high impedeance exists at V_{OUT} with the N-channel open drain configuration. If the pin is pulled up, V_{OUT} will be equal to the pull up voltage.
2. When V_{IN} falls below V_{DF}, V_{OUT} will be equal to the ground voltage (V_{SS}) level (detect state). Note that this also applies to N-channel open drain configurations.
3. When V_{IN} falls to a level below that of the minimum operating voltage (V_{MIN}) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.
4. When V_{IN} rises above the V_{SS} level (excepting levels lower than minimum operating voltage), V_{OUT} will be equal to V_{SS} until V_{IN} reaches the V_{DR} level.
5. Although V_{IN} will rise to a level higher than V_{DR}, V_{OUT} maintains ground voltage level via the delay circuit.
6. Following transient delay time, V_{IN} will be output at V_{OUT}.
   Note that high impedeance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

Notes :

1. The difference between V_{DR} and V_{DF} represents the hysteresis range.
2. Propagation delay time (tDLY) represents the time it takes for V_{IN} to appear at V_{OUT} once the said voltage has exceeded the V_{DR} level.

■ Timing Chart

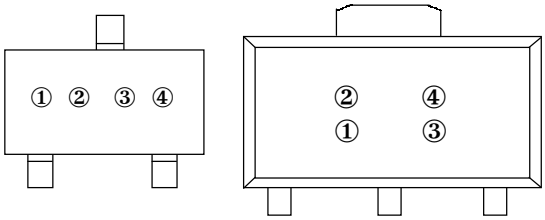


■ Ordering Information

XC61F x xx x x x x
a b c d e f

DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	Output Configuration : C = CMOS N = Nch open drain	e	Package Type : M = SOT-23 P = SOT-89
b	Detect Voltage (VDF) : 25 = 2.5V 38 = 3.8V		
c	Output Delay : 1 = 50ms to 200ms 4 = 80ms to 400ms 5 = 1ms to 50ms	f	Device Orientation : R = Embossed Tape (Right) L = Embossed Tape (Left)
d	Detect Accuracy : 2 = within ±2.0%		

■ Marking



SOT - 23 (TOP VIEW)　　SOT - 89 (TOP VIEW)

① Represents the integer of the Detect Voltage and the Output Configuration

CMOS output (XC61FC series)

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.②
B	CMOS	1.②
C	CMOS	2.②
D	CMOS	3.②
E	CMOS	4.②
F	CMOS	5.②
H	CMOS	6.②

N-channel open drain (XC61FN series)

DESIGNATOR	CONFIGURATION	VOLTAGE (V)
K	Nch	0.②
L	Nch	1.②
M	Nch	2.②
N	Nch	3.②
P	Nch	4.②
R	Nch	5.②
S	Nch	6.②

② Represents the decimal point of the Detect Voltage

DESIGNATOR	VOLTAGE (V)	DESIGNATOR	VOLTAGE (V)
0	①.0	5	①.5
1	①.1	6	①.6
2	①.2	7	①.7
3	①.3	8	①.8
4	①.4	9	①.9

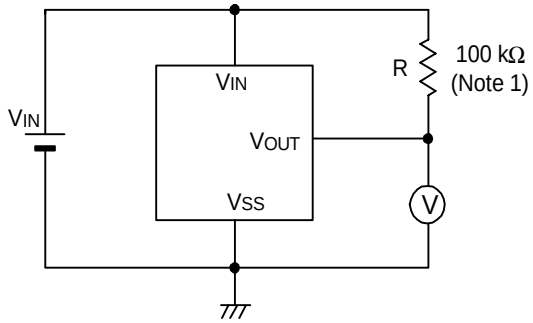
③ Indicates the presence of delay time

DESIGNATOR	DELAY TIME
5	50 to 200ms
6	80 to 400ms
7	1 to 50ms

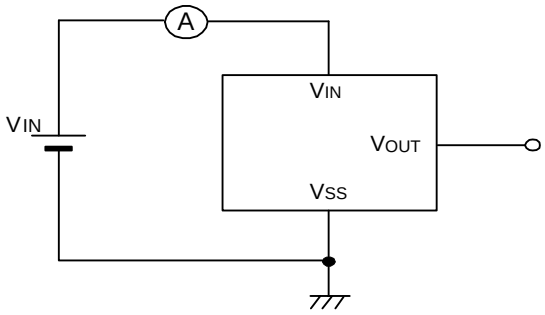
④ Represents the assembly lot no.
Based on internal standards

■ Measuring Circuits

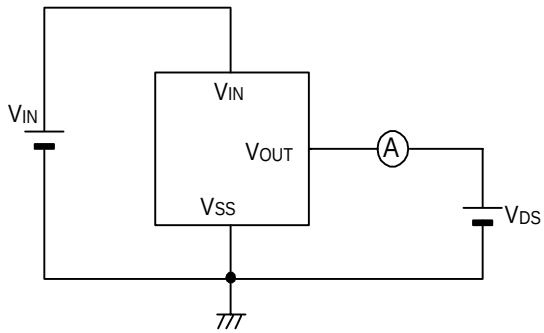
Circuit 1



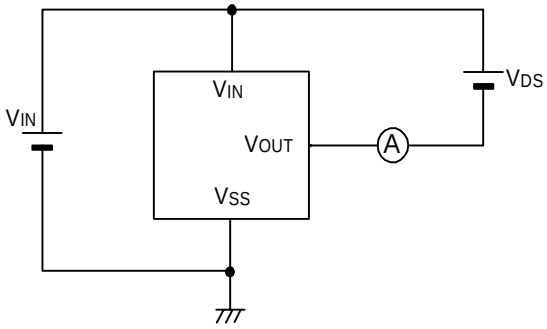
Circuit 2



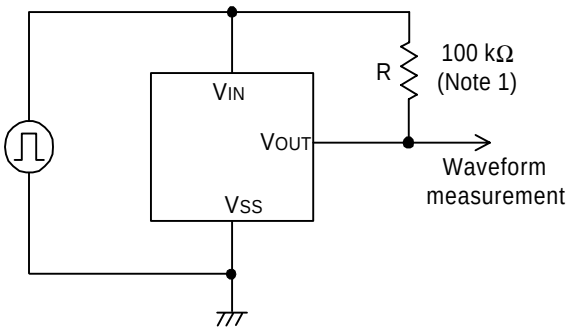
Circuit 3



Circuit 4



Circuit 5



Note 1 ： Not necessary with CMOS output products.

■ Notes on Use

1. When a resistor is connected between the VIN pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at RIN if load current (IOUT) exists. It is therefore recommend that no resistor be added. (refer to N.B. 1 - (1) below)
2. When a resistor is connected between the VIN pin and the input with CMOS output configurations, irrespective of Nch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (IOUT) does not exist. (refer to N.B. 1 - (2) below)
3. With a resistor connected between the VIN pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the VIN pin.
4. If a resistor (RIN) must be used, then please use with as small a level of input impedance as possible in order to control the occurences of oscillation as described above.
   Further, please ensure that RIN is less than 10kΩ and that CIN is more than 0.1µF (Diagram 1).
   In such cases, detect and release voltages will rise due to voltage drops at RIN brought about by the IC's supply current.

■ N.B.

1. Oscillation

(1) Oscillation as a result of output current with the CMOS output configuration :

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (IOUT) will flow through RL. Because a voltage drop (RIN x IOUT) is produced at the RIN resistor, located between the input (IN) and the VIN pin, the load current will flow via the IC's VIN pin. The voltage drop will also lead to a fall in the voltage level at the VIN pin. When the VIN pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at RIN will disappear, the voltage level at the VIN pin will rise and release operations will begin over again.
Oscillation may occur with this " release - detect - release " repetition.
Further, this condition will also appear via means of a similar mechanism during detect operations.

(2) Oscillation as a result of through current :

Since the XC61F series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur during release voltage operations as a result of output current which is influenced by this through current (Diagram 3).
Since hysteresis exists during detect operations, oscillation is unlikely to occur.

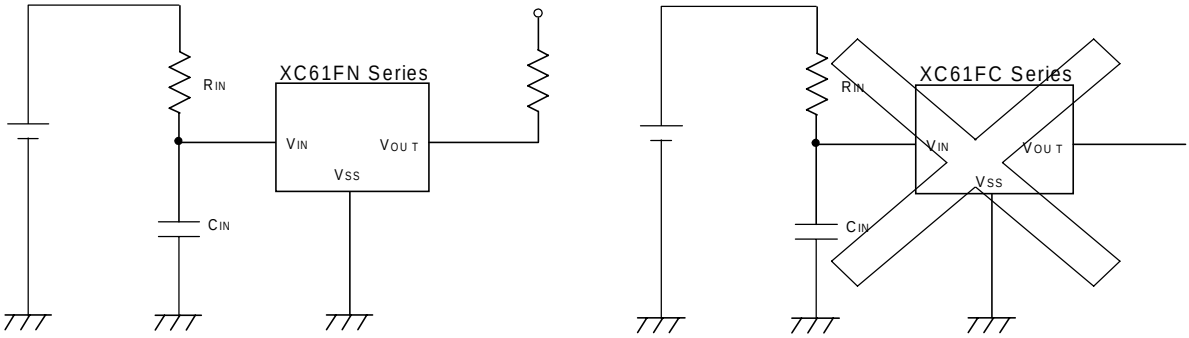


Diagram 1. When using an input resistor

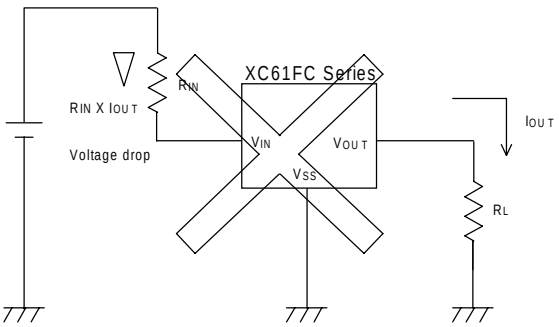


Diagram 2. Oscillation in relation to output current

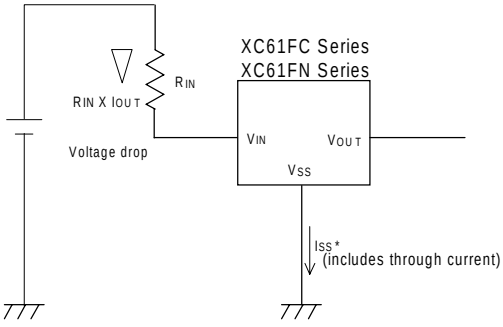
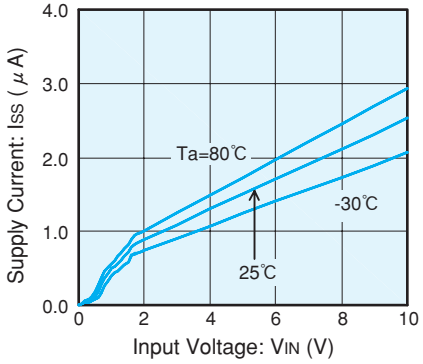


Diagram 3. Oscillation in relation to through current

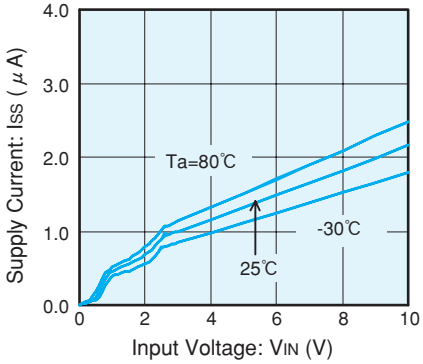
■ Electrical Characteristics

(1) Supply Current vs. Input Voltage

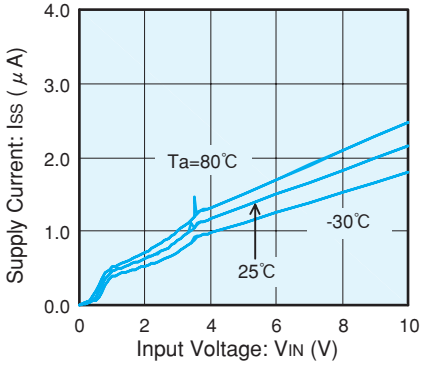
XC61FN1612



XC61FN2512

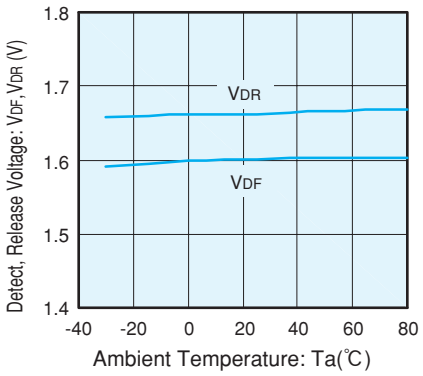


XC61FN3512

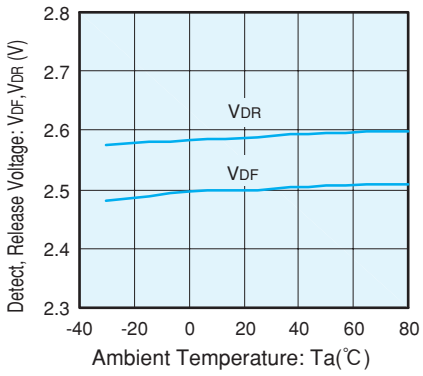


(2) Detect Voltage, Release Voltage vs. Ambient Temperature

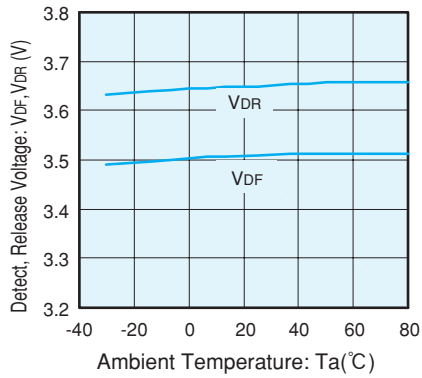
XC61FN1612



XC61FN2512

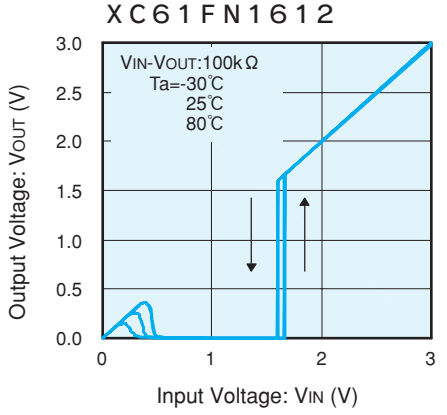


XC61FN3512

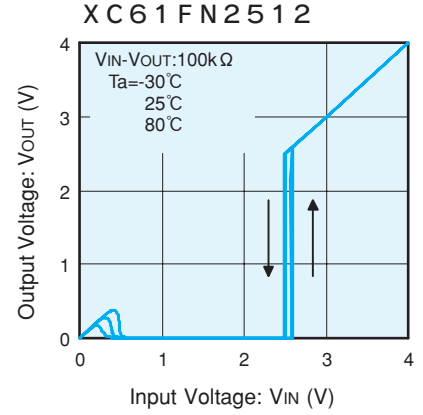


(3) Output Voltage vs. Input Voltage

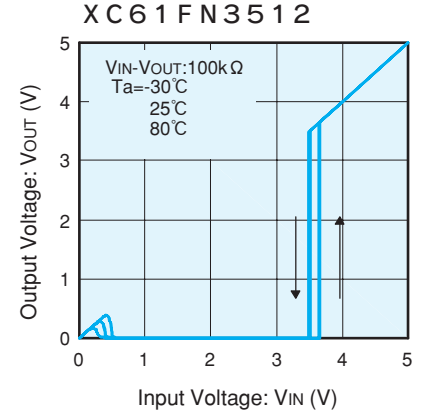
XC61FN1612



XC61FN2512

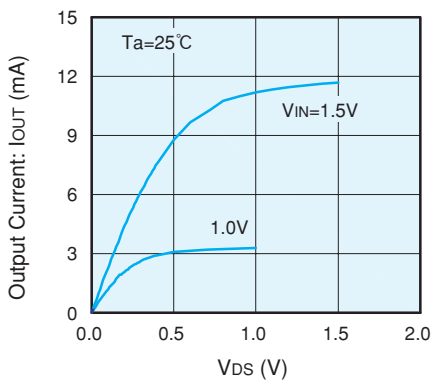


XC61FN3512

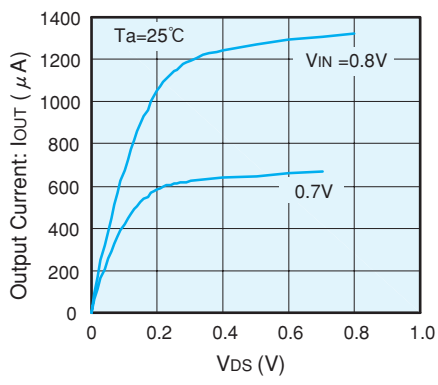


(4) N-Channel Driver Output Current vs. VDS

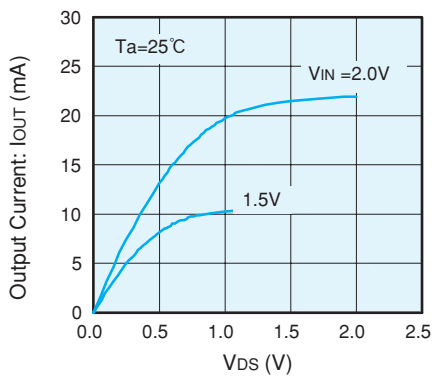
XC61FN1612



XC61FN1612

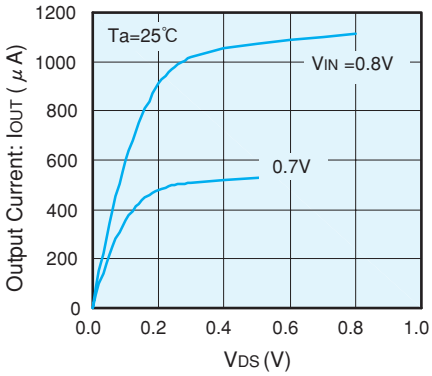


XC61FN2512

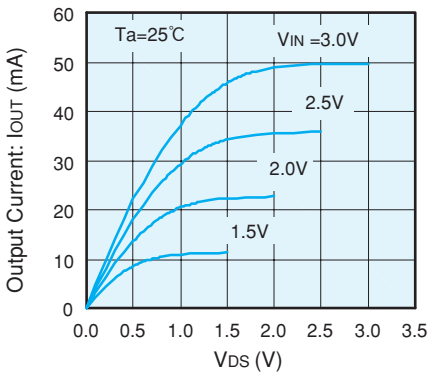


(4) N-Channel Driver Output Current vs. VDS (contd.)

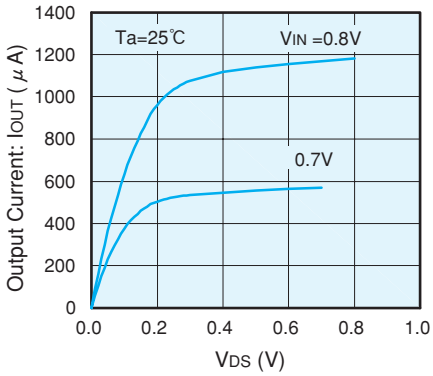
XC61FN2512



XC61FN3512

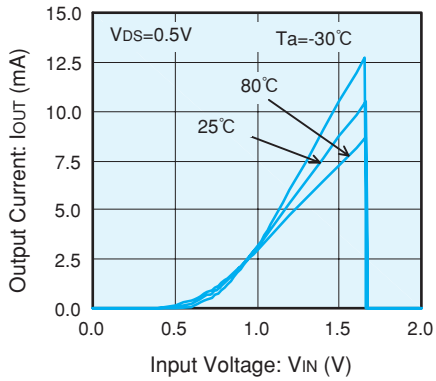


XC61FN3512

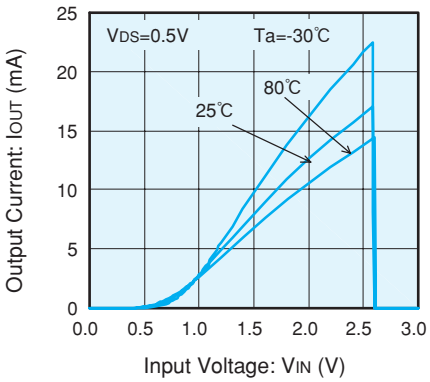


(5) N-Channel Driver Output Current vs. Input Voltage

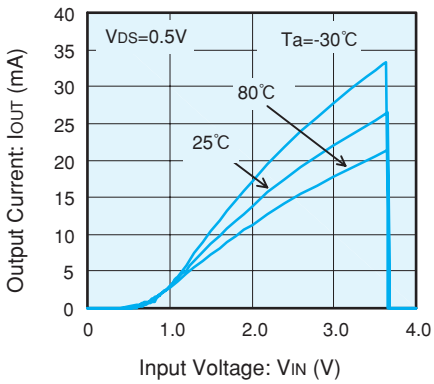
XC61FN1612



XC61FN2512

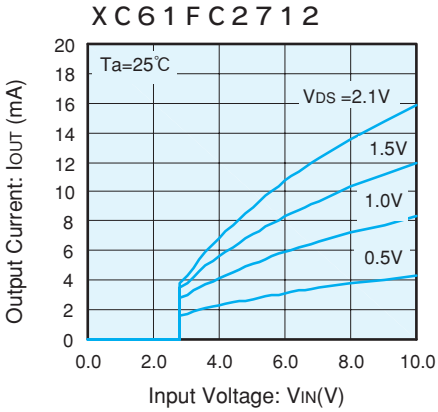


XC61FN3512

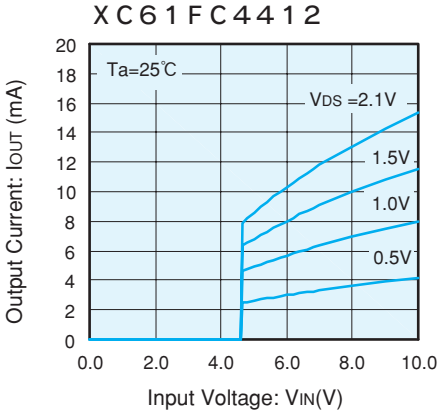


(6) P-Channel Driver Output Current vs. Input Voltage

XC61FC2712

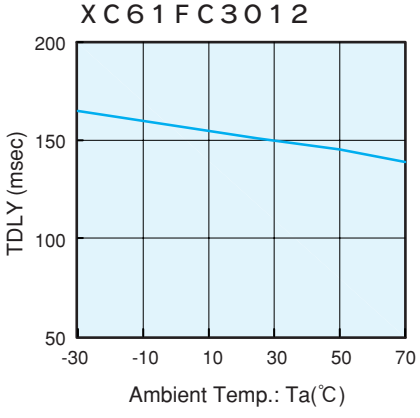


XC61FC4412

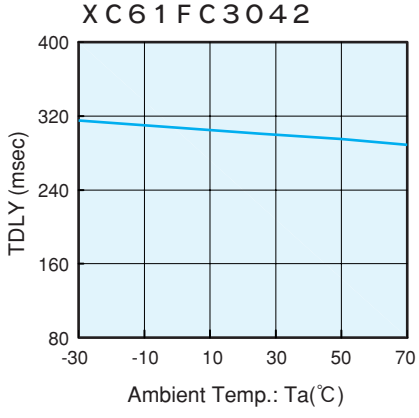


(7) Ambient Temperature vs. Transient Delay Time

XC61FC3012



XC61FC3042



XC61FC3052