DATA SHEET

TJA1054A
Fault-tolerant CAN transceiver

Product specification
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Philips
Semiconductors

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Fault-tolerant CAN transceiver TJA1054A

FEATURES

Optimized for in-car low-speed communication

- Baud rate up to 125 kBaud
- Up to 32 nodes can be connected
- Supports unshielded bus wires
- Very low ElectroMagnetic Emission (EME) due to built-in slope control function and a very good matching of the CANL and CANH bus outputs
- Good ElectroMagnetic Immunity (EMI) in normal operating mode and in low power modes
- Fully integrated receiver filters
- Transmit Data (TxD) dominant time-out function.

Bus failure management

- Supports single-wire transmission modes with ground offset voltages up to 1.5 V
- Automatic switching to single-wire mode in the event of bus failures, even when the CANH bus wire is short-circuited to V_{CC}
- Automatic reset to differential mode if bus failure is removed
- Full wake-up capability during failure modes.

Protections

- Bus pins short-circuit safe to battery and to ground
- Thermally protected
- Bus lines protected against transients in an automotive environment
- An unpowered node does not disturb the bus lines.

Support for low power modes

- Low current sleep and standby mode with wake-up via the bus lines
- Power-on reset flag on the output.

GENERAL DESCRIPTION

The TJA1054A is the interface between the protocol controller and the physical bus wires in a Controller Area Network (CAN). It is primarily intended for low-speed applications up to 125 kBaud in passenger cars. The device provides differential receive and transmit capability but will switch to single-wire transmitter and/or receiver in error conditions.

The TJA1054A is the ESD improved version of the TJA1054. For an overview of the differences between the TJA1054 and the TJA1054A, please refer to “Appendix A”.

The TJA1054AT is, as the TJA1054T, pin and downwards compatible with the PCA82C252T and the TJA1053T. This means that these two devices can be replaced by the TJA1054AT or the TJA1054T with retention of all functions.

The most important improvements of the TJA1054 and the TJA1054A with respect to the PCA82C252 and the TJA1053 are:

- Very low EME due to a very good matching of the CANL and CANH output signals
- Good EMI, especially in low power modes
- Full wake-up capability during bus failures
- Extended bus failure management including short-circuit of the CANH bus line to V_{CC}
- Support for easy system fault diagnosis
- Two-edge sensitive wake-up input signal via pin $\overline{\text{WAKE}}$.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1054AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1054AU	–	bare die; $2000 \times 2860 \times 375$ µm	–

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage on pin V_{CC}		4.75	–	5.25	V
V_{BAT}	battery voltage on pin BAT	no time limit	–0.3	–	+40	V
		operating mode	5.0	–	27	V
		load dump	–	–	40	V
I_{BAT}	battery current on pin BAT	Sleep mode; V_{CC} = 0 V; V_{BAT} = 12 V	–	30	50	µA
V_{CANH}	CANH bus line voltage	V_{CC} = 0 to 5.5 V; $V_{BAT} \geq 0$ V; no time limit	–27	–	+40	V
V_{CANL}	CANL bus line voltage	V_{CC} = 0 to 5.5 V; $V_{BAT} \geq 0$ V; no time limit	–27	–	+40	V
ΔV_{CANH}	CANH bus line transmitter voltage drop	I_{CANH} = –40 mA	–	–	1.4	V
ΔV_{CANL}	CANL bus line transmitter voltage drop	I_{CANL} = 40 mA	–	–	1.4	V
$t_{PD(L)}$	propagation delay TXD (LOW) to RXD (LOW)		–	1	–	µs
t_r	bus line output rise time	10% to 90%; C1 = 10 nF; see Fig.5	–	0.6	–	µs
t_f	bus line output fall time	90% to 10%; C1 = 1 nF; see Fig.5	–	0.3	–	µs
T_{vj}	virtual junction temperature		–40	–	+150	°C

BLOCK DIAGRAM

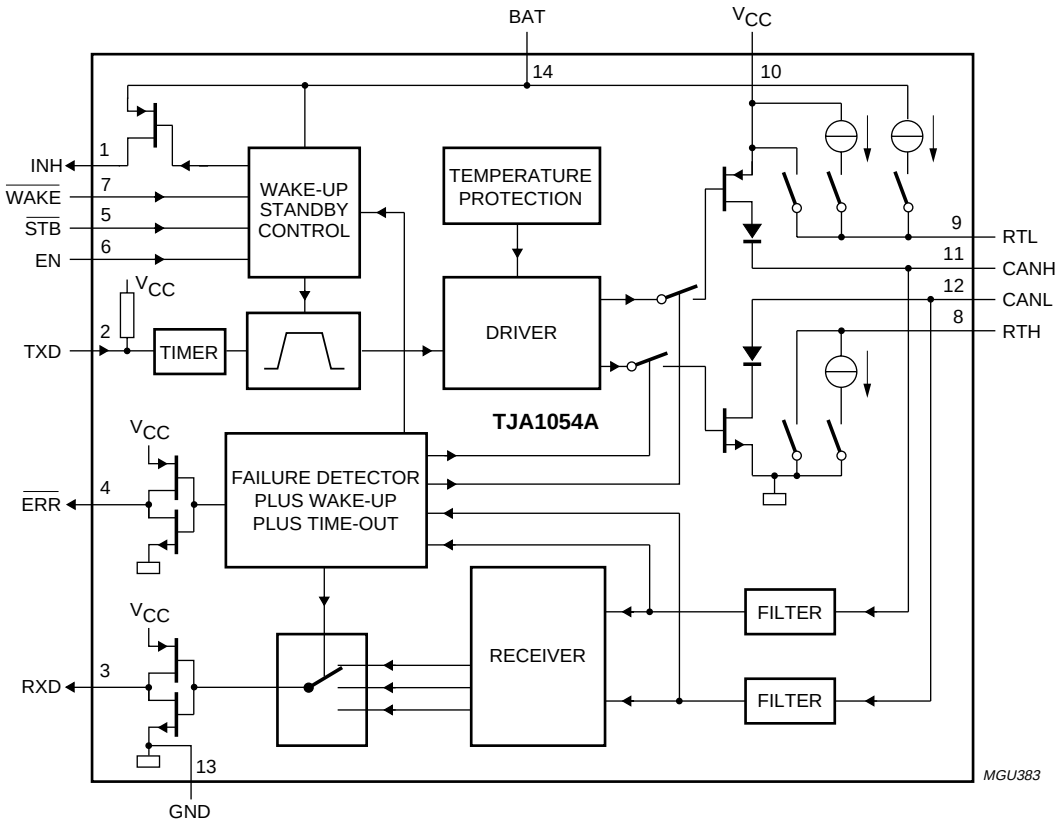


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INH	1	inhibit output for switching an external voltage regulator if a wake-up signal occurs
TXD	2	transmit data input for activating the driver to the bus lines
RXD	3	receive data output for reading out the data from the bus lines
$\overline{\text{ERR}}$	4	error, wake-up and power-on indication output; active LOW in normal operating mode when the bus has a failure, and in low power modes (wake-up signal or in power-on standby)
$\overline{\text{STB}}$	5	standby digital control signal input (active LOW); together with the input signal on pin EN this input determines the state of the transceiver (in normal and low power modes); see Table 2 and Fig.3
EN	6	enable digital control signal input; together with the input signal on pin $\overline{\text{STB}}$ this input determines the state of the transceiver (in normal and low power modes); see Table 2 and Fig.3
$\overline{\text{WAKE}}$	7	local wake-up signal input (active LOW); both falling and rising edges are detected
RTH	8	termination resistor connection; in case of a CANH bus wire error the line is terminated with a predefined impedance
RTL	9	termination resistor connection; in case of a CANL bus wire the line is terminated with a predefined impedance
V_{CC}	10	supply voltage
CANH	11	HIGH-level voltage bus line
CANL	12	LOW-level voltage bus line
GND	13	ground
BAT	14	battery supply voltage

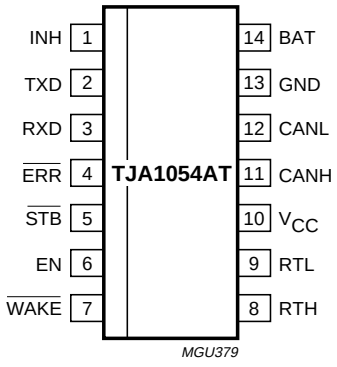


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TJA1054A is the interface between the CAN protocol controller and the physical wires of the CAN bus (see Fig.7). It is primarily intended for low speed applications, up to 125 kBaud, in passenger cars. The device provides differential transmit capability to the CAN bus and differential receive capability to the CAN controller.

To reduce EME, the rise and fall slopes are limited. This allows the use of an unshielded twisted pair or a parallel pair of wires for the bus lines. Moreover, the device supports transmission capability on either bus line if one of the wires is corrupted. The failure detection logic automatically selects a suitable transmission mode.

In normal operating mode (no wiring failures) the differential receiver is output on pin RXD (see Fig.1). The differential receiver inputs are connected to pins CANH and CANL through integrated filters. The filtered input signals are also used for the single-wire receivers. The receivers connected to pins CANH and CANL have threshold voltages that ensure a maximum noise margin in single-wire mode.

A timer function (TxD dominant time-out function) has been integrated to prevent the bus lines from being driven into a permanent dominant state (thus blocking the entire network communication) due to a situation in which pin TXD is permanently forced to a LOW level, caused by a hardware and/or software application failure.

If the duration of the LOW level on pin TXD exceeds a certain time, the transmitter will be disabled. The timer will be reset by a HIGH level on pin TXD.

Failure detector

The failure detector is fully active in the normal operating mode. After the detection of a single bus failure the detector switches to the appropriate mode (see Table 1). The differential receiver threshold voltage is set at −3.2 V typical (V_{CC} = 5 V). This ensures correct reception with a noise margin as high as possible in the normal operating mode and in the event of failures 1, 2, 5 and 6a. These failures, or recovery from them, do not destroy ongoing transmissions. The output drivers remain active, the termination does not change and the receiver remains in differential mode (see Table 1).

Failures 3, 3a and 6 are detected by comparators connected to the CANH and CANL bus lines. Failures 3 and 3a are detected in a two-step approach. If the CANH bus line exceeds a certain voltage level, the differential comparator signals a continuous dominant condition. Because of interoperability reasons with the predecessor products PCA82C252 and TJA1053, after a first time-out the transceiver switches to single wire operation through CANH. If the CANH bus line is still exceeding the CANH detection voltage for a second time-out, the TJA1054A switches to CANL operation; the CANH driver is switched off and the RTH bias changes to the pull-down current source. The time-outs (delays) are needed to avoid false triggering by external RF fields.

Table 1 Bus failures

FAILURE	DESCRIPTION	TERMINATION CANH (RTH)	TERMINATION CANL (RTL)	CANH DRIVER	CANL DRIVER	RECEIVER MODE
1	CANH wire interrupted	on	on	on	on	differential
2	CANL wire interrupted	on	on	on	on	differential
3	CANH short-circuited to battery	weak; note 1	on	off	on	CANL
3a	CANH short-circuited to V_{CC}	weak; note 1	on	off	on	CANL
4	CANL short-circuited to ground	on	weak; note 2	on	off	CANH
5	CANH short-circuited to ground	on	on	on	on	differential
6	CANL short-circuited to battery	on	weak; note 2	on	off	CANH
6a	CANL short-circuited to V_{CC}	on	on	on	on	differential
7	CANL and CANH mutually short-circuited	on	weak; note 2	on	off	CANH

Notes

1. A weak termination implies a pull-down current source behaviour of 75 μA typical.
2. A weak termination implies a pull-up current source behaviour of 75 μA typical.

Failure 6 is detected if the CANL bus line exceeds its comparator threshold for a certain period of time. This delay is needed to avoid false triggering by external RF fields. After detection of failure 6, the reception is switched to the single wire mode through CANH; the CANL driver is switched off and the RTL bias changes to the pull-up current source.

Recovery from failures 3, 3a and 6 is detected automatically after reading a consecutive recessive level by the corresponding comparators for a certain period of time.

Failures 4 and 7 initially result in a permanent dominant level on pin RXD. After a time-out the CANL driver is switched off and the RTL bias changes to the pull-up current source. Reception continues by switching to the single-wire mode via pins CANH or CANL. When failures 4 or 7 are removed, the recessive bus levels are restored. If the differential voltage remains below the recessive threshold level for a certain period of time, reception and transmission switch back to the differential mode.

If any of the wiring failure occurs, the output signal on pin $\overline{ERR}$ will be set to LOW. On error recovery, the output signal on pin $\overline{ERR}$ will be set to HIGH again. In case of an interrupted open bus wire, this failure will be detected and signalled only if there is an open wire between the transmitting and receiving node(s). Thus, during open wire failures, pin $\overline{ERR}$ typically toggles.

During all single-wire transmissions, EMC performance (both immunity and emission) is worse than in the differential mode. The integrated receiver filters suppress any HF noise induced into the bus wires. The cut-off frequency of these filters is a compromise between propagation delay and HF suppression. In single-wire mode, LF noise cannot be distinguished from the required signal.

Low power modes

The transceiver provides three low power modes which can be entered and exited via pins $\overline{STB}$ and EN (see Table 2 and Fig.3).

The Sleep mode is the mode with the lowest power consumption. Pin INH is switched to high-impedance for deactivation of the external voltage regulator. Pin CANL is biased to the battery voltage via pin RTL. If the supply voltage is provided, pins RXD and $\overline{ERR}$ will signal the wake-up interrupt.

The Standby mode operates in the same way as the Sleep mode but with a HIGH level on pin INH.

The Power-on standby mode is the same as the Standby mode, however, in this mode the battery power-on flag is shown on pin $\overline{ERR}$ instead of the wake-up interrupt signal. The output on pin RXD will show the wake-up interrupt. This mode is only for reading out the power-on flag.

Table 2 Normal operating and low power modes

MODE	$\overline{STB}$	EN	$\overline{ERR}$		RXD		RTL SWITCHED TO
			LOW	HIGH	LOW	HIGH	
goto-sleep command	0	1	wake-up interrupt signal; notes 1 and 2		wake-up interrupt signal; notes 1 and 2		V_{BAT}
sleep	0	0[3]					
standby	0	0					
power-on standby	1	0	V_{BAT} power-on flag; notes 1 and 4		wake-up interrupt signal; notes 1 and 2		V_{BAT}
normal operating	1	1	error flag	no error flag	dominant received data	recessive received data	V_{CC}

Notes

1. If the supply voltage V_{CC} is present.
2. Wake-up interrupts are released when entering normal operating mode.
3. In case the goto-sleep command was used before. When V_{CC} drops, pin EN will become LOW, but due to the fail-safe functionality this does not effect the internal functions.
4. V_{BAT} power-on flag will be reset when entering normal operating mode.

Wake-up requests are recognized by the transceiver through two possible channels:

- The bus lines for remote wake-up
- Pin $\overline{WAKE}$ for local wake-up.

In order to wake-up the transceiver remotely through the bus lines, a filter mechanism is integrated. This mechanism makes sure that noise and any present bus failure conditions do not result into an erroneous wake-up. Because of this mechanism it is not sufficient to simply pull the CANH or CANL bus lines to a dominant level for a certain time. To guarantee a successful remote wake-up under all conditions, a message frame with a dominant phase of at least the maximum specified t_{CANH} or t_{CANL} in it is required.

A local wake-up through pin $\overline{WAKE}$ is detected by a rising or falling edge with a consecutive level with the maximum specified t_{WAKE}.

On a wake-up request the transceiver will set the output on pin INH to HIGH which can be used to activate the external supply voltage regulator.

If V_{CC} is provided the wake-up request can be read on the $\overline{ERR}$ or RXD outputs, so the external microcontroller can activate the transceiver (switch to normal operating mode) via pins $\overline{STB}$ and EN.

To prevent a false remote wake-up due to transients or RF fields, the wake-up voltage levels have to be maintained for a certain period of time. In the low power modes the failure detection circuit remains partly active to prevent an increased power consumption in the event of failures 3, 3a, 4 and 7.

To prevent a false local wake-up during an open wire at pin $\overline{WAKE}$, this pin has a weak pull-up current source towards V_{BAT}. Pin INH is set to floating only if the goto-sleep command is entered successfully. To enter a successful goto-sleep command under all conditions, this command must be kept stable for the maximum specified $t_{h(sleep)}$.

Pin INH will be set to a HIGH level again by the following events only:

- V_{BAT} power-on (cold start)
- Rising or falling edge on pin $\overline{WAKE}$
- A message frame with a dominant phase of at least the maximum specified t_{CANH} or t_{CANL}, while pin EN or pin $\overline{STB}$ is at a LOW level
- pin $\overline{STB}$ goes to a HIGH level with V_{CC} active.

To provide fail-safe functionality, the signals on pins $\overline{STB}$ and EN will internally be set to LOW when V_{CC} is below a certain threshold voltage ($V_{CC(stb)}$).

Power-on

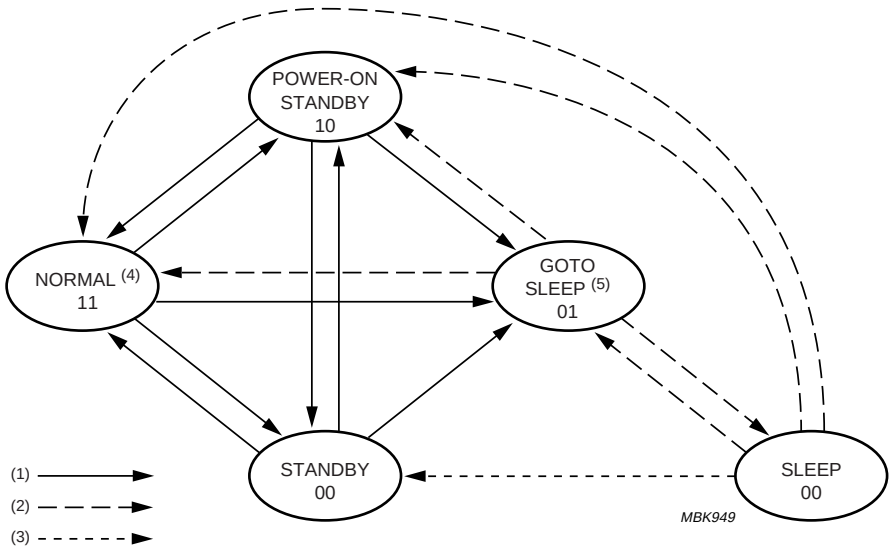
After power-on (V_{BAT} switched on) the signal on pin INH will become HIGH and an internal power-on flag will be set. This flag can be read in the power-on standby mode through pin $\overline{ERR}$ ($\overline{STB}$ = 1; EN = 0) and will be reset by entering the normal operating mode.

Protections

A current limiting circuit protects the transmitter output stages against short-circuit to positive and negative battery voltage.

If the junction temperature exceeds the typical value of 165 °C, the transmitter output stages are disabled. Because the transmitter is responsible for the major part of the power dissipation, this will result in a reduced power dissipation and hence a lower chip temperature. All other parts of the device will continue to operate.

The pins CANH and CANL are protected against electrical transients which may occur in an automotive environment.



Mode 10 stands for: Pin $\overline{STB}$ = HIGH and pin EN = LOW.

(1) Mode change via input pins $\overline{STB}$ and EN.

(2) Mode change via input pins $\overline{STB}$ and EN; it should be noted that in the sleep mode pin INH is inactive and possibly there is no V_{CC}. Mode control is only possible if V_{CC} of the transceiver is active.

(3) Pin INH is activated after wake-up via bus or input pin $\overline{WAKE}$.

(4) Transitions to normal mode clear the internal wake-up: interrupt and battery fail flag are cleared.

(5) Transitions to sleep mode: pin INH is deactivated.

Fig.3 Mode control.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage on pin V_{CC}		–0.3	+6	V
V_{BAT}	battery voltage on pin BAT		–0.3	+40	V
V_n	DC voltage on pins TXD, RXD, $\overline{ERR}$, $\overline{STB}$ and EN		–0.3	V_{CC} + 0.3	V
V_{CANH}	DC voltage on pin CANH		–27	+40	V
V_{CANL}	DC voltage on pin CANL		–27	+40	V
$V_{trt(n)}$	transient voltage on pins CANH and CANL	see Fig.6	–150	+100	V
V_{WAKE}	DC input voltage on pin $\overline{WAKE}$		–	V_{BAT} + 0.3	V
I_{WAKE}	DC input current on pin $\overline{WAKE}$	note 2	–15	–	mA
V_{INH}	DC output voltage on pin INH		–0.3	V_{BAT} + 0.3	V
V_{RTH}	DC voltage on pin RTH		–0.3	V_{BAT} + 1.2	V
V_{RTL}	DC voltage on pin RTL		–0.3	V_{BAT} + 1.2	V
R_{RTH}	termination resistance on pin RTH		500	16000	Ω
R_{RTL}	termination resistance on pin RTL		500	16000	Ω
T_{vj}	virtual junction temperature	note 3	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic discharge voltage	human body model; note 4			
		pins RTH, RTL, CANH and CANL	–4	+4	kV
		all other pins	–2	+2	kV
		machine model; note 5			
		any pin	–300	+300	V

Notes

1. All voltages are defined with respect to pin GND. Positive current flows into the device.
2. Only relevant if $V_{WAKE} < V_{GND} - 0.3$ V; current will flow into pin GND.
3. Junction temperature in accordance with *"IEC 60747-1"*. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$ where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and operating ambient temperature (T_{amb}).
4. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
5. Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH coil.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(vj-a)}$	thermal resistance from junction to ambient	in free air	120	K/W
$R_{th(vj-s)}$	thermal resistance from junction to substrate bare die	in free air	40	K/W

QUALITY SPECIFICATION

Quality specification in accordance with *"AEC-Q100"*.

DC CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; V_{BAT} = 5 to 27 V; V_{STB} = V_{CC}; T_{vj} = –40 to +150 °C; all voltages are defined with respect to ground; positive currents flow into the device; unless otherwise specified; notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CC}	supply voltage on pin V_{CC}		4.75	–	5.25	V
$V_{CC(stb)}$	supply voltage for forced standby mode (fail safe)		2.75	–	4.5	V
I_{CC}	supply current	normal operating mode; V_{TXD} = V_{CC} (recessive)	4	7	11	mA
		normal operating mode; V_{TXD} = 0 V (dominant); no load	10	17	27	mA
		low power modes; V_{TXD} = V_{CC}	0	0	10	µA
V_{BAT}	battery voltage on pin BAT	no time limit	–0.3	–	+40	V
		operating mode	5.0	–	27	V
		load dump	–	–	40	V
I_{BAT}	battery current on pin BAT	all modes and in low power modes at V_{RTL} = V_{BAT}				
		V_{BAT} = V_{WAKE} = V_{INH} = 12 V	10	30	50	µA
		V_{BAT} = V_{WAKE} = V_{INH} = 5 to 27 V	5	30	125	µA
		V_{BAT} = V_{WAKE} = V_{INH} = 3.5 V	5	20	30	µA
		V_{BAT} = V_{WAKE} = V_{INH} = 1 V	0	0	10	µA
$V_{BAT(Pwon)}$	power-on flag voltage on pin BAT	low power modes				
		power-on flag set	–	–	1	V
		power-on flag not set	3.5	–	–	V
I_{tot}	supply current plus battery current	low power modes; V_{CC} = 5 V; V_{BAT} = V_{WAKE} = V_{INH} = 12 V	–	30	60	µA
Pins $\overline{\text{STB}}$, EN and TXD						
V_{IH}	HIGH-level input voltage		0.7V_{CC}	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	0.3V_{CC}	V
I_{IH}	HIGH-level input current	V_I = 4 V				
	pins $\overline{\text{STB}}$ and EN		–	9	20	µA
	pin TXD		–200	–80	–25	µA
I_{IL}	LOW-level input current	V_I = 1 V				
	pins $\overline{\text{STB}}$ and EN		4	8	–	µA
	pin TXD		–800	–320	–100	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RXD and $\overline{ERR}$						
V_{OH}	HIGH-level output voltage					
	on pin $\overline{ERR}$	I_O = –100 µA	V_{CC} – 0.9	–	V_{CC}	V
	on pin RXD	I_O = –1 mA	V_{CC} – 0.9	–	V_{CC}	V
V_{OL}	LOW-level output voltage on pins $\overline{ERR}$ and RXD	I_O = 1.6 mA	0	–	0.4	V
		I_O = 7.5 mA	0	–	1.5	V
Pin $\overline{WAKE}$						
I_{IL}	LOW-level input current	V_{WAKE} = 0 V; V_{BAT} = 27 V	–10	–4	–1	µA
$V_{th(wake)}$	wake-up threshold voltage	V_{STB} = 0 V	2.5	3.2	3.9	V
Pin INH						
ΔV_H	HIGH-level voltage drop	I_{INH} = –0.18 mA	–	–	0.8	V
$\lvert I_L \rvert$	leakage current	Sleep mode; V_{INH} = 0 V	–	–	5	µA
Pins CANH and CANL						
$V_{th(dif)}$	differential receiver threshold voltage	no failures and bus failures 1, 2, 5 and 6a; see Fig.4				
		V_{CC} = 5 V	–3.5	–3.2	–2.9	V
		V_{CC} = 4.75 to 5.25 V	$-0.70V_{CC}$	$-0.64V_{CC}$	$-0.58V_{CC}$	V
$V_{O(reces)}$	recessive output voltage	V_{TXD} = V_{CC}				
	on pin CANH	R_{RTH} < 4 kΩ	–	–	0.2	V
	on pin CANL	R_{RTL} < 4 kΩ	V_{CC} – 0.2	–	–	V
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; V_{EN} = V_{CC}				
	on pin CANH	I_{CANH} = –40 mA	V_{CC} – 1.4	–	–	V
	on pin CANL	I_{CANL} = 40 mA	–	–	1.4	V
$I_{O(CANH)}$	output current on pin CANH	normal operating mode; V_{CANH} = 0 V; V_{TXD} = 0 V	–110	–80	–45	mA
		low power modes; V_{CANH} = 0 V; V_{CC} = 5 V	–	–0.25	–	µA
$I_{O(CANL)}$	output current on pin CANL	normal operating mode; V_{CANL} = 14 V; V_{TXD} = 0 V	45	70	100	mA
		low power modes; V_{CANL} = 12 V; V_{BAT} = 12 V	–	0	–	µA
$V_{d(CANH)(sc)}$	detection voltage for short-circuit to battery voltage on pin CANH	normal operating mode	1.5	1.7	1.85	V
		low power modes	1.1	1.8	2.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{d(CANL)(sc)}$	detection voltage for short-circuit to battery voltage on pin CANL	normal operating mode				
		V_{CC} = 5 V	6.6	7.2	7.8	V
		V_{CC} = 4.75 to 5.25 V	$1.32V_{CC}$	$1.44V_{CC}$	$1.56V_{CC}$	V
$V_{th(wake)}$	wake-up threshold voltage					
	on pin CANL	low power modes	2.5	3.2	3.9	V
	on pin CANH	low power modes	1.1	1.8	2.5	V
$\Delta V_{th(wake)}$	difference of wake-up threshold voltages	low power modes	0.8	1.4	–	V
$V_{th(CANH)(se)}$	single-ended receiver threshold voltage on pin CANH	normal operating mode and failures 4, 6 and 7				
		V_{CC} = 5 V	1.5	1.7	1.85	V
		V_{CC} = 4.75 to 5.25 V	$0.30V_{CC}$	$0.34V_{CC}$	$0.37V_{CC}$	V
$V_{th(CANL)(se)}$	single-ended receiver threshold voltage on pin CANL	normal operating mode and failures 3 and 3a				
		V_{CC} = 5 V	3.15	3.3	3.45	V
		V_{CC} = 4.75 to 5.25 V	$0.63V_{CC}$	$0.66V_{CC}$	$0.69V_{CC}$	V
$R_{i(CANH)(se)}$	single-ended input resistance on pin CANH	normal operating mode	110	165	270	kΩ
$R_{i(CANL)(se)}$	single-ended input resistance on pin CANL	normal operating mode	110	165	270	kΩ
$R_{i(dif)}$	differential input resistance	normal operating mode	220	330	540	kΩ
Pins RTH and RTL						
$R_{sw(RTL)}$	switch-on resistance between pin RTL and V_{CC}	normal operating mode; $\lvert I_O \rvert$ < 10 mA	–	50	100	Ω
$R_{sw(RTH)}$	switch-on resistance between pin RTH and ground	normal operating mode; $\lvert I_O \rvert$ < 10 mA	–	50	100	Ω
$V_{O(RTH)}$	output voltage on pin RTH	low power modes; I_O = 1 mA	–	0.7	1.0	V
$I_{O(RTL)}$	output current on pin RTL	low power modes; V_{RTL} = 0 V	–1.25	–0.65	–0.3	mA
$I_{pu(RTL)}$	pull-up current on pin RTL	normal operating mode and failures 4, 6 and 7	–	75	–	µA
$I_{pd(RTH)}$	pull-down current on pin RTH	normal operating mode and failures 3 and 3a	–	75	–	µA
Thermal shutdown						
$T_{j(sd)}$	junction temperature for shutdown		155	165	180	°C

Notes

1. All parameters are guaranteed over the virtual junction temperature range by design, but only 100% tested at T_{amb} = 125 °C for dies on wafer level, and above this for cased products 100% tested at T_{amb} = 25 °C, unless otherwise specified.
2. For bare die, all parameters are only guaranteed if the back side of the die is connected to ground.

TIMING CHARACTERISTICS

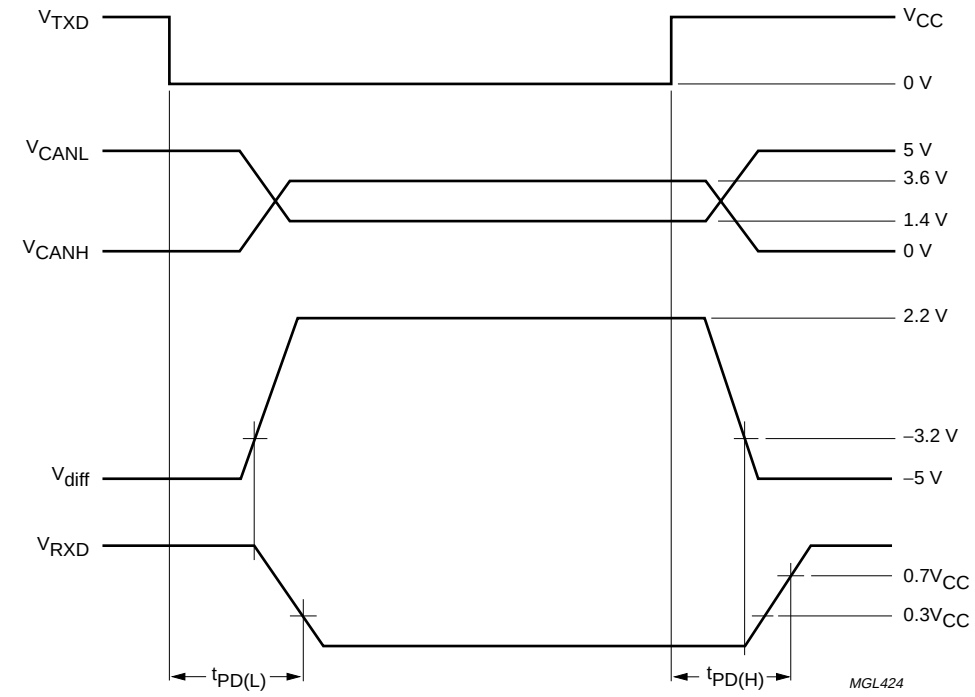
V_{CC} = 4.75 to 5.25 V; V_{BAT} = 5 to 27 V; V_{STB} = V_{CC}; T_{vj} = −40 to +150 °C; all voltages are defined with respect to ground; unless otherwise specified; notes 1 and 2

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{t(r-d)}$	CANL and CANH output transition time for recessive to dominant	10% to 90%; C1 = 10 nF; C2 = not present; R1 = 100 Ω; see Fig.5	0.35	0.60	–	µs
$t_{t(d-r)}$	CANL and CANH output transition time for dominant to recessive	10% to 90%; C1 = 1 nF; C2 = not present; R1 = 100 Ω; see Fig.5	0.2	0.3	–	µs
$t_{PD(L)}$	propagation delay TXD (LOW) to RXD (LOW)	no failures and failures 1, 2, 5 and 6a; see Figs 4 and 5				
		C1 = 1 nF; C2 = not present; R1 = 100 Ω	–	0.75	1.5	µs
		C1 = C2 = 3.3 nF; R1 = 100 Ω	–	1	1.75	µs
		failures 3, 3a, 4, 6 and 7; see Figs 4 and 5				
		C1 = 1 nF; C2 = not present; R1 = 100 Ω	–	0.85	1.4	µs
		C1 = C2 = 3.3 nF; R1 = 100 Ω	–	1.1	1.7	µs
$t_{PD(H)}$	propagation delay TXD (HIGH) to RXD (HIGH)	no failures and failures 1, 2, 5 and 6a; see Figs 4 and 5				
		C1 = 1 nF; C2 = not present; R1 = 100 Ω	–	1.2	1.9	µs
		C1 = C2 = 3.3 nF; R1 = 100 Ω	–	2.5	3.3	µs
		failures 3, 3a, 4, 6 and 7; see Figs 4 and 5				
		C1 = 1 nF; C2 = not present; R1 = 100 Ω	–	1.1	1.7	µs
		C1 = C2 = 3.3 nF; R1 = 100 Ω	–	1.5	2.2	µs
$t_{react(sleep)}$	reaction time of goto-sleep command	note 3	5	–	50	µs
$t_{dis(TxD)}$	disable time of TxD permanent dominant timer	normal operating mode; V_{TXD} = 0 V	0.75	–	4	ms
t_{CANH}	dominant time for remote wake-up on pin CANH	low power modes; V_{BAT} = 12 V; note 3	7	–	38	µs
t_{CANL}	dominant time for remote wake-up on pin CANL	low power modes; V_{BAT} = 12 V; note 3	7	–	38	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{WAKE}	required time on pin $\overline{WAKE}$ for local wake-up	low power modes; V_{BAT} = 12 V; for wake-up after receiving a falling or rising edge; note 3	7	–	38	µs
t_{det}	failure detection time	normal operating mode				
		failures 3 and 3a	1.6	–	8.0	ms
		failures 4, 6 and 7	0.3	–	1.6	ms
		low power modes; V_{BAT} = 12 V				
		failures 3 and 3a	1.6	–	8.0	ms
		failures 4 and 7	0.1	–	1.6	ms
t_{rec}	failure recovery time	normal operating mode				
		failures 3 and 3a	0.3	–	1.6	ms
		failures 4 and 7	7	–	38	µs
		failure 6	125	–	750	µs
		low power modes; V_{BAT} = 12 V				
		failures 3, 3a, 4 and 7	0.3	–	1.6	ms
N_{det}	pulse-count difference between CANH and CANL for failure detection	normal operating mode and failures 1, 2, 5 and 6a; pin ERR becomes LOW	–	4	–	
N_{rec}	number of consecutive pulses on CANH and CANL simultaneously for failure recovery	failures 1, 2, 5 and 6a	–	4	–	

Notes

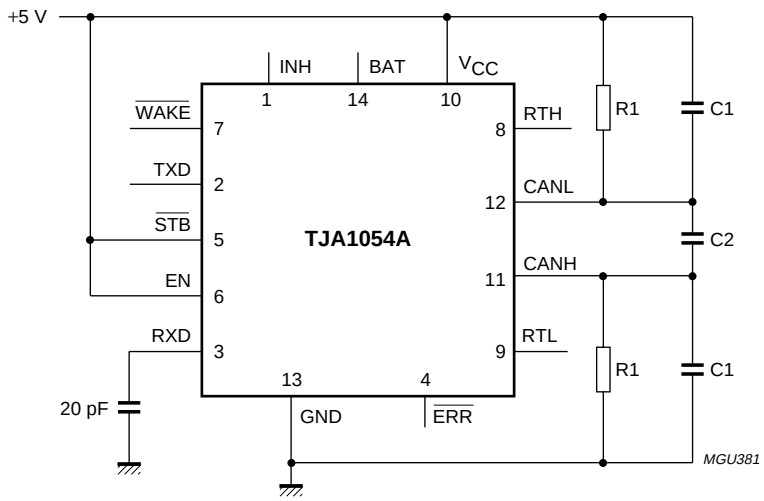
1. All parameters are guaranteed over the virtual junction temperature range by design, but only 100% tested at T_{amb} = 125 °C for dies on wafer level, and above this for cased products 100% tested at T_{amb} = 25 °C, unless otherwise specified.
2. For bare die, all parameters are only guaranteed if the back side of the die is connected to ground.
3. To guarantee a successful mode transition under all conditions, the maximum specified time must be applied.



$V_{diff} = V_{CANH} - V_{CANL}$.

Fig.4 Timing diagram for dynamic characteristics.

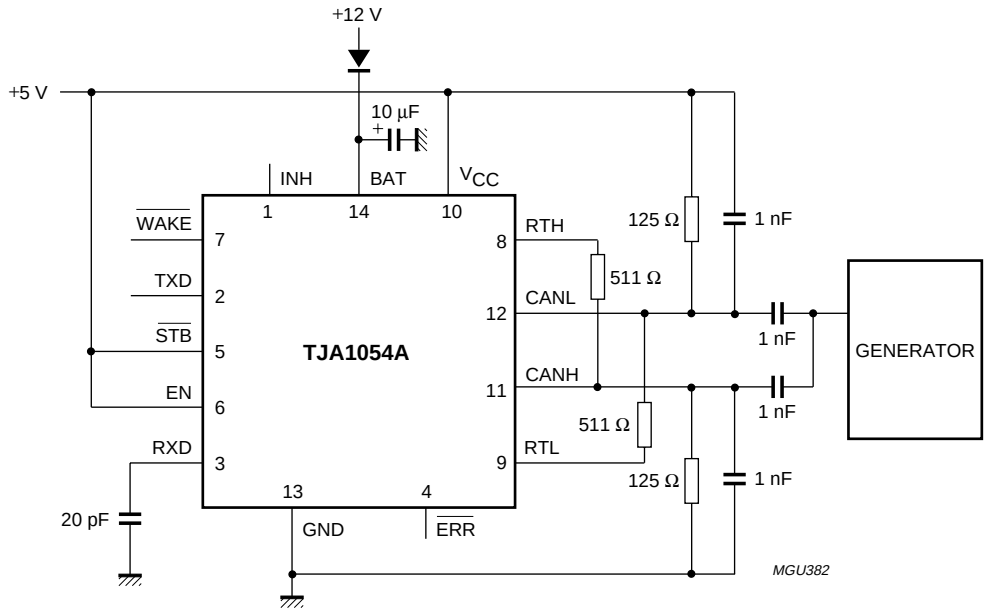
TEST AND APPLICATION INFORMATION



(1) Termination resistors R1 (100 Ω) are not connected to pin RTH or pin RTL for testing purposes because the minimum load allowed on the CAN bus lines is 500 Ω per transceiver.

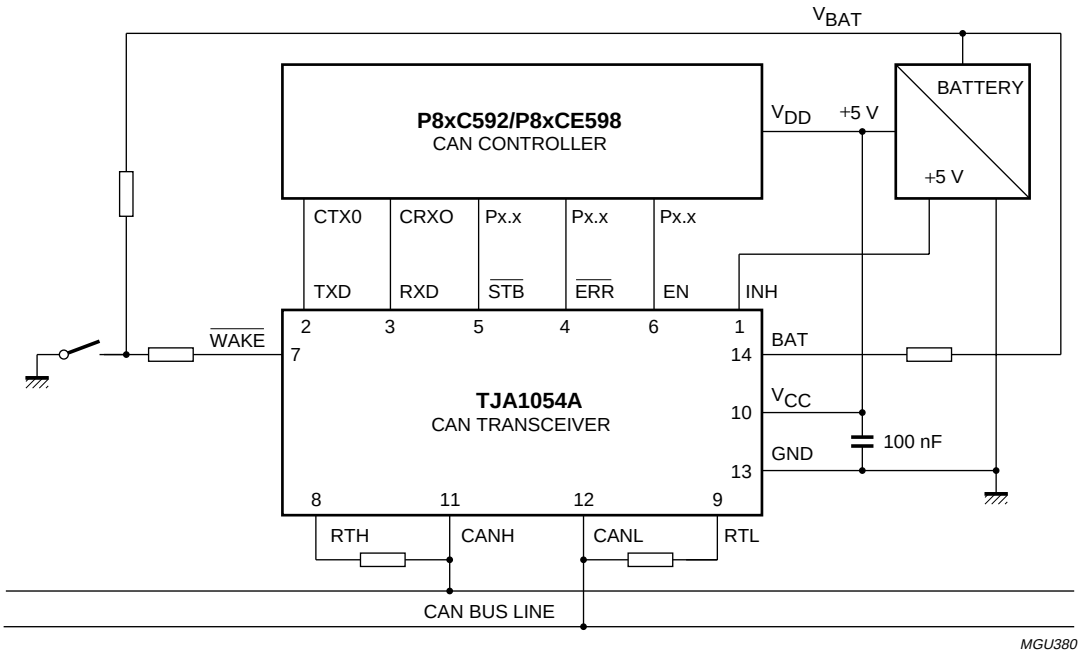
(2) The capacitive bus load of 10 nF is split into 3 equal capacitors (3.3 nF) to simulate the bus cable.

Fig.5 Test circuit for dynamic characteristics.



The waveforms of the applied transients on pins CANH and CANL will be in accordance with *"ISO 7637 part 1"*: test pulses 1, 2, 3a and 3b.

Fig.6 Test circuit for automotive transients.



For more information: please refer to the separate FTCAN information available from our website.

Fig.7 Application diagram.

BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES[1]	
		x	y
INH	1	206	357
TXD	2	211	208
RXD	3	850	151
$\overline{ERR}$	4	1447	151
$\overline{STB}$	5	2348	143
EN	6	2651	280
$\overline{WAKE}$	7	2659	421
RTH	8	2563	1483
RTL	9	2489	1880
V_{CC}	10	1986	1849
CANH	11	1000	1738
CANL	12	501	1738
GND	13a	180	1396
GND	13b	180	1281
BAT	14	205	812

Note

1. All coordinates (μm) represent the position of the centre of each pad with respect to the bottom left-hand corner of the die (see Fig.8).

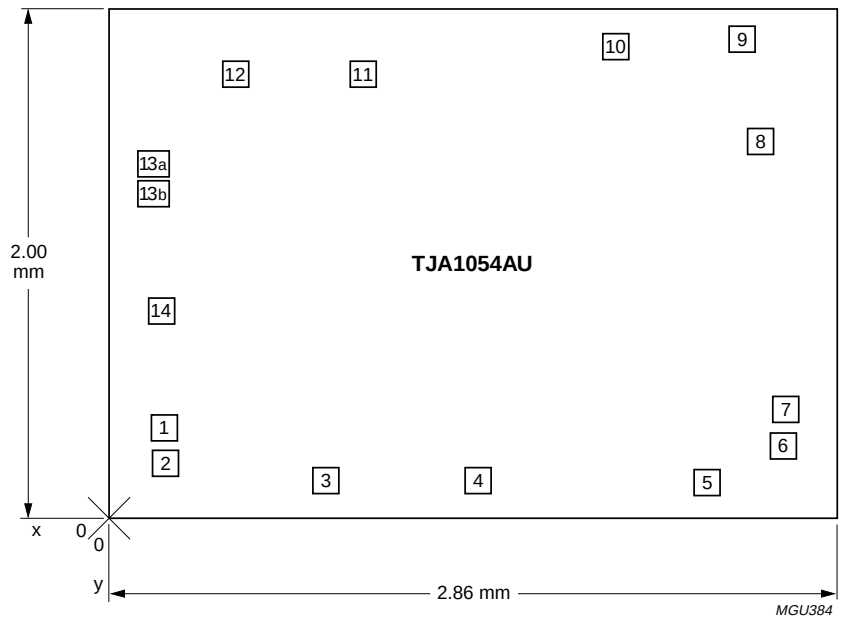


Fig.8 Bonding pad locations.

APPENDIX A

Overview of differences between the TJA1054 and the TJA1054A

Limiting values

SYMBOL	PARAMETER	CONDITIONS	TJA1054		TJA1054A		UNIT
			MIN.	MAX.	MIN.	MAX.	
V_{CANH}	CANH bus line voltage		–40	+40	–27	+40	V
V_{CANL}	CANL bus line voltage		–40	+40	–27	+40	V
V_{esd}	electrostatic discharge voltage	human body model					
		pins RTH, RTL, CANH, and CANL	–2	+2	–4	+4	kV
		all other pins	–2	+2	–2	+2	kV
		machine model					
		any pin	–175	+175	–300	+300	V

Bare die

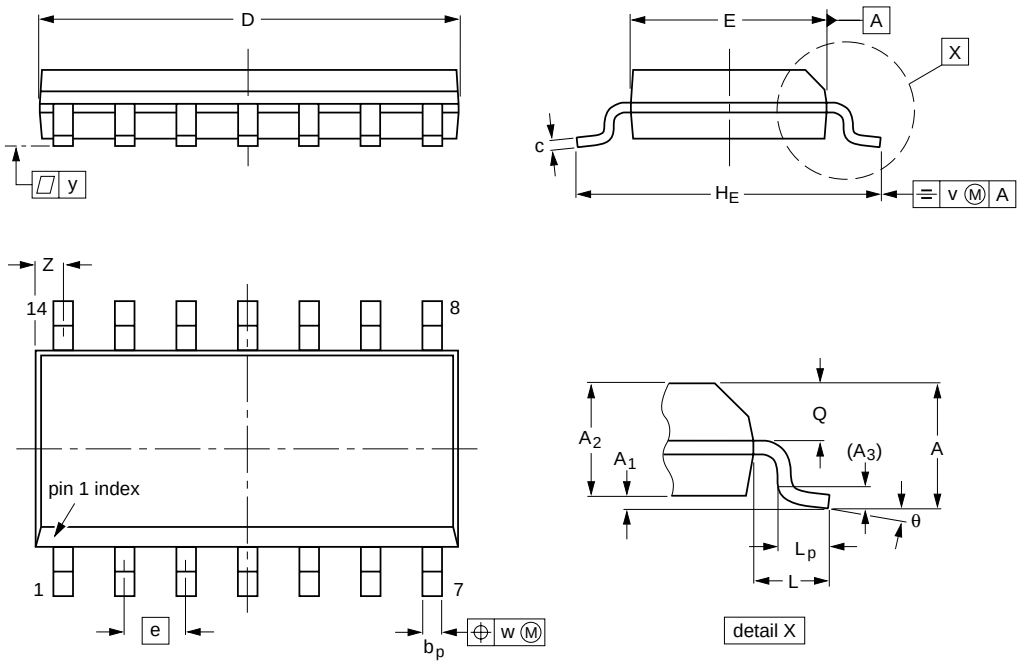
PARAMETER	TJA1054	TJA1054A	UNIT
Dimensions	2000×2830	2000×2860	μm
Bonding pad coordinates	note 1	note 1	

Note

1. The bonding pad coordinates partly differ between the TJA1054 and the TJA1054A.

PACKAGE OUTLINE

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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