INTEGRATED CIRCUITS

DATA SHEET

TJA1050
High speed CAN transceiver

Preliminary specification
Supersedes data of 1999 Sep 27
File under Integrated Circuits, IC18

2000 May 26

Philips
Semiconductors

PHILIPS

FEATURES

- Fully compatible with the *"ISO 11898"* standard
- High speed (up to 1 Mbaud)
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with wide common-mode range for high ElectroMagnetic Immunity (EMI)
- An unpowered node does not disturb the bus lines
- Transmit Data (TXD) dominant time-out function
- Silent mode in which the transmitter is disabled
- Bus pins protected against transients in an automotive environment
- Input levels compatible with 3.3 V devices
- Thermally protected
- Short-circuit proof to supply voltage and ground
- At least 110 nodes can be connected.

GENERAL DESCRIPTION

The TJA1050 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The TJA1050 is the successor to the PCA82C250 high-speed CAN transceiver. The most important improvements are:

- Much lower electromagnetic emission due to optimal matching of the output signals CANH and CANL
- Improved behaviour in case of an unpowered node.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.25	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
$V_{i(dif)(bus)}$	differential bus input voltage	dominant	1.5	3	V
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	$V_S = 0$ V; see Fig.7	–	250	ns
T_{amb}	ambient temperature		–40	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1050T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1050U	–	bare die; die dimensions 1700 x 1280 x 380 µm	–

BLOCK DIAGRAM

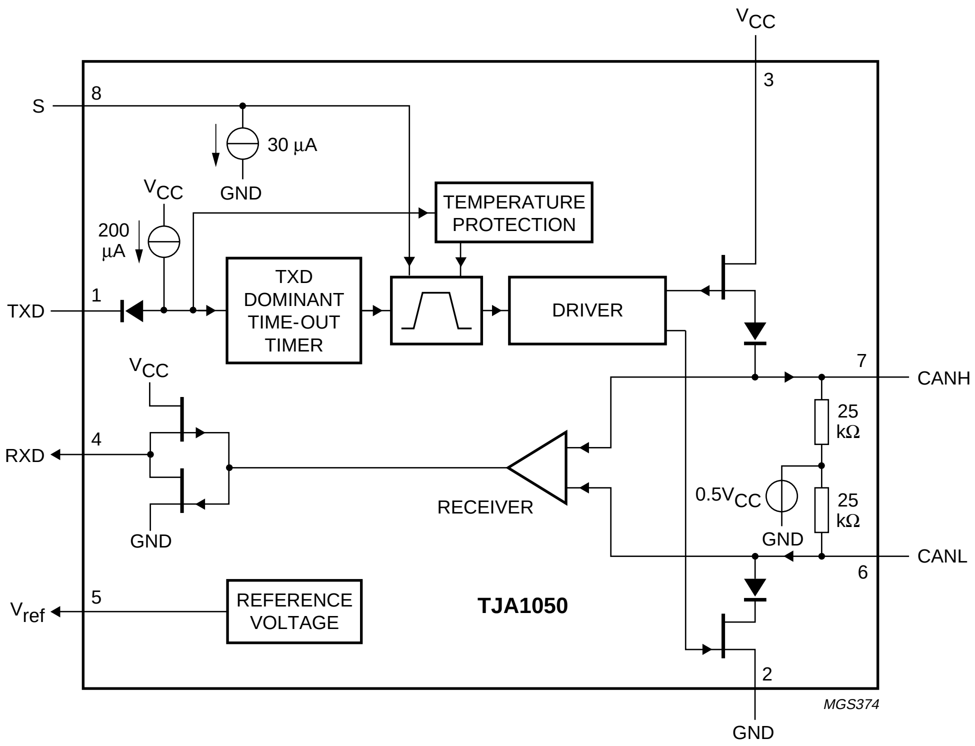


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXD	1	transmit data input; reads in data from the CAN controller to the bus line drivers
GND	2	ground
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines to the CAN controller
V_{ref}	5	reference voltage output
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
S	8	select input for high-speed mode or silent mode

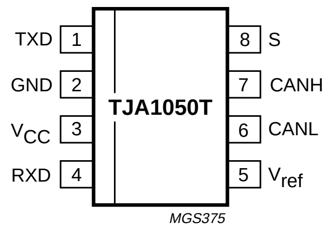


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TJA1050 is the interface between the CAN protocol controller and the physical bus. It is primarily intended for high-speed automotive applications using baud rates from 60 kbaud up to 1 Mbaud. It provides differential transmit capability to the bus and differential receiver capability to the CAN protocol controller. It is fully compatible to the *“ISO 11898”* standard.

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 165 °C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when pin TXD goes HIGH. The thermal protection circuit is particularly needed when a bus line short-circuits.

The pins CANH and CANL are protected from automotive electrical transients (according to *“ISO 7637”*; see Fig.4).

Control pin S allows two operating modes to be selected: high-speed mode or silent mode.

The high-speed mode is the normal operating mode and is selected by connecting pin S to ground. It is the default mode if pin S is not connected.

In the silent mode, the transmitter is disabled. All other IC functions continue to operate. The silent mode is selected by connecting pin S to V_{CC} and can be used to prevent network communication from being blocked, due to a CAN controller which is out of control.

A ‘TXD dominant time-out’ timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD. If the duration of the LOW-level on pin TXD exceeds the internal timer value, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TXD.

Table 1 Function table of the CAN transceiver; X = don’t care

V_{CC}	TXD	S	CANH	CANL	BUS STATE	RXD
4.75 to 5.25 V	0	0 (or floating)	HIGH	LOW	dominant	0
4.75 to 5.25 V	X	1	$0.5V_{CC}$	$0.5V_{CC}$	recessive	1
4.75 to 5.25 V	1 (or floating)	X	$0.5V_{CC}$	$0.5V_{CC}$	recessive	1
<2 V (not powered)	X	X	$0\ V < V_{CANH} < V_{CC}$	$0\ V < V_{CANL} < V_{CC}$	recessive	X
$2\ V < V_{CC} < 4.75\ V$	>2 V	X	$0\ V < V_{CANH} < V_{CC}$	$0\ V < V_{CANL} < V_{CC}$	recessive	X

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND (pin 2). Positive currents flow into the IC.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.3	+6	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{TXD}	DC voltage at pin TXD		–0.3	V_{CC} + 0.3	V
V_{RXD}	DC voltage at pin RXD		–0.3	V_{CC} + 0.3	V
V_{ref}	DC voltage at pin V_{ref}		–0.3	V_{CC} + 0.3	V
V_S	DC voltage at pin S		–0.3	V_{CC} + 0.3	V
$V_{trt(CANH)}$	transient voltage at pin CANH	note 1	–200	+200	V
$V_{trt(CANL)}$	transient voltage at pin CANL	note 1	–200	+200	V
V_{es}	electrostatic discharge voltage at all pins	note 2	–4000	+4000	V
		note 3	–200	+200	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+125	°C
T_{vj}	virtual junction temperature	note 4	–40	+150	°C

Notes

1. The waveforms of the applied transients shall be in accordance with *"ISO 7637 part 1"*, test pulses 1, 2, 3a and 3b (see Fig.4).
2. Human body model: C = 100 pF and R = 1.5 kΩ. In case of a discharge from pin CANH to all other non-supply pins: $-3750\text{ V} < V_{es} < +3750\text{ V}$.
3. Machine model: C = 200 pF, R = 10 Ω and L = 0.75 μH. In case of a discharge from pin CANL to pin GND: $-100\text{ V} < V_{es} < +100\text{ V}$; in case of a discharge from pin CANH to V_{CC}: $-150\text{ V} < V_{es} < +150\text{ V}$.
4. In accordance with *"IEC 60747-1"*. An alternative definition of T_{vj} is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

THERMAL CHARACTERISTICS

According to IEC 60747-1.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(vj-a)}$	thermal resistance from junction to ambient in SO8 package	in free air	145	K/W
$R_{th(vj-s)}$	thermal resistance from junction to substrate of bare die	in free air	50	K/W

QUALITY SPECIFICATION

Quality specification *"SNW-FQ-611 part D"* is applicable.

CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; T_{vj} = –40 to +150 °C; R_L = 60 Ω unless specified otherwise; all voltages are referenced to GND (pin 2); positive currents flow into the IC; see notes 1 and 2.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin V_{CC})						
I_{CC}	supply current	dominant; V_{TXD} = 0 V	25	50	75	mA
		recessive; V_{TXD} = V_{CC}	2.5	5	10	mA
Transmitter data input (pin TXD)						
V_{IH}	HIGH-level input voltage	output recessive	2.0	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage	output dominant	–0.3	–	+0.8	V
I_{IH}	HIGH-level input current	V_{TXD} = V_{CC}	–5	0	+5	μA
I_{IL}	LOW-level input current	V_{TXD} = 0 V	–100	–200	–300	μA
C_i	input capacitance	not tested	–	5	10	pF
Mode select input (pin S)						
V_{IH}	HIGH-level input voltage	silent mode	2.0	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage	high-speed mode	–0.3	–	+0.8	V
I_{IH}	HIGH-level input current	V_S = 2 V	20	30	50	μA
I_{IL}	LOW-level input current	V_S = 0.8 V	15	30	45	μA
Receiver data output (pin RXD)						
I_{OH}	HIGH-level output current	V_{RXD} = 0.7V_{CC}	–2	–6	–15	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.45 V	2	8.5	20	mA
Reference voltage output (pin V_{ref})						
V_{ref}	reference output voltage	–50 μA < I_{Vref} < +50 μA	0.45V_{CC}	0.5V_{CC}	0.55V_{CC}	V
Bus lines (pins CANH and CANL)						
$V_{o(reces)(CANH)}$	recessive bus voltage at pin CANH	V_{TXD} = V_{CC}; no load	2.0	2.5	3.0	V
$V_{o(reces)(CANL)}$	recessive bus voltage at pin CANL	V_{TXD} = V_{CC}; no load	2.0	2.5	3.0	V
$I_{o(reces)(CANH)}$	recessive output current at pin CANH	–27 V < V_{CANH} < +32 V; 0 V < V_{CC} < 5.25 V	–2.0	–	+2.5	mA
$I_{o(reces)(CANL)}$	recessive output current at pin CANL	–27 V < V_{CANL} < +32 V; 0 V < V_{CC} < 5.25 V	–2.0	–	+2.5	mA
$V_{o(dom)(CANH)}$	dominant output voltage at pin CANH	V_{TXD} = 0 V	3.0	3.6	4.25	V
$V_{o(dom)(CANL)}$	dominant output voltage at pin CANL	V_{TXD} = 0 V	0.5	1.4	1.75	V
$V_{i(dif)(bus)}$	differential bus input voltage (V_{CANH} – V_{CANL})	V_{TXD} = 0 V; dominant; 42.5 < R_L < 60 Ω	1.5	2.25	3.0	V
		V_{TXD} = V_{CC}; recessive; no load	–50	0	+50	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{o(sc)(CANH)}$	short-circuit output current at pin CANH	V_{CANH} = 0 V; V_{TXD} = 0 V	–45	–70	–95	mA
$I_{o(sc)(CANL)}$	short-circuit output current at pin CANL	V_{CANL} = 36 V; V_{TXD} = 0 V	45	70	100	mA
$V_{i(dif)(th)}$	differential receiver threshold voltage	–12 V < V_{CANL} < +12 V; –12 V < V_{CANH} < +12 V; see Fig.5	0.5	0.7	0.9	V
$V_{i(dif)(hys)}$	differential receiver input voltage hysteresis	–12 V < V_{CANL} < +12 V; –12 V < V_{CANH} < +12 V; see Fig.5	50	70	100	mV
$R_{i(cm)(CANH)}$	common mode input resistance at pin CANH		15	25	35	kΩ
$R_{i(cm)(CANL)}$	common mode input resistance at pin CANL		15	25	35	kΩ
$R_{i(cm)(m)}$	matching between pin CANH and pin CANL common mode input resistance	V_{CANH} = V_{CANL}	–3	0	+3	%
$R_{i(dif)}$	differential input resistance		25	50	75	kΩ
$C_{i(CANH)}$	input capacitance at pin CANH	V_{TXD} = V_{CC}; not tested	–	7.5	20	pF
$C_{i(CANL)}$	input capacitance at pin CANL	V_{TXD} = V_{CC}; not tested	–	7.5	20	pF
$C_{i(dif)}$	differential input capacitance	V_{TXD} = V_{CC}; not tested	–	3.75	10	pF
$I_{LI(CANH)}$	input leakage current at pin CANH	V_{CC} = 0 V; V_{CANH} = 5 V	100	170	250	μA
$I_{LI(CANL)}$	input leakage current at pin CANL	V_{CC} = 0 V; V_{CANL} = 5 V	100	170	250	μA
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		155	165	180	°C
Timing characteristics (see Figs.6 and 7)						
$t_{d(TXD-BUSon)}$	delay TXD to bus active	V_S = 0 V	25	55	110	ns
$t_{d(TXD-BUSoff)}$	delay TXD to bus inactive	V_S = 0 V	25	60	95	ns
$t_{d(BUSon-RXD)}$	delay bus active to RXD	V_S = 0 V	20	50	110	ns
$t_{d(BUSoff-RXD)}$	delay bus inactive to RXD	V_S = 0 V	45	95	155	ns
$t_{dom(TXD)}$	TXD dominant time for time-out	V_{TXD} = 0 V	250	450	750	μs

Notes

1. All parameters are guaranteed over the virtual junction temperature range by design, but only 100% tested at 125 °C ambient temperature for dies on wafer level and in addition to this 100% tested at 25 °C ambient temperature for cased products, unless specified otherwise.
2. For bare die, all parameters are only guaranteed if the backside of the bare die is connected to ground.

APPLICATION AND TEST INFORMATION

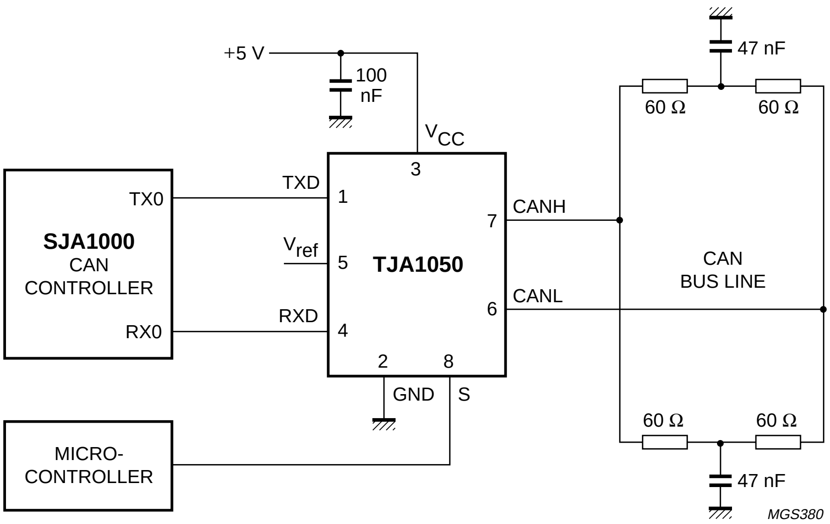
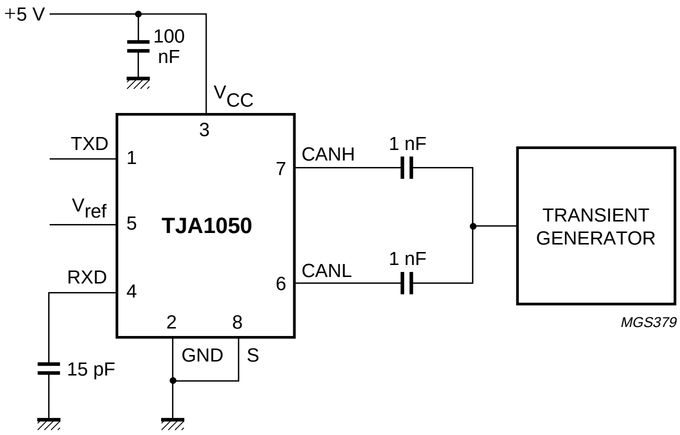


Fig.3 Application information.



The waveforms of the applied transients shall be in accordance with *"ISO 7637 part 1"*, test pulses 1, 2, 3a and 3b.

Fig.4 Test circuit for automotive transients.

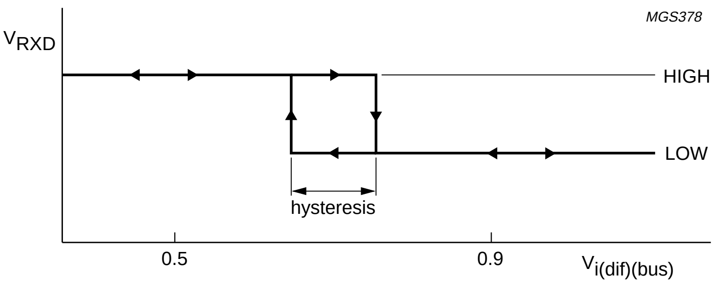


Fig.5 Hysteresis of the receiver.

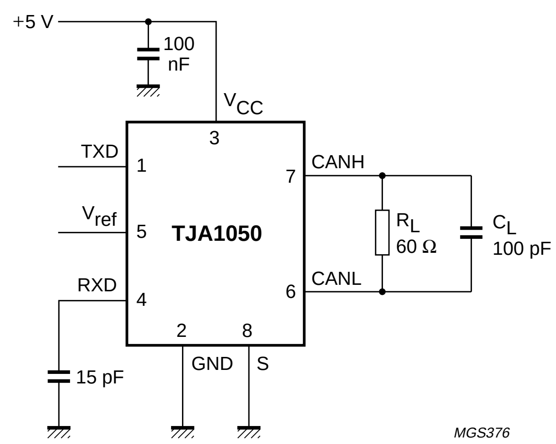
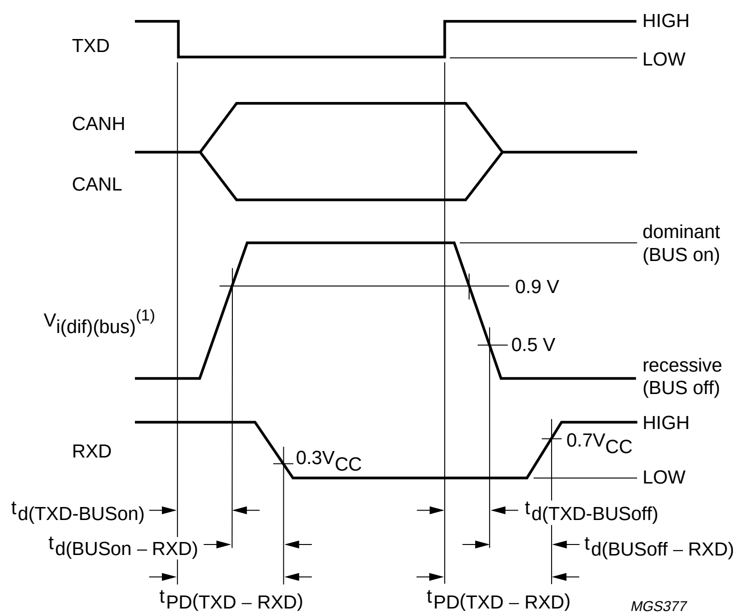


Fig.6 Test circuit for timing characteristics.



(1) $V_{i(dif)(bus)} = V_{CANH} - V_{CANL}$.

Fig.7 Timing diagram for AC characteristics.

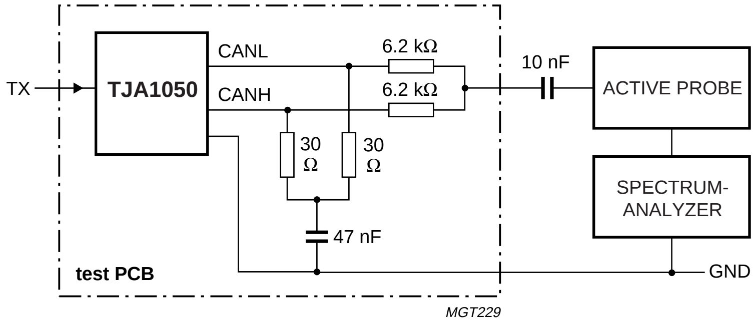
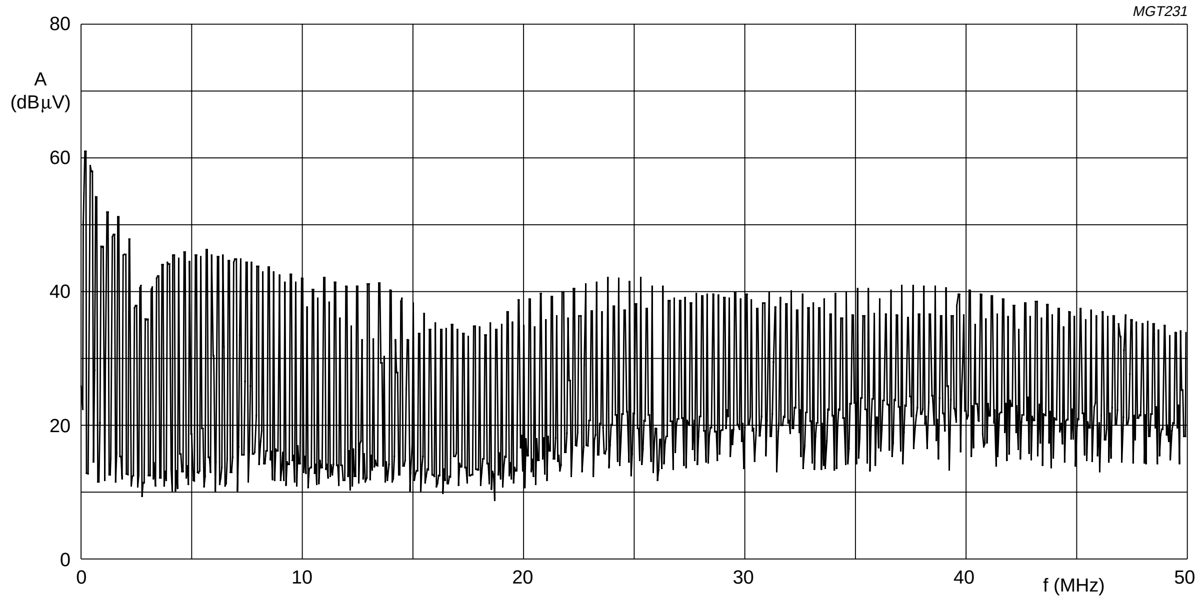
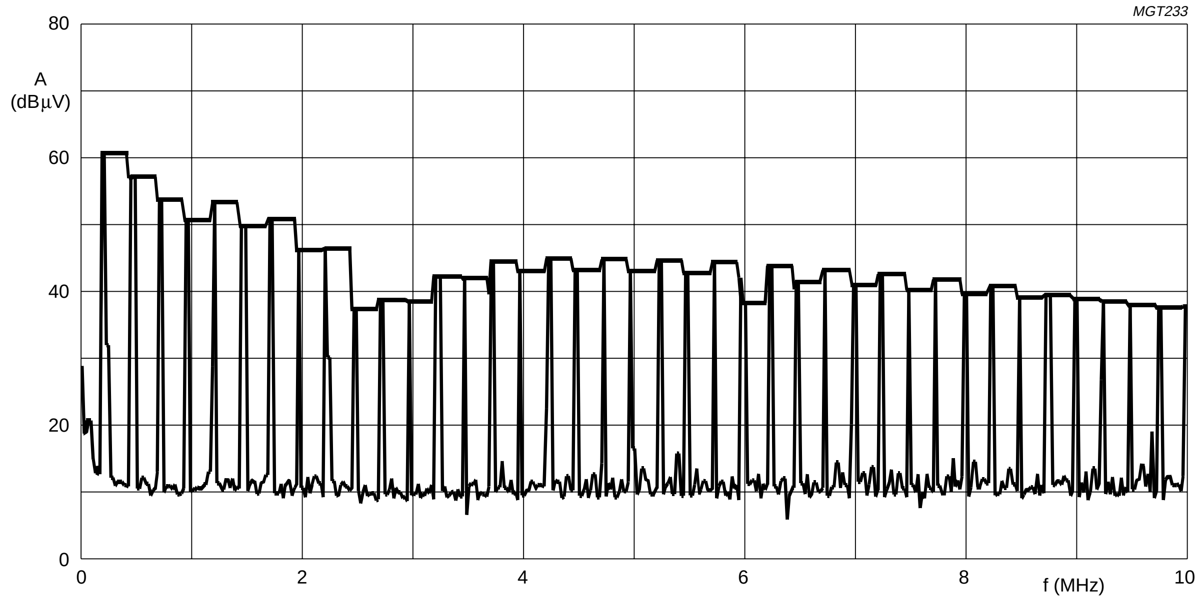


Fig.8 Basic test set-up (with split termination) for electromagnetic emission measurement (see Figs 9 and 10).



Data rate of 500 kbits/s.

Fig.9 Typical electromagnetic emission up to 50 MHz (peak amplitude measurement).



Data rate of 500 kbits/s.

Fig.10 Typical electromagnetic emission up to 10 MHz (peak amplitude measurement and envelope on peak amplitudes).

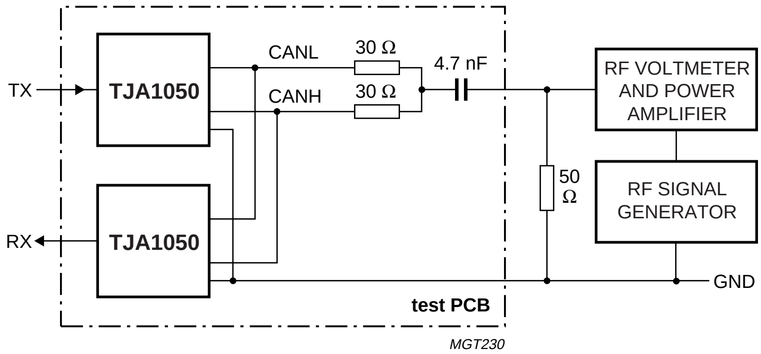
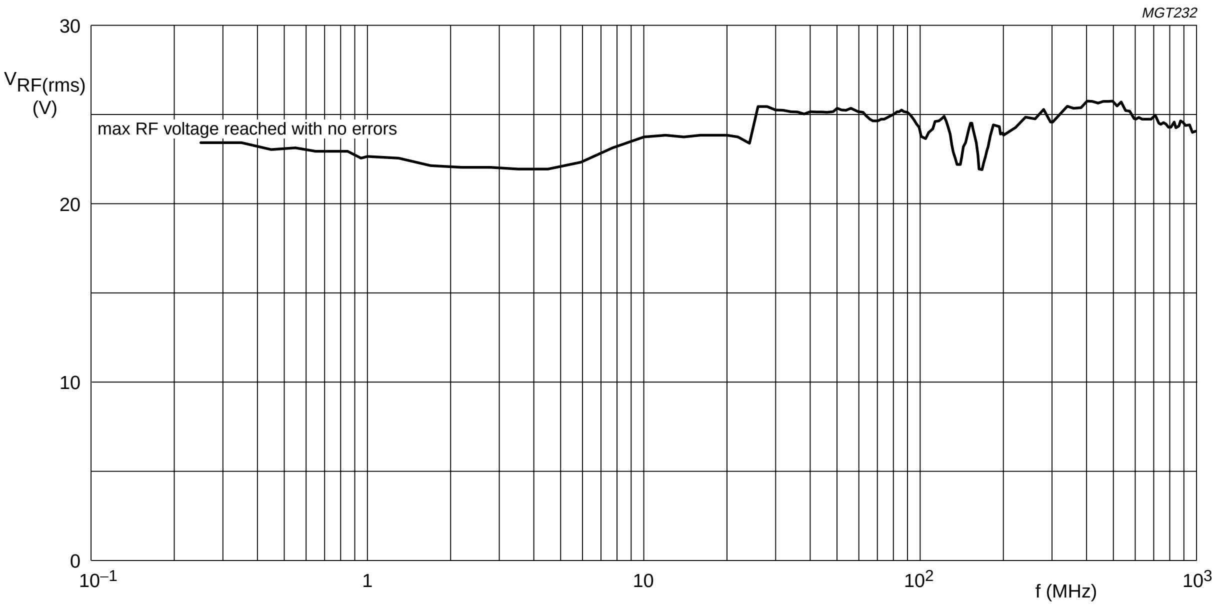


Fig.11 Basic test set-up for electromagnetic immunity measurement (see Fig.12).



Data rate of 500 kbits/s.

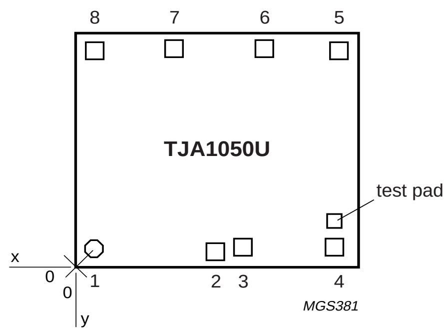
Fig.12 Typical electromagnetic immunity.

BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES[1]	
		x	y
TXD	1	103	103
GND	2	740	85
V_{CC}	3	886.5	111
RXD	4	1371.5	111
V_{ref}	5	1394	1094
CANL	6	998	1115
CANH	7	538.5	1115
S	8	103	1097

Note

1. All x/y coordinates represent the position of the centre of each pad (in µm) with respect to x/y = 0 of the die (see Fig.13).

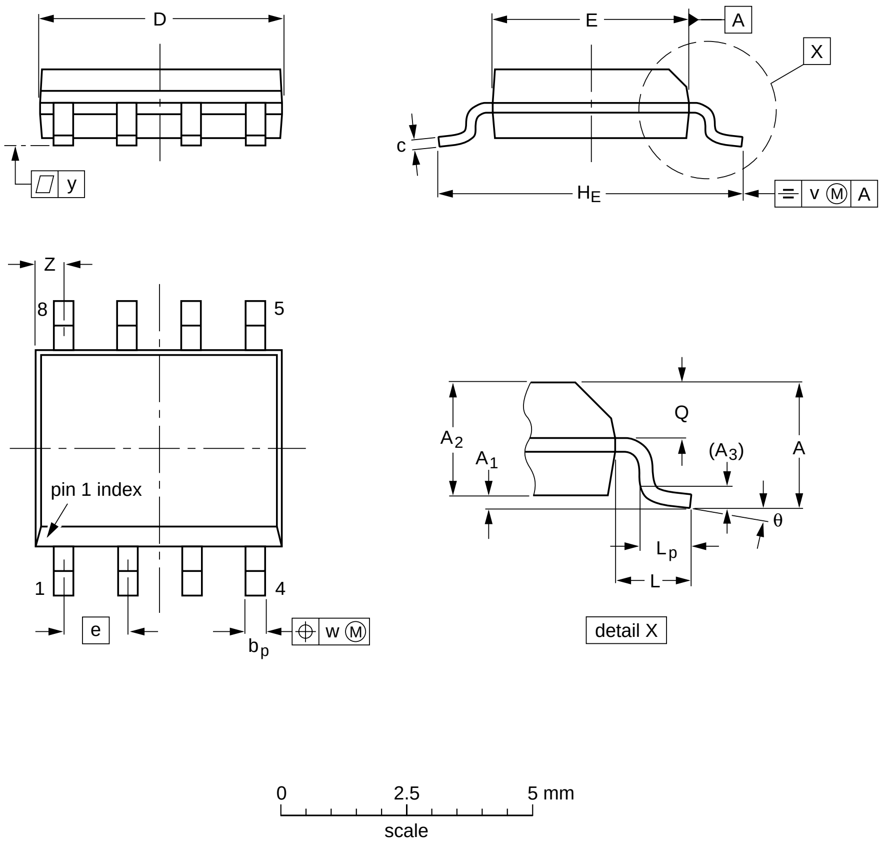


The backside of the bare die must be connected to ground.

Fig.13 Bonding pad locations.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing for a period of ninety (90) days from the date of Philips' delivery. If there are data sheet limits not guaranteed, these will be separately indicated in the data sheet. There are no post packing tests performed on individual die or wafer. Philips Semiconductors has no control of third party procedures in the sawing, handling, packing or assembly of the die. Accordingly, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems after third party sawing, handling, packing or assembly of the die. It is the responsibility of the customer to test and qualify their application in which the die is used.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140, Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V, Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI), Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW, Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 58088 Newville 2114, Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye, ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

SCA69

Printed in The Netherlands 02/pp20 Date of release: 2000 May 26 Document order number: 9397 750 07004

Let's make things better.

Philips Semiconductors

PHILIPS