Wireless Components

ASK/FSK Transmitter 868/433 MHz

TDA 5101 Version 1.3

Specification March 2000

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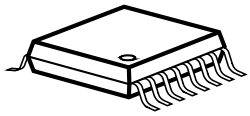
Productinfo

General Description

The TDA5101 is a single chip ASK/FSK transmitter for the frequency 314-316 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery live. Additionally features like a power down mode, a low power detect and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

Package



Features

- fully integrated frequency synthesizer
- VCO without external components
- high efficiency power amplifier
- frequency range 314-316 MHz
- ASK/FSK modulation
- low supply current (typically < 7mA)
- voltage supply range 2.1 - 4 V
- power down mode
- low voltage sensor
- low external component count

Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

Ordering Information

Type	Ordering Code	Package
TDA 5101	Q67036-A1120	P-TSSOP-16
available on tape and reel		

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The TDA5101 is a single chip ASK/FSK transmitter for the frequency band from 314 to 316 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery live. Additionally features like a power down mode, a low power detect and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

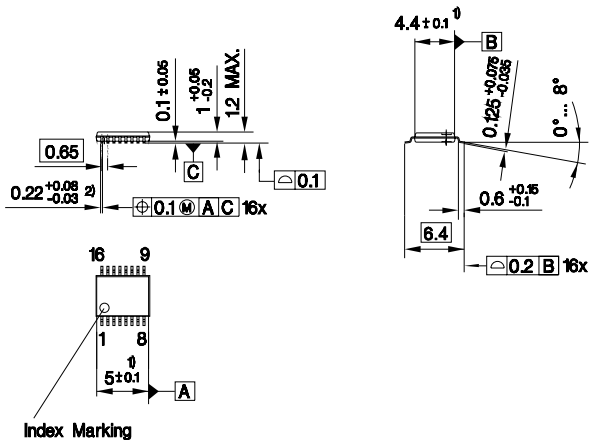
2.2 Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

2.3 Features

- fully integrated frequency synthesizer
- VCO without external components
- high efficiency power amplifier
- frequency range 314-316 MHz
- ASK/FSK modulation
- low supply current (typically < 7mA)
- voltage supply range 2.1 - 4 V
- power down mode
- low voltage sensor
- low external component count

2.4 Package Outlines



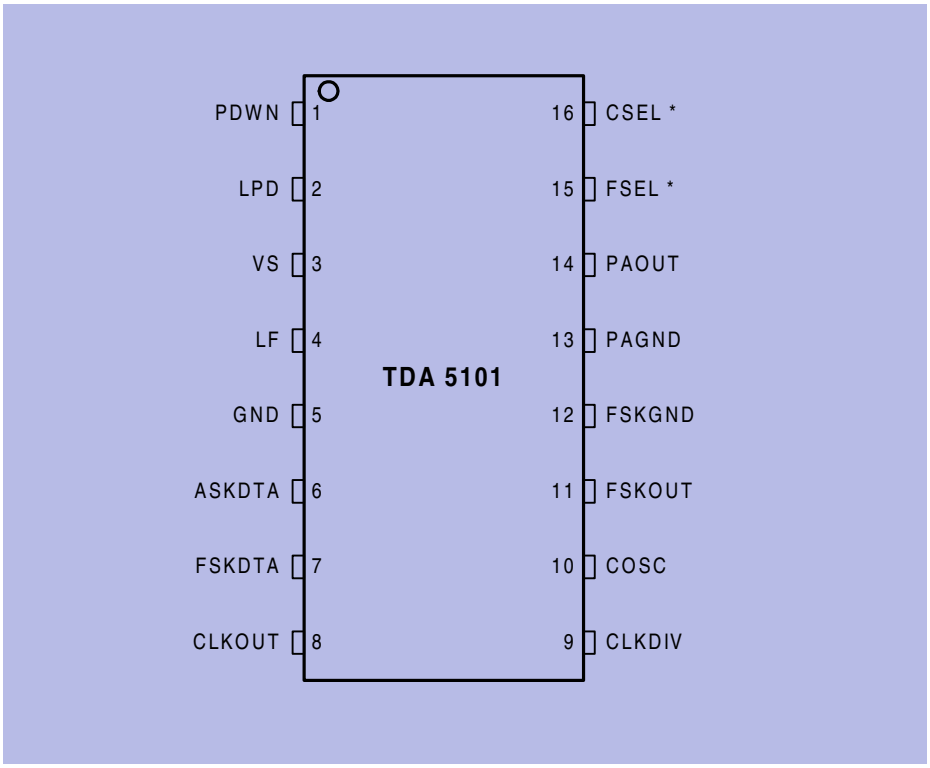
1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 2-1 P-TSSOP-16

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration



Pin_config.wmf

Figure 3-1 IC Pin Configuration

* For applications in the 315 MHz band:
CSEL always open, FSEL always shortened to ground

3.2 Pin Definition and Function

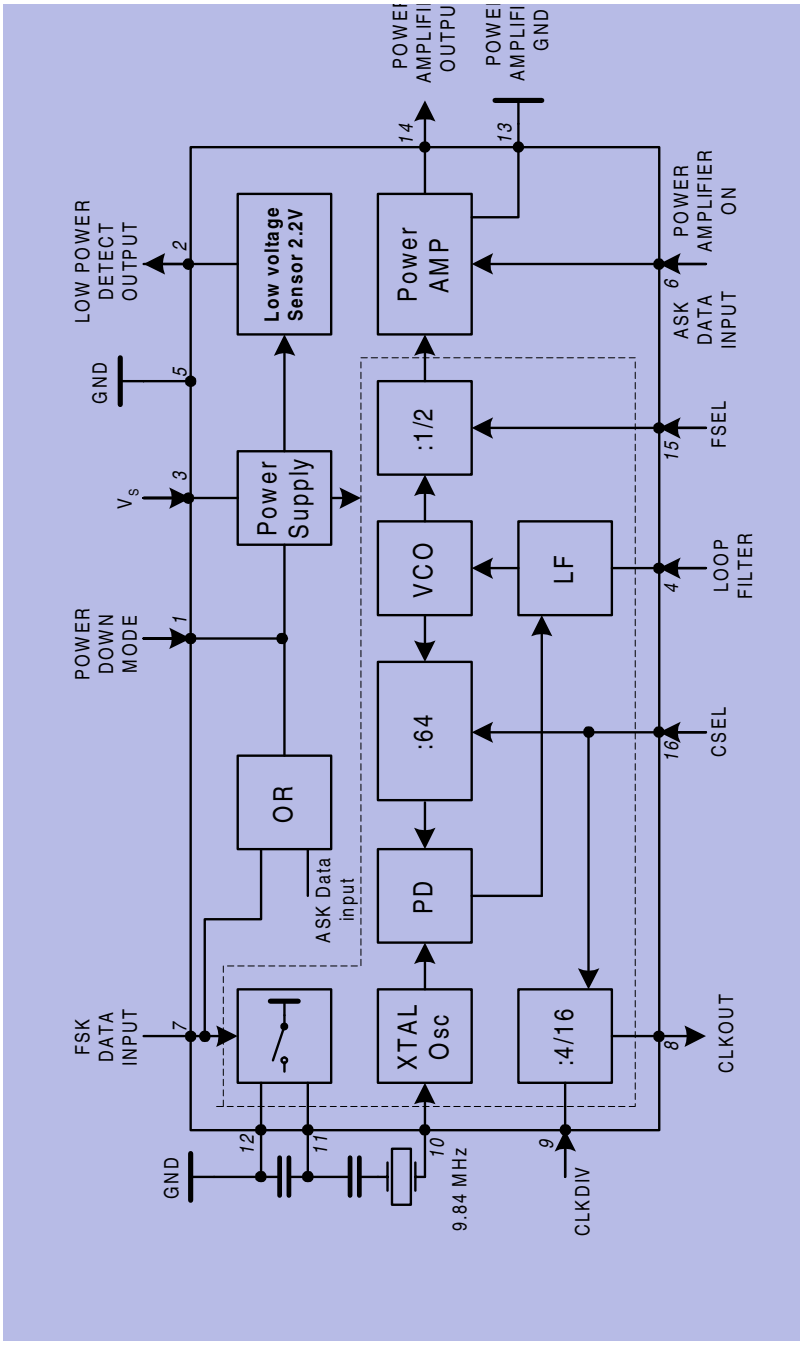
Table 3-1 Pin Configuration

Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	PDWN		Power down mode
2	LPD		Low power detect output
3	VS		Voltage supply
4	LF		Loop filter
5	GND		Ground
6	ASKDTA		Amplitude Shift Keying data input
7	FSKDTA		Frequency Shift Keying data input
8	CLKOUT		Clock output
9	CLKDIV		Clock divider control
10	COSC		Crystal oscillator input
11	FSKOUT		Frequency Shift Keying output
12	FSKGND		Frequency Shift Keying ground
13	PAGND		Power amplifier ground
14	PAOUT		Power amplifier output
15	FSEL *		FSEL always shortend to ground
16	CSEL *		CSEL always open

* For applications in the 315 MHz band:

CSEL always open, FSEL always shortened to ground

3.3 Block diagram



Block_diagram.wmf

Figure 3-2 Main Block Diagram

3.4 Functional Blocks

1. PLL Synthesizer

The Phase Locked Loop synthesizer consists of a voltage controlled oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter and is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 630 MHz. The oscillator signal is fed both to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asyncronous divider chain is 64. The phase detector is a Typ IV PD with charge pump. The passive loop filter is realized on chip. In all 315 MHz applications, the CSEL pin is not connected.

2. Crystal Oscillator

The crystal oscillator operates at 9.84 MHz. In case of FSK transmission the oscillator frequency can be detuned by a fixed amount determined by an external capacitor via pin 7 (FSKDTA). 615 kHz or 2.40 MHz are available as a clock frequency output (CLKOUT) to drive the clock input of a micro controller. The dividing ratio is controlled by the CLKDIV pin.

Table 3-2

FSKDTA	FSKOUT Switch
Open	OFF
Shorted to ground	ON

Table 3-3

CLKDIV	Dividing Ratio
Shortened to ground	4
Open	16

3. Power Amplifier

In FSK transmission the power amplifier can be switched on with pin 6 (ASKDTA). In case of ASK transmission the same pin is used as the data input.

The PAOUT pin is an open collector output and requires an external pull up coil to provide bias. The coil is part of the tuning and matching LC cuircit to get best performance with the external loop antenna. To achieve the best power amplifier efficiency the high frequency voltage peak to peak swing at the PAOUT pin should be two times the supply voltage.
The power amplifier has its own ground pin (PAGND) in order to reduce the amount of coupling to the other circuits.
In all 315 MHz applications, the pin FSEL is to connect to ground.

4. Low Power Detect

The supply voltage is sensed by a low power detector. If the supply voltage drops below 2.15 V, the LPD pin (pin2) switches to low. The minimum sink current is 1 mA. To spare at most cases the external pull up resistor, an internal pull up current of 30µA is implemented.
A simple application of this feature is the switching off of the power amplifier via pin 6.

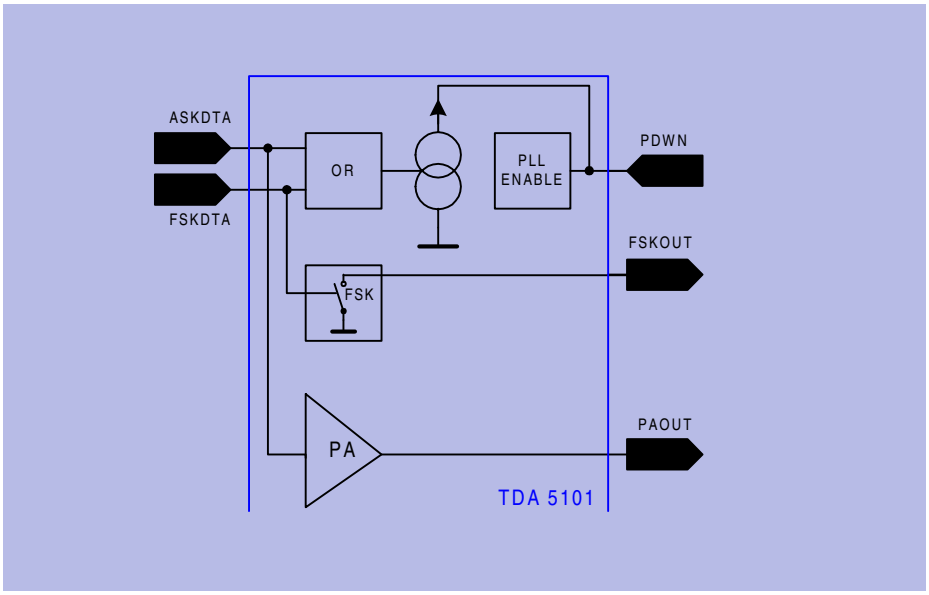
5. Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE. How to get in this modes is described in the table below.

Table 3-4

PDWN	FSKDTA	ASKDTA	
L	L	L	POWER DOWN MODE
H	L;H	L	PLL ENABLE MODE
not connected;H	H	L	PLL ENABLE MODE
not connected,H	L;H	H	TRANSMIT MODE

If ASKDTA or FSKDTA gets high, the PDWN pin is pulled up internally via a current source as shown in the diagram below. Therefore, in most applications it is not necessary and recommended to connect the PDWN pin.



Power_Mode.wmf

Figure 3-3 Power mode

6. Power Down Mode

In the POWER DOWN MODE the current consumption is less than 100nA. To switch the IC in this mode, the input pins PDWN (pin1), ASKDTA (pin6) and FSKDTA (pin7) has to be in the low state.

7. PLL Enable Mode

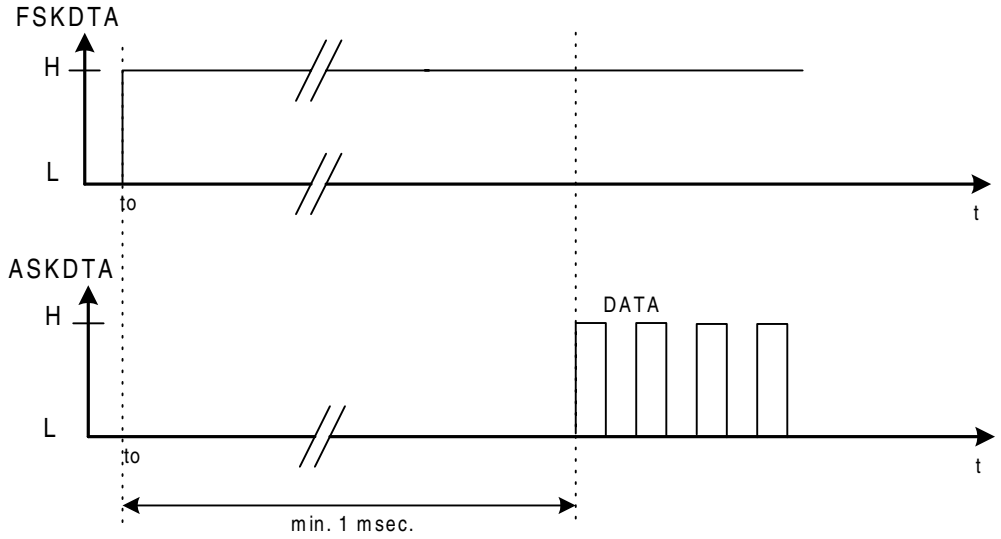
The turn on time of the PLL is determined by the turn on time of the crystal oscillator and is typically less than 1 msec (dependent on the crystal itself). To save current consumption and to avoid undesired power radiation during this time, the power amplifier is turned off. The current consumption at this mode is typically 3.5 mA.
To have the possibility to control the IC via two data lines from a micro processor, the ASK- and FSK Data inputs are connected via a “logical or” to pull up internally the PDWN input. In this case, it is recommended to leave the PDWN pin unconnected.

8. Transmit Enable Mode

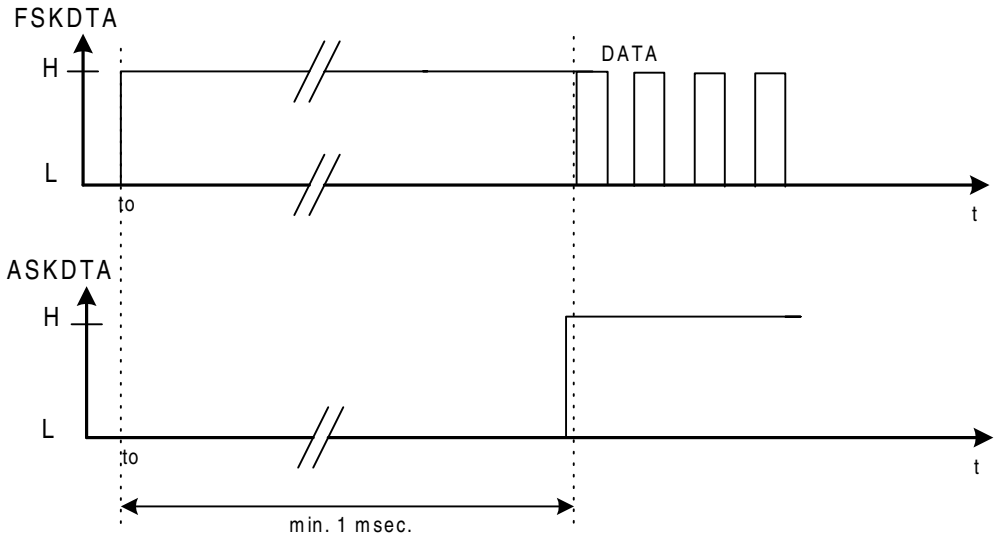
In the TRANSMIT ENABLE MODE the power amplifier is turned on too, and the current consumption of the IC is about 7 mA. To get in this state, the ASKDTA input is to switch to a high level.

9. Recommended timing diagrams for ASK- and FSK modulation

ASK Modulation :
(Pin1 (PDWN) not connected)
Figure 3-4 ASK Modulation



FSK Modulation:
(Pin1 (PDWN) not connected)
Figure 3-5 FSK Modulation



4 Applications

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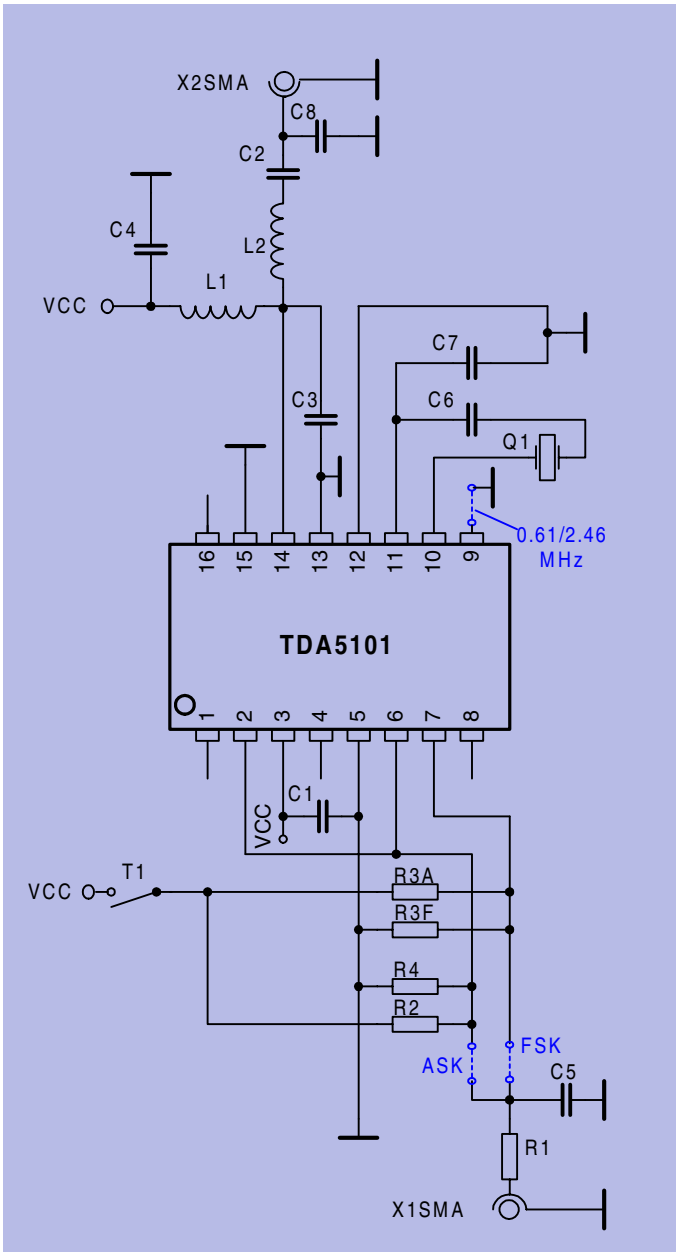
4.1 Circuits



50ohm_test_v5.wmf

Figure 4-1 50Ω testboard

4.2 Test Board Layouts

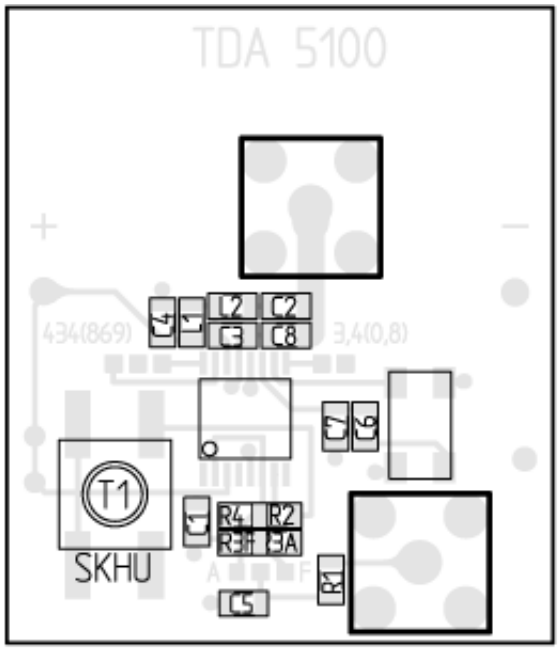


Figure 4-2 Top Side of TDA 5101 (identical to TDA 5100)

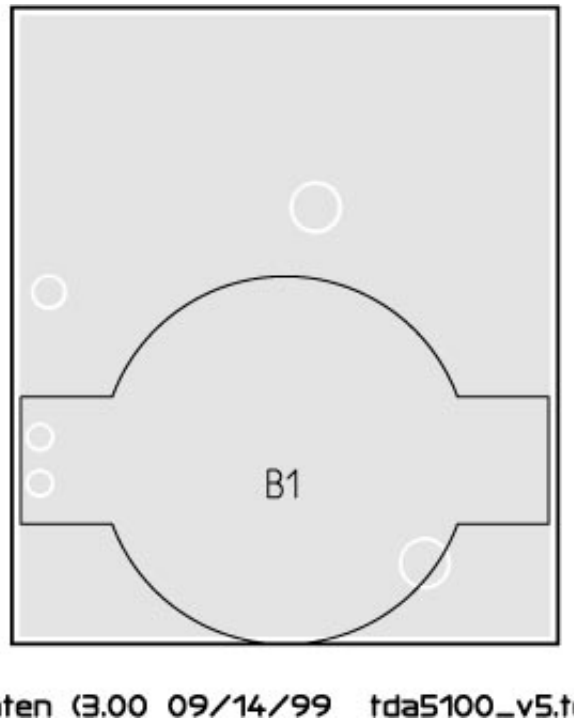


Figure 4-3 Bottom Side of TDA 5101 (identical to TDA 5100)

4.3 Bill of material (Testboard)

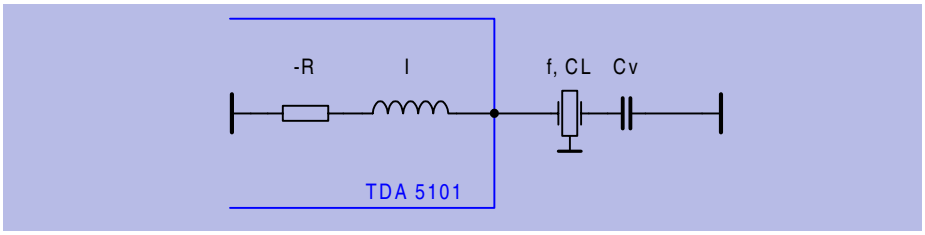
Table 4-1 Bill of material

Part	Value	315 MHz	ASK	FSK	Specification
R1	4.7 kΩ				0805, ± 5%
R2				12 kΩ	0805, ± 5%
R3A			15 kΩ		0805, ± 5%
R3F				15 kΩ	0805, ± 5%
R4	open				0805, ± 5%
C1	47 nF				0805,X7R, ± 10%
C2		56 pF			0805, COG, ± 5%
C3		5.6 pF			0805, COG, ± 0.1 pF
C4		330 pF			0805, COG, ± 5%
C5	1 nF				0805,X7R, ± 10%
C6	8.2 pF				0805, COG, ± 0.1 pF
C7			0Ω Jumper	47 pF	0805, COG, ± 5% 0805 0Ω Jumper
C8		22 pF			0805, COG, ± 5%
L1		220 nH			TOKO LL2012-J
L2		56 nH			TOKO LL2012-J
Q3	9.84375 MHz, CL=12pF				Tokyo Denpa TSS-3B 9843,75 kHz Spec.No. 20-18905
IC1		TDA5101			
T1	Taster				replaced by a short
X1	SMA-S				SMA standing
X2	SMA-S				SMA standing

4.4 Hints

1. Application Hints to the crystal oscillator

As mentioned before, the crystal oscillator achieves a turne on time less than 1 msec. To attend this, a NIC oscillator type is implemented in the TDA5101. This oscillator type has the property, that the input impedance is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.



$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 l}$$

CL: crystal load capacitance for nominal frequency
ω: angular frequency
l: inductivity of the crystal oscillator

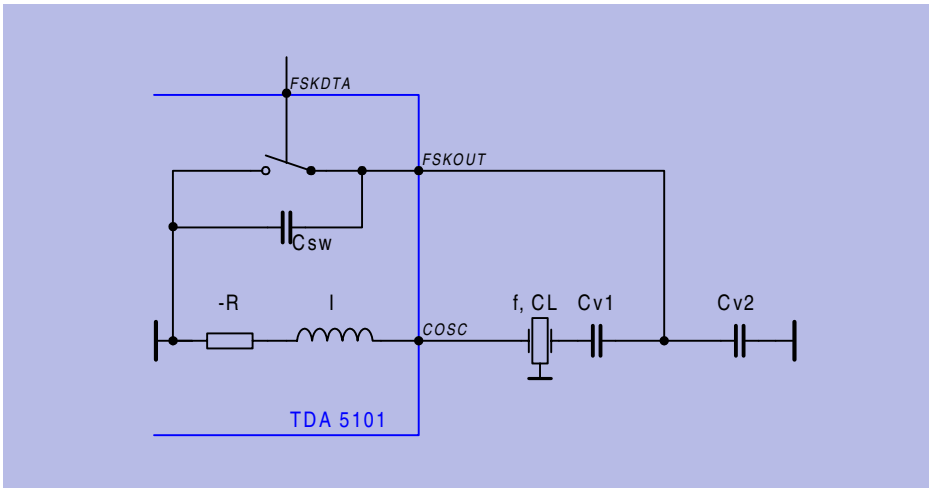
Example for the ASK-Mode:

Refering to the application circuit, in ASK-Mode the capacitance C7 is replaced by a short to ground. Assuming a crystal frequency of 9.84 MHz and a crystal load capacitance of CL=20pF. The inductance l is specified within the electrical characterisics at 9.84 MHz to a value of 11uH. Therefore C6 is calculated to ???.

$$C6 = \frac{1}{\frac{1}{CL} + \omega^2 l} = Cv$$

Example for the FSK-Mode:

FSK modulation is achieved by switching the load capacitance of the crystal as shown below.



The frequency deviation of the crystal oscillator is multiplied with the divider factor N of the Phase Locked Loop to the output of the power amplifier. In case of small fequency deviations (up to +/- 1000ppm), the two desired load capacitances can be calculated with the formula below.

$$CL\pm = \frac{CL \mp C0\frac{\Delta f}{N * f1}(1+\frac{2(C0+CL)}{C1})}{1\pm\frac{\Delta f}{N * f1}(1+\frac{2(C0+CL)}{C1})}$$

C_L: crystal load capacitance for nominal frequency
C_0: shunt capacity of the crystal
ω: angular frequency
N: divider factor of the PLL
df: peak frequency deviation

Because of the inductive part of the TDA5101 this values must be corrected by formula 1). Therefore Cv± can be calculated.

$$Cv\pm = \frac{1}{\frac{1}{CL\pm} + \omega^2 l}$$

If the FSK switch is closed, Cv_ is equal to Cv1 (C6 in the application diagram). If the FSK switch is open, Cv2 (C7 in the application diagram)can be calculated.

$$Cv2 = C7 = \frac{Csw * Cv1 - (Cv+) * (Cv1 + Csw)}{(Cv+) - Cv1}$$

Csw: parallel capacitance of the FSK switch (1 pF)

Remark: This calculations are only approximations. The exact values must be found in the specific application board

2. Design hints to the buffered clock output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) is to connect between this pin and the supply voltage. The value of RL is dependent on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the microcontroler). RL can be calculated to:

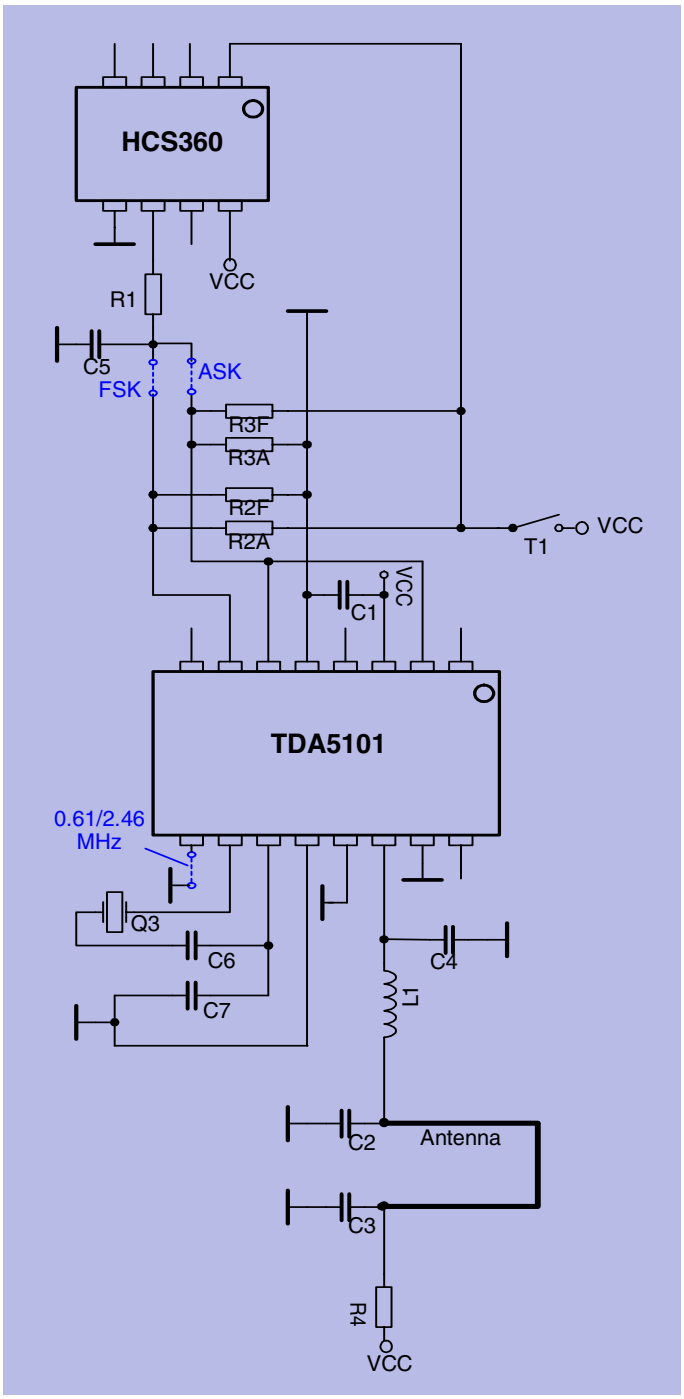
$$RL = \frac{1}{fCLKOUT * 8 * CLD}$$

Table 4-2

	fCLKOUT= 615 kHz	fCLKOUT= 2.40 MHz
CL/pF	RL/kOhm	RL/kOhm
5	39	10
10	18	5.1
20	10	2.2

Remark: Because of the reason of a low current consumption and a low spurious radiation the largest possible RL should be choosen.

4.5 Application Circuit



Application_circuit.wmf

Figure 4-4 Application Circuit

4.6 Test Board Layouts

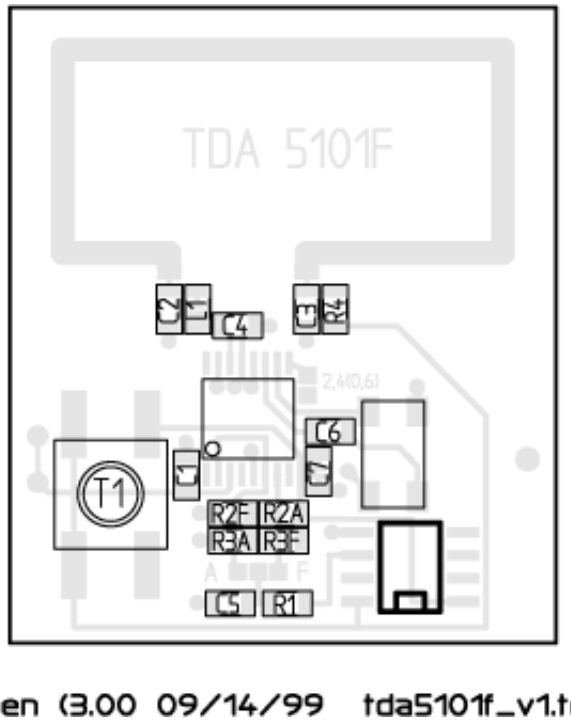


Figure 4-5 Top Side of TDA 5101

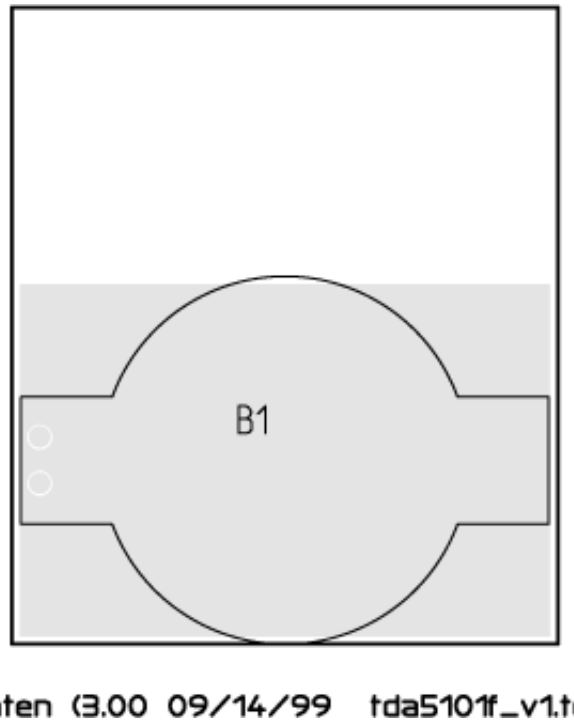


Figure 4-6 Bottom Side of TDA 5101

4.7 Bill of material (Application Circuit)

Table 4-3 Bill of material

Part	Value	315 MHz	ASK	FSK	Specification
R1	4.7 kΩ				0805, ± 5%
R2A			15 kΩ		0805, ± 5%
R2F				12 kΩ	0805, ± 5%
R3A	15 kΩ				0805, ± 5%
R3F				12 kΩ	0805, ± 5%
R4	1 kΩ				0805, ± 5%
C1	47 nF				0805,X7R, ± 10%
C2	18 pF				0805, COG, ± 1%
C3	330 pF				0805, COG, ± 10%
C4	10 pF				0805, COG, ± 1%
C5	4.7 nF				0805, X7R, ± 10%
C6	8.2 pF				0805, COG, ± 0.1 pF
C7			open	47 pF	0805, COG, ± 10%
L1	39 nH				TOKO LL2012-J
Q3	9.84375 MHz CL=12pF				Tokyo Denpa TSS-3B 9843.75kHz Spec.No. 20-18905
IC1	TDA5101				Infineon
IC2	HCS360				Microchip
B1	Batteriehalter				HU2031-1, RENATA
T1	Taster				STTSKHMPW, ALPS

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

The AC / DC characteristic limits are not guaranteed. The maximum ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Table 5-1

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Junction Temperature	T_J	-40	150	°C	
Storage Temperature	T_s	-40	125	°C	
Thermal Resistance	R_{thSA}		tbd.	K/W	
ESD integrity, all pins	V_{ESD}	-1	+1	kV	100pF, 1500 Ω

Ambient Temperature under bias: T_A=-25 to +85°C

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed

Table 5-2

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min	Max		
Supply voltage	V_S	2.1	4.0	V	
Ambient temperature	T_A	-25	85	°C	

5.1.3 AC/DC Characteristics

Table 5-3 Supply Voltage V_S = 3V, Ambient temperature T_{amb} = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Stand by mode	$I_{S\ PDWN}$			100	nA	Pins 6,7,9,15 and 16 =0V or N.C.
PLL enable	$I_{S\ PLL\_EN}$		3.3	4.2	mA	
Transmit enable	$I_{S\ TRANSM}$		7	9	mA	Load tank see fig. 4-1*
Power Down Modeswitch						
Stand by mode	V_{PDWN}	0		0.7	V	V_{ASKDTA} < 0.2V V_{FSKDTA}< 0.2V
PLL enable	V_{PDWN}	1.5		Vs	V	V_{ASKDTA} < 0.5V
Transmit enable	V_{PDWN}	1.5		Vs	V	V_{ASKDTA} > 1.4V
Input bias current PDWN	I_{PDWN}			30	µA	V_s = 4V
Low Power Detect						
Internal pull up current	I_{LPD1}	30			µA	V_s = 2.3 ... 4V
Input current low voltage	I_{LPD2}	1			mA	V_s = 1.9 ... 2.1V
VCO tuning voltage	V_{LF}	Vs-1.6		Vs-0.6	V	PLL locked
ASK Modulation						
ASK Transmit disable	V_{ASKDTA}	0		0.5	V	FSK Switch disable
ASK Transmit enable	V_{ASKDTA}	1.5		Vs	V	FSK Switch disable
Input bias current ASKDTA	I_{ASKDTA}			30	µA	V_{ASKDTA} =Vs
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0V
ASK data rate	f_{ASKDTA}			20	kHz	
FSK Modulation						
FSK Switch on	V_{FSKDTA}			0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		Vs	V	
Input bias current FSKDTA	I_{FSKDTA}			30	µA	V_{FSKDAT}= Vs
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDAT}= 0V
FSK data rate	f_{FSKDTA}			20	kHz	
CLOCK driver output						
Output current	I_{CLKOUT}	1			mA	
CLOCK divider control						
Buffered clock output for f=fCRSTL/2 or f=fCRSTL/8	V_{CLKDIV}	0		0.2	V	
Buffered clock output for f=fCRSTL/4 or f=fCRSTL/16	V_{CLKDIV}	1.5		Vs	V	or pin open
Input bias current CLKDIV	I_{CLKDIV}			30	µA	V_{CLKDIV} =Vs

Table 5-3 Supply Voltage V_S = 3V, Ambient temperature T_{amb} = 25 °C (continued)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
CLOCK divider control						
Input bias current CLKDIV	I_{CLKDIV}	-20			µA	V_{CLKDIV} = 0V
Crystal oscillator input						
Load capacitance	$C_{COSC-max}$			5	pF	
Serial Resistance of the crystal				100	Ohm	f=9.84 MHz
Input inductance of the COSC pin			12		µH	f=9.84 MHz
FSK output switch						
On resistance	R_{FSKOUT}			250	Ohm	
On capacitance	C_{FSKOUT}		1		pF	
Off resistance	R_{FSKOUT}	10k			Ohm	
Off capacitance	C_{FSKOUT}		1.5		pF	
Power amplifier output, transformed to 50 Ohm						
Output Power*	P_{PAOUT}	3	5	7	dBm	f=315 MHz

*Power amplifier in overcritical C-operation