SiGe Power Amplifier for CW Applications

Description

The T0931 is a monolithic integrated power amplifier IC. The device is manufactured in TEMIC Semiconductors' Silicon-Germanium (SiGe) technology and has been designed for use in 900-MHz two-way pagers, PDAs, meter readers and ISM phones.

With a single supply voltage operation of + 2.4 to 3.4 V and a neglectable leakage current in power-down mode, the pager amplifier needs less external components and thus helps to reduce system costs. It is suited for operation in CW mode.

Features

- Up to 33 dBm output power in CW mode
- Power Added Efficiency (PAE) 47%
- Single supply operation at 2.4 V (1 W) or 3.2 V (2 W) no negative voltage necessary
- Current consumption in power-down mode ≤ 10 μA, no external power supply switch required
- Power ramp control
- Simple input and output matching
- Simple output matching for maximum flexibility
- Flipchip package

Block Diagram

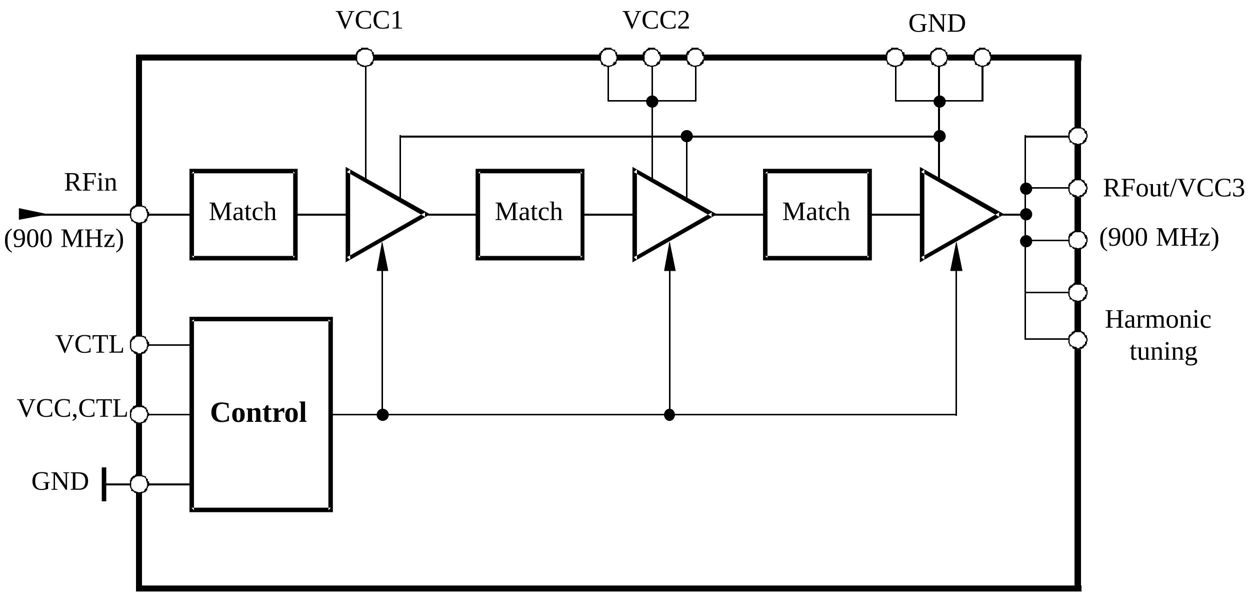


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
T0931-DD	Flipchip	

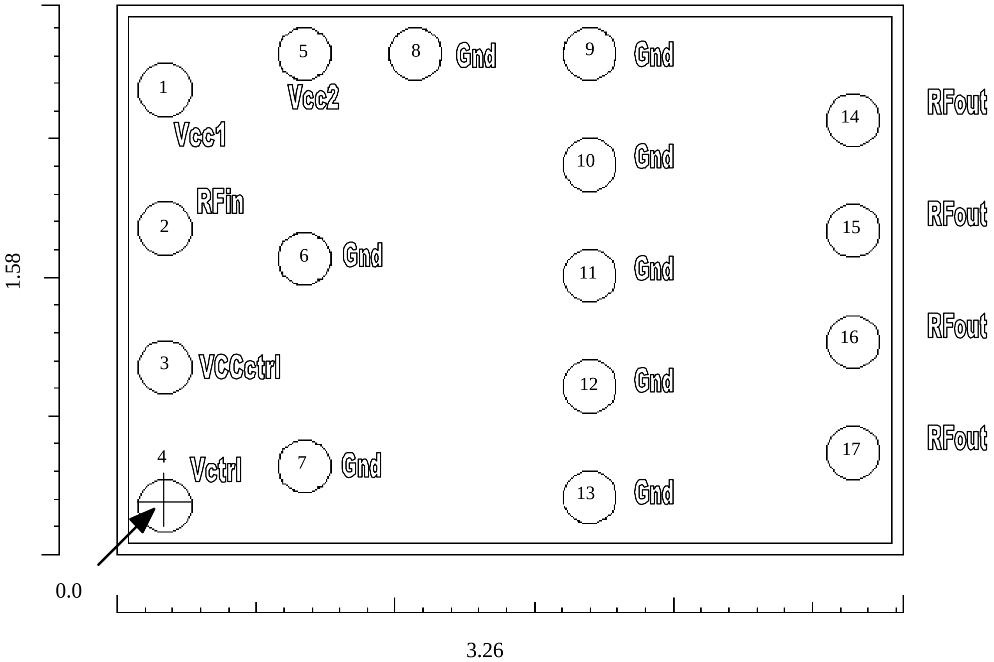
Preliminary Information

Pad Description

Pad	Symbol	Function	X-Coordinate of Pad *) (µm)	Y-Coordinate of Pad *) (µm)
1	Vcc1	Supply voltage 1	0	1500
2	RFin	RF input	0	1000
3	VCCctrl	Supply voltage for control	0	500
4	VCTL	Control input	0	0
5	Vcc2	Supply voltage 2	500	1630
6	GND	Ground	500	891
7	GND	Ground	500	142
8	GND	Ground	900	1630
9	GND	Ground	1527	1630
10	GND	Ground	1527	1230
11	GND	Ground	1527	830
12	GND	Ground	1527	430
13	GND	Ground	1527	30
14	RFout/ Vcc3	RF output/ supply voltage 3	2474	1391
15	RFout/ Vcc3	RF output/ supply voltage 3	2474	991
16	RFout/ Vcc3	RF output/ supply voltage 3	2474	591
17	RFout/ Vcc3	RF output/ supply voltage 3	2474	191

*) Relative to centre of Pad 4

Pad Location



Dimensions-scale division = 100 µm, for pad coordinates see Pad Decsription table.

Figure 2. Pad location

Absolute Maximum Ratings

All voltages are referred to GND

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}			4.0	V
Input power	P_{in}			12	dBm
Gain control voltage	V_{CTL}	0		2.0	V
Duty cycle for operation				100	%
Junction temperature	T_j			+150	°C
Storage temperature	T_{stg}	–40		+150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
		t.b.d.	

Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC1} V_{CC2} V_{CC3} $V_{CC,CTL}$	1.8	2.4	3.0	V
Ambient temperature	T_{amb}	– 25		+ 85	°C
Input frequency	f_{in}		900		MHz

Electrical Characteristics for 1 Watt Application

$V_{CC} = V_{CC1}, \ldots, V_{CC3}, V_{CC, CTL}$ = + 2.4 V, V_{CTL} = 1.7 V, T_{amb} = + 25°C, 50-Ω input and 50-Ω external output match

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Supply voltage		V_{CC}	1.8	2.4	3.0	V
Current consumption: active mode	P_{out} = 30 dBm, PAE = 47%	I		0.9		A
Current consumption (leakage current) in power-down mode	$V_{CTL} \leq 0.2$ V	I			10	µA
RF input						
Frequency range		f_{in}	880	900	935	MHz
Input impedance *)		Z_i		50		Ω
Input power		P_{in}		5	12	dBm
Input VSWR *)	P_{in} = 0 to 12 dBm, P_{out} = 30 dBm				2 : 1	
RF output						
Output impedance *)		Z_o		50		Ω
Output power: normal conditions	Pin = 5 dBm, $R_L = R_G$ = 50 Ω V_{CC} = 2.4 V, T_{amb} = +25°C V_{CC} = 1.8 V, T_{amb} = +25°C	 P_{out} P_{out}		 30 27		 dBm dBm
Minimum output power	V_{CTL} = 0.3 V			– 20		dBm
Power-added efficiency	V_{CC} = 2.4 V, P_{out} = 27 dBm V_{CC} = 2.4 V, P_{out} = 30 dBm	PAE PAE		40 47		% %
Stability	Temp = –25 to + 85 °C, no spurious >= –60 dBc	VSWR			10 : 1	
Load mismatch (stable, no damage)	P_{out} = 30 dBm, all phases	VSWR			10 : 1	
Second harmonic distortion		2fo			–35	dBc
Third harmonic distortion		3fo			–35	dBc
Noise power f = 925 to 935 MHz f ≥ 935 MHz	 P_{out} = 30 dBm, RBW = 100 kHz			 –73 –85	 –70 –82	 dBm dBm
Rise and fall time					0.5	µs
Isolation between input and output	P_{in} = 0 to 10 dBm, $V_{CTL} \leq 0.2$ V (power down)		50			dB
Power control						
Control curve	Pout ≥ 25 dBm				150	dB/V
Power control range	V_{CTL} = 0.3 to 2.0 V		50			dB
Control voltage range		V_{CTL}	0.3		2.0	V
Control current	P_{in} = 0 to 10 dBm, V_{CTL} = 0 to 2.0 V	I_{CTL}			200	µA

Note: *) with external matching (see application circuit)

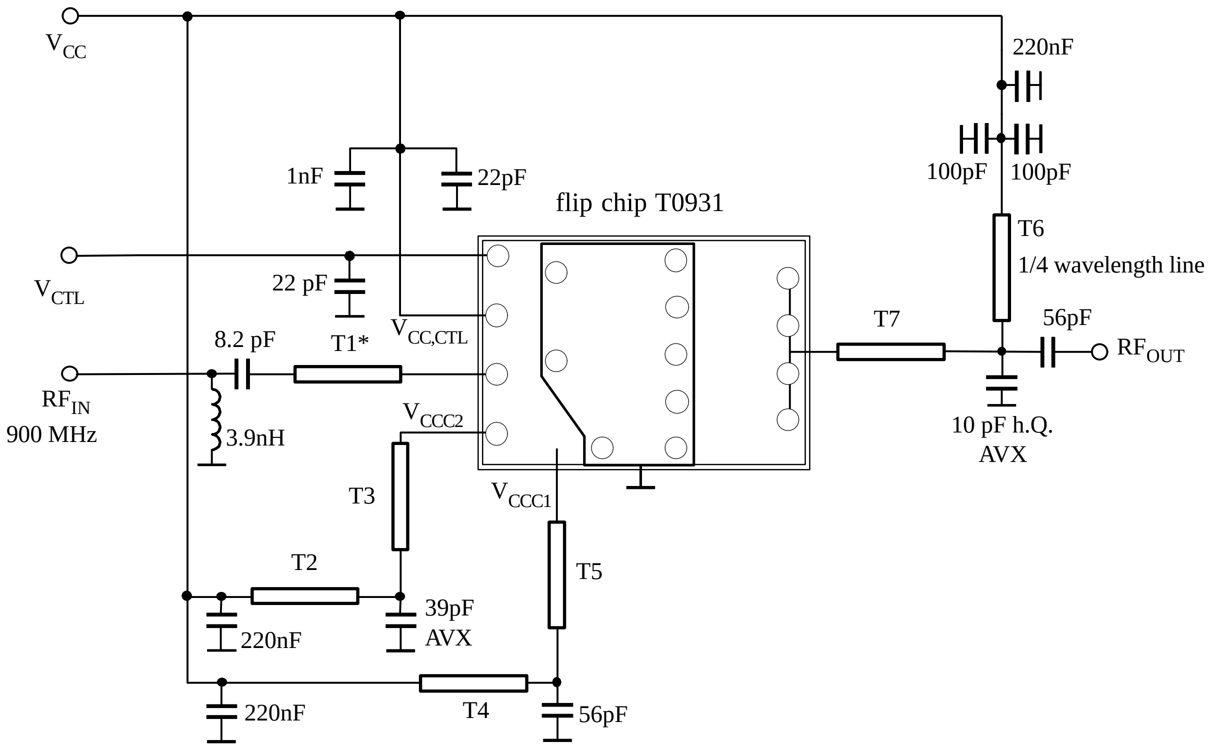
Electrical Characteristics for 2 Watt Application

$V_{CC} = V_{CC1}$, ... , V_{CC3}, $V_{CC, CTL}$ = + 3.2 V, V_{CTL} = 1.9 V, T_{amb} = + 25°C, 50-Ω input and 50-Ω external output match

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Supply voltage		V_{CC}	2.6	3.2	3.6	V
Current consumption: active mode	P_{out} = 33 dBm, PAE = 47%	I		1.33		A
Current consumption (leakage current) in power-down mode	$V_{CTL} \leq 0.2$ V	I			10	µA
RF input						
Frequency range		f_{in}	880	900	935	MHz
Input impedance *)		Z_i		50		Ω
Input power		P_{in}		5	12	dBm
Input VSWR *)	P_{in} = 0 to 12 dBm, P_{out} = 30 dBm				2 : 1	
RF output						
Output impedance *)		Z_o		50		Ω
Output power: normal conditions	Pin = 5 dBm, $R_L = R_G$ = 50 Ω V_{CC} = 3.2 V, T_{amb} = +25°C V_{CC} = 2.2 V, T_{amb} = +25°C	 P_{out} P_{out}		 33 30		 dBm dBm
Minimum output power	V_{CTL} = 0.3 V			– 20		dBm
Power-added efficiency	V_{CC} = 3.2 V, P_{out} = 27 dBm	PAE		47		%
Stability	Temp = –25 to + 85 °C, no spurious >= –60 dBc	VSWR			10 : 1	
Load mismatch (stable, no damage)	P_{out} = 33 dBm, all phases	VSWR			10 : 1	
Second harmonic distortion		2fo			–35	dBc
Third harmonic distortion		3fo			–35	dBc
Noise power f = 925 to 935 MHz f ≥ 935 MHz	 P_{out} = 33 dBm, RBW = 100 kHz			 –73 –85	 –70 –82	 dBm dBm
Rise and fall time					0.5	µs
Isolation between input and output	P_{in} = 0 to 10 dBm, $V_{CTL} \leq 0.2$ V (power down)		50			dB
Power control						
Control curve	Pout ≥ 25 dBm				150	dB/V
Power control range	V_{CTL} = 0.3 to 2.0 V		50			dB
Control voltage range		V_{CTL}	0.3		2.0	V
Control current	P_{in} = 0 to 10 dBm, V_{CTL} = 0 to 2.0 V	I_{CTL}			200	µA

Note: *) with external matching (see application circuit)

Application Circuit



Microstrip line: FR4; Epsilon (r): 4.3; metal Cu: 3.5 µm distance 1. layer – rf ground 0.5 mm
length (mm) × width (mm)
T1: 2.08 × 1 + 2.6 × 0.25
T2: 4.6 × 0.5
T3: 1.5 × 0.25 + 0.93 × 0.2
T4: 11.85 × 1.0
T5: 6.7 × 0.5 + 3.14 × 0.25
T6: 68.06 × 0.5
T7: 1.34 × 0.27 + 5.74 × 1.16
T...*: –> stripline can be reduced to minimum length

Figure 3. Application circuit

PCB Layout

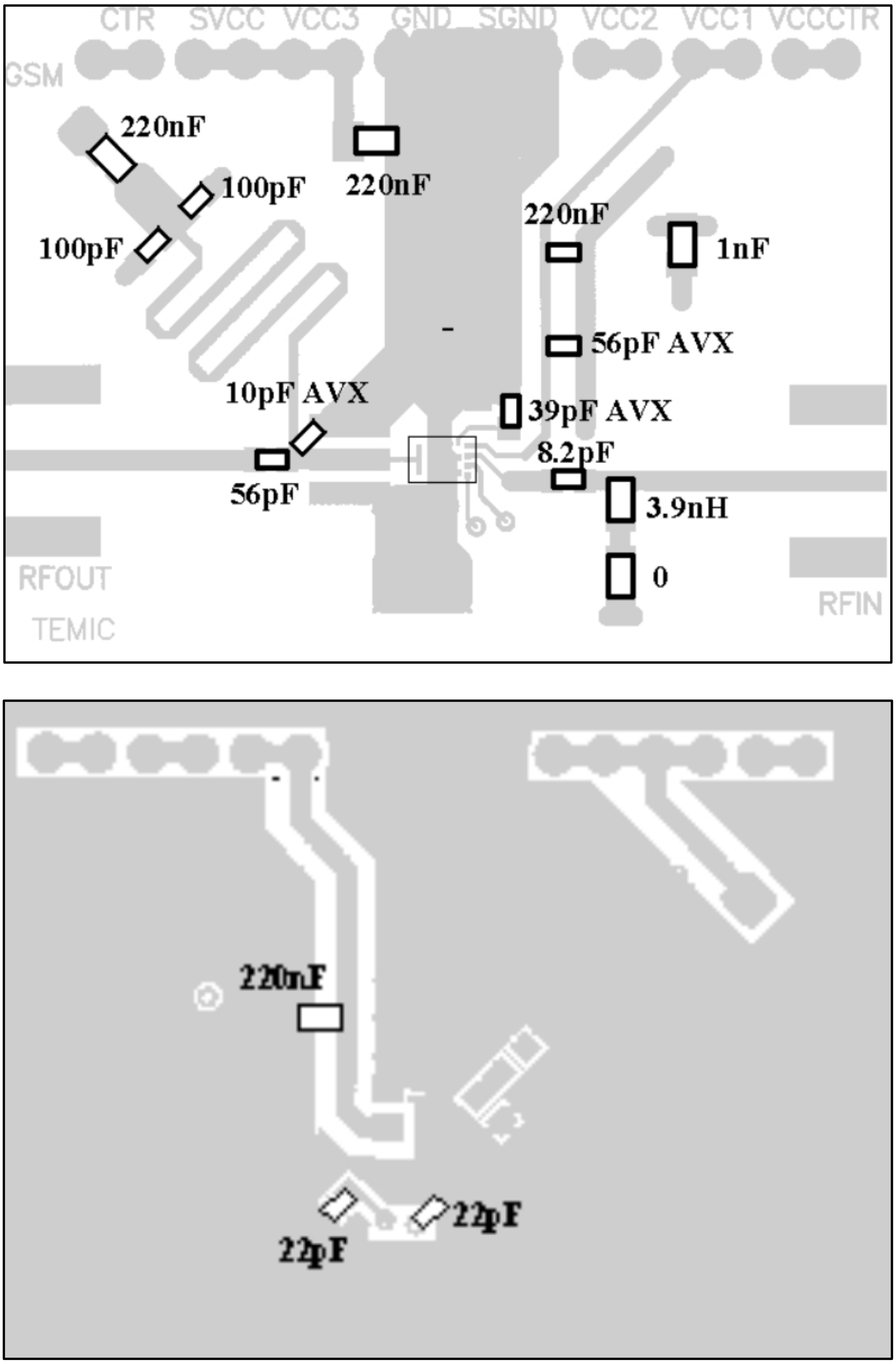
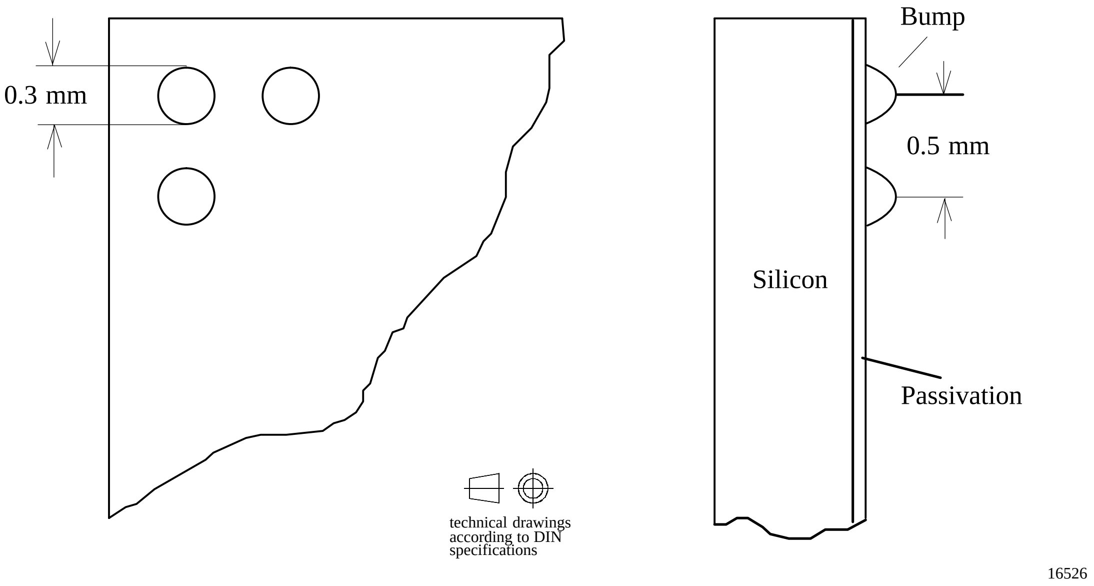


Figure 4. PCB layout

Package Information

Flipchip



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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