ERRATA
TO THE MSP50C6xx USER'S GUIDE

(TEXAS INSTRUMENTS LITERATURE NO. SPSU014, JANUARY 2000)

This document contains corrections and additions to information in the MSP50C6xx User's Guide (TI Literature Number SPSU014, January 2000).

MSP50C6xx User's Guide Text Errors:

1. Page 2–39 of the user's guide, the 5th sentence is: ***Not*** *that the reduced power mode*... This should be: ***Note*** *that the reduced power mode*... (i.e., Not becomes Note)
2. Page 4–24, Table 4.11, Class 4, Subclass C, instruction description should be *Memory references with long constant fields operating on Rx*
3. Page 4–24, Table 4.11, Class 4, Subclass D, instruction description should be *Memory references with R5 operating on Rx*
4. On page 5–27, Section 5.6.5, know should be *known*

MSP50C6xx User's Guide Table and Figure Errors:

Errors	Page(s)	Table(s) or Figure(s)	Correction
INITZ	A–7	Table A–1	RESET
X1	1–11	Table 1–2	OSCIN
	1–12	Figure 1–4	
	7–3	Table 7–1	
	A–7	Table A–1	
	B–8	Table B–1	
	C–6	Table 1	
X2	1–11	Table 1–2	OSCOUT
	1–12	Figure 1–4	
	7–3	Table 7–1	
	A–7	Table A–1	
	C–6	Table 1	
X2 (Pin#13)	B–8	Table B–1	PLL
PLL (Pin#15)	B–8	Table B–1	OSCOUT
NC (Pin#31)	B–8	Table B–1	VCC
GND1 (Pin#48)	B–8	Table B–1	GND2
SCAN_OUT	A–7	Table A–1	SCANOUT
	B–8	Table B–1	
SCAN_IN	B–8	Table B–1	SCANIN
SCAN_CLK	B–8	Table B–1	SCANCLK
PG0	B–4	Figure B–1	Replace Figure B–1 with Figure 1 in this document
OSCIN, OSCOUT	1–10	Table 1–1	Exchange pad numbers (See Table 1 in this document)

FIGURE 1. Revised MSP50C604 Block Diagram

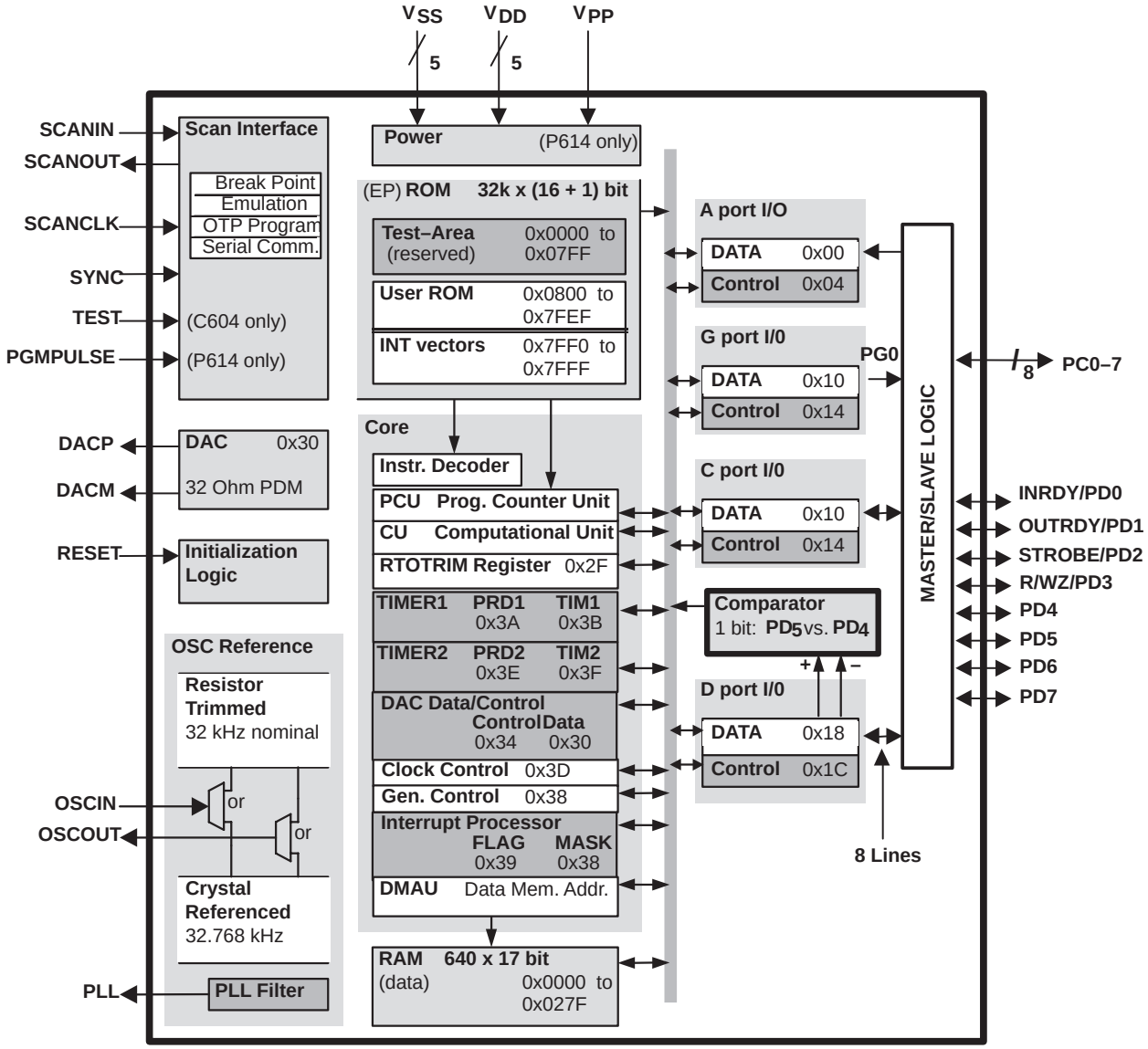

TABLE 1. Revised MSP50C6xx Pad Numbers

SIGNAL	PAD NUMBER	I/O	DESCRIPTION
			Oscillator Reference Signals
OSCOUT	65	O	Resistor/crystal reference out
OSCIN	66	I	Resistor/crystal reference in

Missing Instruction

Add this instruction between pages 4–132 and 4–133.

MULR Multiply (Rounded) With No Data Transfer

Syntax

[label]	***name***	*src*	**Clock**, *clk*	**Word**, *w*	**With RPT**, *clk*	**Class**
	MULR	{adrs}	Table 4–0–46		Table 4–0–46	5

Execution

PH,**PL** ⇐ **MR** * *src*
PC ⇐ **PC** + 1

Flags Affected

TAG bit is set accordingly

Opcode

Instructions	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MULR [adrs]	1	1	0	1	1	1	0	1	0	adrs							
	x	dma16 (for direct) or offset16 (long relative) (see Section 4.13)															

Description

Perform multiplication of multiply register (**MR**) and effective data memory value, add 08x00 to the product. The 16 MSBs of the 32-bit product are stored in the product high (**PH**) register. No status change. Round upper 16 bits.

See Also

MULS, MUL, MULAPL, MULSPL, MULSPLS, MULTPL, MULTPLS, MULAPL

Example

```
MULR *R0++
```

Multiply **MR** with the content of data memory location pointed by **R0** and store the rounded upper 16 bits of the result in **PH**. Increment **R0** by 2.

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