- **Organization:**
  - **TM4SK64KPU . . . 4 194 304 x 64 Bits**
  - **TM8SK64KPU . . . 8 388 608 x 64 Bits**
- **Single 3.3-V Power Supply (±10% Tolerance)**
- **Designed for 66-MHz 4-Clock Systems.**
- **JEDEC 144-Pin Small-Outline Dual-In-Line Memory Module (SODIMM) Without Buffer for Use With Socket**
- **TM4SK64KPU — Uses Four 64M-Bit Synchronous Dynamic RAMs (SDRAMs) (4M × 16-Bit) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM8SK64KPU — Uses Eight 64M-Bit SDRAMs (4M × 16-Bit) in Plastic TSOPs**
- **Byte-Read/Write Capability**
- **Performance Ranges:**

	SYNCHRONOUS CLOCK CYCLE TIME		ACCESS TIME CLOCK TO OUTPUT		REFRESH INTERVAL
	t_{CK3}	t_{CK2}	t_{AC3}	t_{AC2}	t_{REF}
'xSK64KPU–10	10 ns	10 ns	7.5 ns	9 ns	64 ms
'xSK64KPU–12	12 ns	12 ns	8 ns	9.5 ns	

- **High-Speed, Low-Noise Low-Voltage TTL (LVTTL) Interface**
- **Read Latencies 2 and 3 Supported**
- **Support Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, 8, and Full Page**
- **Four Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Pipeline Architecture**
- **Serial Presence-Detect (SPD) Using EEPROM**

PRODUCT PREVIEW

description

The TM4SK64KPU is a 32M-byte, 144-pin small-outline dual-in-line memory module (SODIMM). The SODIMM is composed of four TMS664164DGE, 4194304 x 16-bit SDRAMs, each in a 400-mil, 54-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS664164 data sheet (literature number SMOS690).

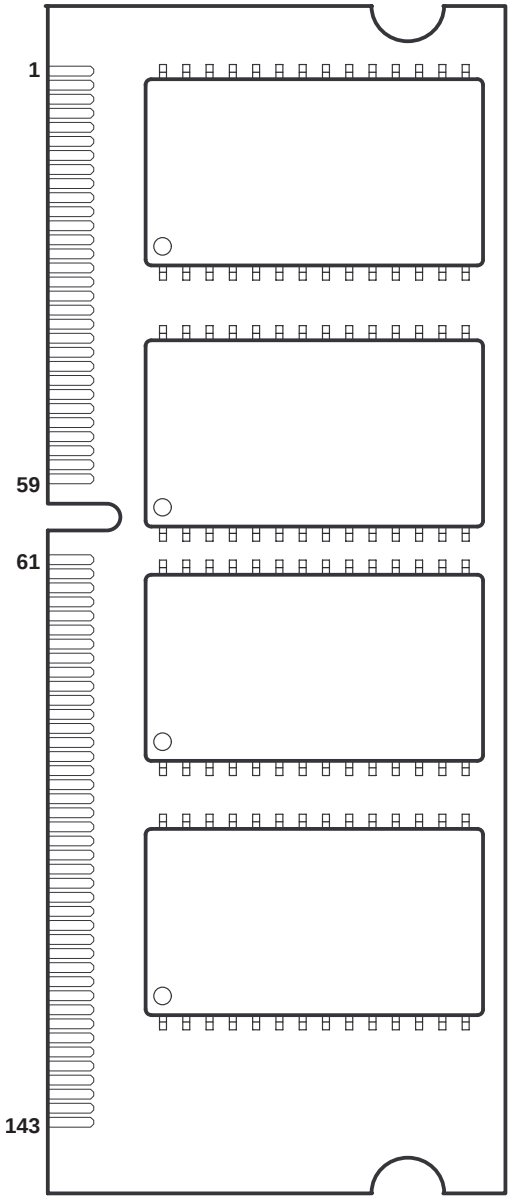
The TM8SK64KPU is a 64M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS664164DGE, 4194304 x 16-bit SDRAMs, each in a 400-mil, 54-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS664164 data sheet (literature number SMOS690).

operation

The TM4SK64KPU operates as four TMS664164DGE devices that are connected as shown in the TM4SK64KPU functional block diagram. The TM8SK64KPU operates as eight TMS664164DGE devices connected as shown in the TM8SK64KPU functional block diagram.

PRODUCT PREVIEW

DUAL-IN-LINE MEMORY MODULE (TOP VIEW)



TM4SK64KPU (SIDE VIEW)

TM8SK64KPU (SIDE VIEW)

PIN NOMENCLATURE

A[0:11]	Row Address Inputs
A[0:7]	Column Address Inputs
A13/BA0	Bank-Select Zero
A12/BA0	Bank-Select One
$\overline{CAS}$	Column-Address Strobe
CKE[0:1]	Clock Enable
CK[0:3]	System Clock
DQ[0:63]	Data-In / Data-Out
DQMB[0:7]	Data-In/Data-Out Mask Enable
$\overline{NC}$	No Connect
$\overline{RAS}$	Row-Address Strobe
$\overline{S}$[0:1]	Chip-Select
SCL	SPD Clock
SDA	SPD Address / Data
V_{DD}	3.3-V Supply
$V_{\overline{SS}}$	Ground
$\overline{WE}$	Write Enable

Pin Assignments

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	V_{SS}	37	DQ8	73	NC	109	A9
2	V_{SS}	38	DQ40	74	CK1	110	A12/BA1
3	DQ0	39	DQ9	75	V_{SS}	111	A10
4	DQ32	40	DQ41	76	V_{SS}	112	A11
5	DQ1	41	DQ10	77	NC	113	V_{DD}
6	DQ33	42	DQ42	78	NC	114	V_{DD}
7	DQ2	43	DQ11	79	NC	115	DQMB2
8	DQ34	44	DQ43	80	NC	116	DQMB6
9	DQ3	45	V_{DD}	81	V_{DD}	117	DQMB3
10	DQ35	46	V_{DD}	82	V_{DD}	118	DQMB7
11	V_{DD}	47	DQ12	83	DQ16	119	V_{SS}
12	V_{DD}	48	DQ44	84	DQ48	120	V_{SS}
13	DQ4	49	DQ13	85	DQ17	121	DQ24
14	DQ36	50	DQ45	86	DQ49	122	DQ56
15	DQ5	51	DQ14	87	DQ18	123	DQ25
16	DQ37	52	DQ46	88	DQ50	124	DQ57
17	DQ6	53	DQ15	89	DQ19	125	DQ26
18	DQ38	54	DQ47	90	DQ51	126	DQ58
19	DQ7	55	V_{SS}	91	V_{SS}	127	DQ27
20	DQ39	56	V_{SS}	92	V_{SS}	128	DQ59
21	V_{SS}	57	NC	93	DQ20	129	V_{DD}
22	V_{SS}	58	NC	94	DQ52	130	V_{DD}
23	DQMB0	59	NC	95	DQ21	131	DQ28
24	DQMB4	60	NC	96	DQ53	132	DQ60
25	DQMB1	61	CK0	97	DQ22	133	DQ29
26	DQMB5	62	CKE0	98	DQ54	134	DQ61
27	V_{DD}	63	V_{DD}	99	DQ23	135	DQ30
28	V_{DD}	64	V_{DD}	100	DQ55	136	DQ62
29	A0	65	$\overline{RAS}$	101	V_{DD}	137	DQ31
30	A3	66	$\overline{CAS}$	102	V_{DD}	138	DQ63
31	A1	67	$\overline{WE}$	103	A6	139	V_{SS}
32	A4	68	CKE1	104	A7	140	V_{SS}
33	A2	69	$\overline{S0}$	105	A8	141	SDA
34	A5	70	NC	106	A13/BA0	142	SCL
35	V_{SS}	71	$\overline{S1}$	107	V_{SS}	143	V_{DD}
36	V_{SS}	72	NC	108	V_{SS}	144	V_{DD}

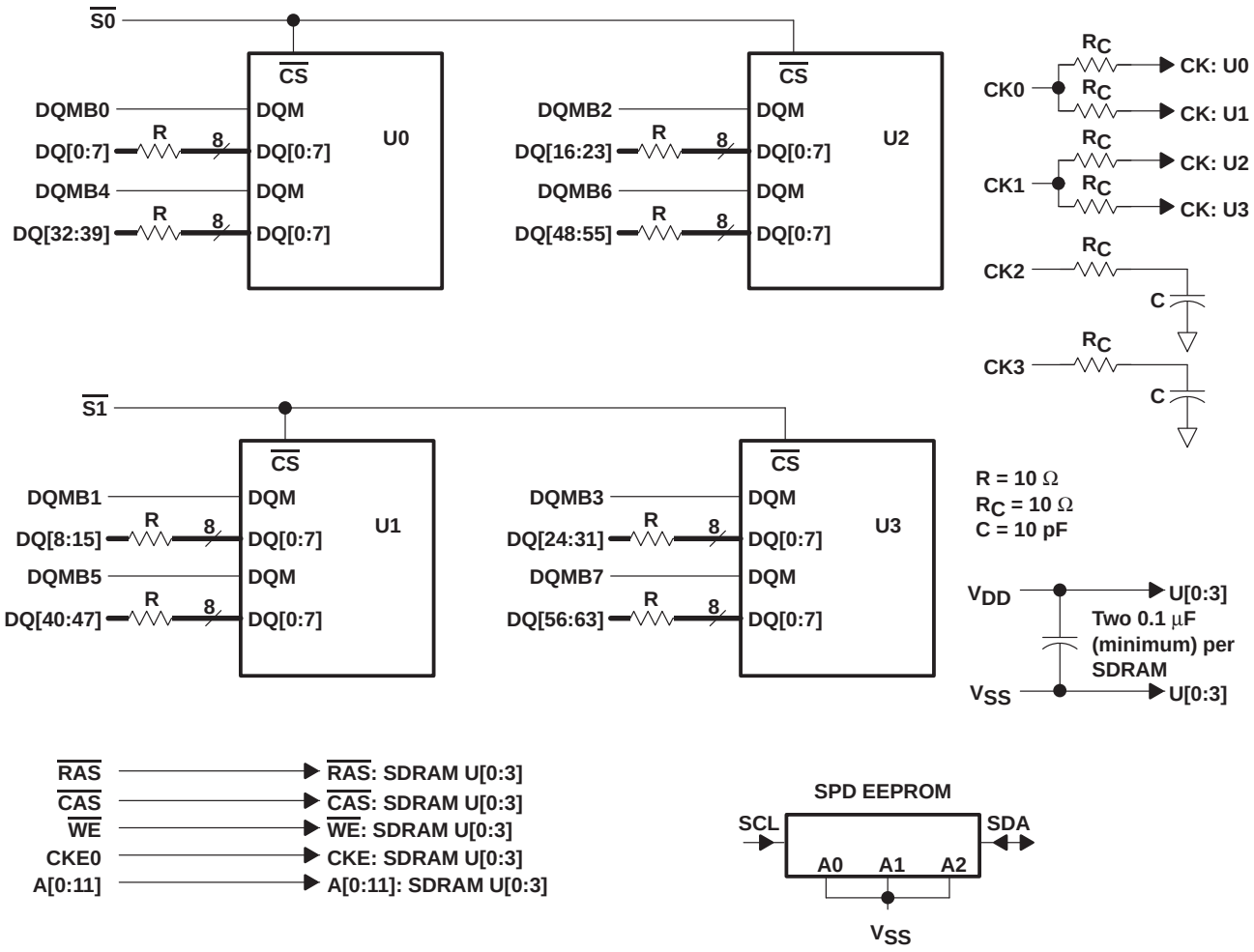
PRODUCT PREVIEW

small-outline dual-in-line memory module and components

The small-outline dual-in-line memory module and components include:

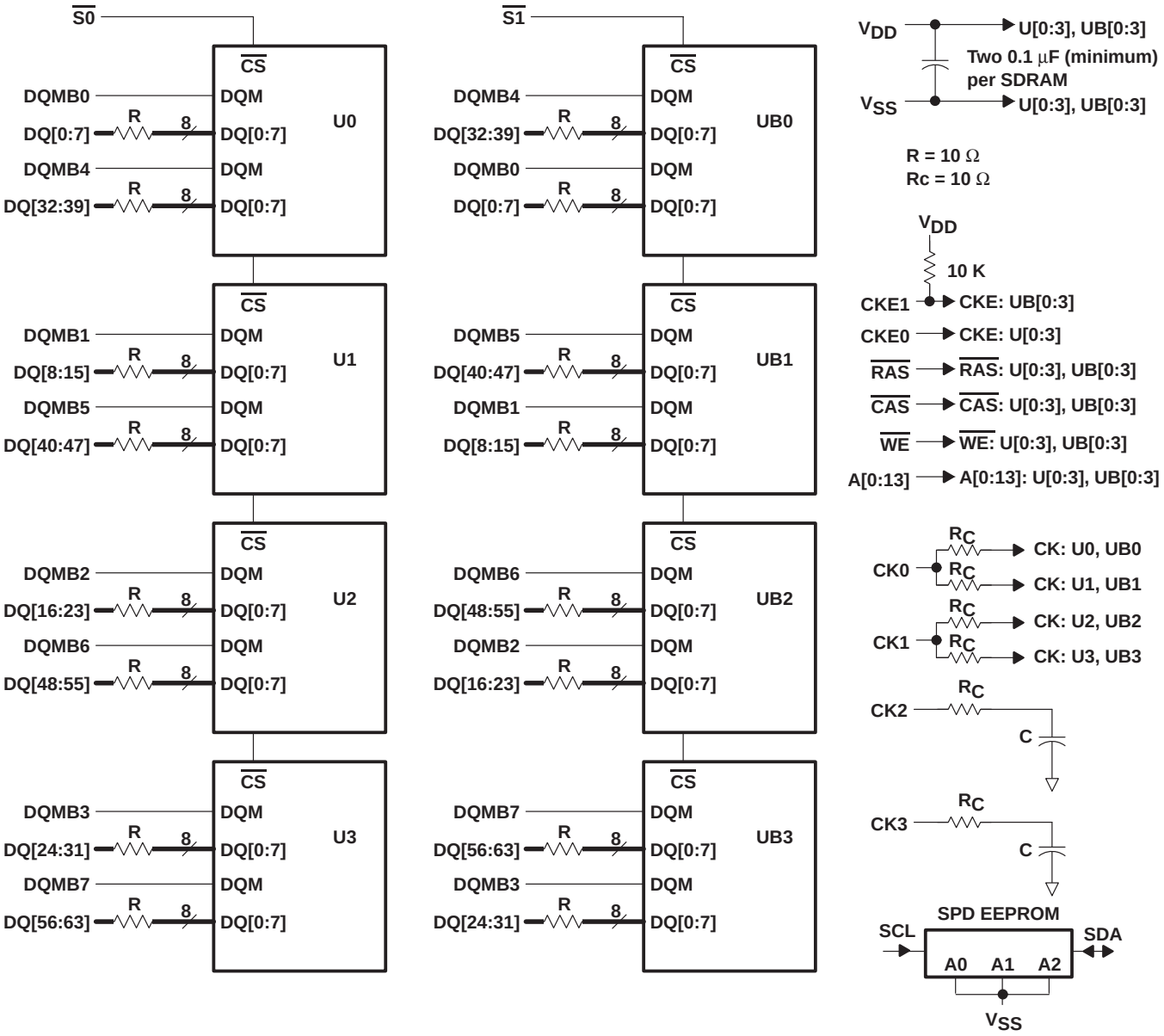
- PC substrate: 1,10 ± 0,1 mm (0.04 inch) nominal thickness
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM4SK64KPU



LEGEND: $\overline{CS}$ = Chip select
SPD = Serial Presence Detect

functional block diagram for the TM8SK64KPU



PRODUCT PREVIEW

absolute maximum ratings over ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 4.6 V
Voltage range on any pin (see Note 1) . . . . . – 0.5 V to 4.6 V
Short-circuit output current . . . . . 50 mA
Power dissipation: TM4SK64KPU . . . . . 4 W
TM8SK64KPU . . . . . 8 W
Ambient temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2		V_{DD} + 0.3	V
V_{IH-SPD}	High-level input voltage for the SPD device	2		5.5	V
V_{IL}	Low-level input voltage	–0.3		0.8	V
T_A	Ambient temperature	0		70	°C

capacitance over recommended ranges of supply voltage and ambient temperature, f = 1 MHz (see Note 2)

PARAMETER		TM4SK64KPU		TM8SK64KPU		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(CK)}$	Input capacitance, CK input		12		22	pF
$C_{i(AC)}$	Input capacitance, address and control inputs: A0–A13, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		22		42	pF
$C_{i(CKE)}$	Input capacitance, CKE input		22		22	pF
C_o	Output capacitance		10		16	pF
$C_{i(DQMBx)}$	Input capacitance, DQMBx input		7		12	pF
$C_{i(Sx)}$	Input capacitance, $\overline{Sx}$ input		22		22	pF
$C_{i/o(SDA)}$	Input/output capacitance, SDA input		9		9	pF
$C_{i(SPD)}$	Input capacitance, SPD inputs (except SDA)		7		7	pF

NOTE 2: V_{DD} = 3.3 V ± 0.3 V. Bias on pins under test is 0 V.

electrical characteristics over recommended ranges of supply voltage and ambient (unless otherwise noted) (see Note 3)

TM4SK64KPU

PARAMETER		TEST CONDITIONS		'4SK64KPU-10 MIN	'4SK64KPU-10 MAX	'4SK64KPU-12 MIN	'4SK64KPU-12 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±10		±10	µA
I_O	Output current (leakage)	0 V < V_O < V_{DD} +0.3 V, Output disabled			±10		±10	µA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN, I_{OH}/I_{OL} = 0 mA, (see Notes 4, 5, and 6)	CAS latency = 2		480		460	mA
			CAS latency = 3		540		480	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 7)			8		8	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 8)			8		8	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 7)			160		160	mA
I_{CC2NS}		t_{CK} = ∞ (see Note 8)			12		12	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Notes 4 and 7)			40		80	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Notes 4 and 8)			80		80	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Notes 4 and 7)			560		520	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Notes 4 and 8)			160		160	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Notes 9 and 10)	CAS latency = 2		1000		960	mA
			CAS latency = 3		1480		1240	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN (see Notes 5 and 8)	CAS latency = 2		1320		1280	mA
			CAS latency = 3		1560		1280	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			16		16	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Only one bank is activated.
5. $t_{RC} \geq$ MIN
6. Control and address inputs change state twice during t_{RC}.
7. Control and address inputs change state once every 30 ns.
8. Control and address inputs do not change state (stable).
9. Control and address inputs change once every cycle.
10. Continuous burst access, n_{CCD} = 1 cycle

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)

TM8SK64KPU

PARAMETER		TEST CONDITIONS		'8SK64KPU-10 MIN	'8SK64KPU-10 MAX	'8SK64KPU-12 MIN	'8SK64KPU-12 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 2 mA		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4	V
I_I	Input current (leakage)	0 V < V_I < V_{DD} + 0.3 V, All other pins = 0 V to V_{DD}			±10		±10	µA
I_O	Output current (leakage)	0 V < V_O < V_{DD} +0.3 V, Output disabled			±10		±10	µA
I_{CC1}	Operating current	Burst length = 1, $t_{RC} \geq t_{RC}$ MIN, I_{OH}/I_{OL} = 0 mA, (see Notes 4, 5, and 6)	CAS latency = 2		488		468	mA
			CAS latency = 3		588		488	mA
I_{CC2P}	Precharge standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Note 7)			16		16	mA
I_{CC2PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 8)			16		16	mA
I_{CC2N}	Precharge standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Note 7)			320		320	mA
I_{CC2NS}		t_{CK} = ∞ (see Note 8)			24		24	mA
I_{CC3P}	Active standby current in power-down mode	CKE ≤ V_{IL} MAX, t_{CK} = 15 ns (see Notes 4 and 7)			80		80	mA
I_{CC3PS}		CKE and CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Notes 4 and 8)			80		80	mA
I_{CC3N}	Active standby current in non-power-down mode	CKE ≥ V_{IH} MIN, t_{CK} = 15 ns (see Notes 4 and 7)			560		520	mA
I_{CC3NS}		CKE ≥ V_{IH} MIN, CK ≤ V_{IL} MAX, t_{CK} = ∞ (see Note 4 and 8)			160		160	mA
I_{CC4}	Burst current	Page burst, I_{OH}/I_{OL} = 0 mA All banks activated, n_{CCD} = one cycle (see Notes 9 and 10)	CAS latency = 2		588		568	mA
			CAS latency = 3		868		728	mA
I_{CC5}	Auto-refresh current	$t_{RC} \leq t_{RC}$ MIN (see Notes 5 and 8)	CAS latency = 2		668		648	mA
			CAS latency = 3		788		648	mA
I_{CC6}	Self-refresh current	CKE ≤ V_{IL} MAX			16		16	mA

NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Only one bank is activated.
5. $t_{RC} \geq$ MIN
6. Control and address inputs change state twice during t_{RC}.
7. Control and address inputs change state once every 30 ns.
8. Control and address inputs do not change state (stable).
9. Control and address inputs change once every cycle.
10. Continuous burst access, n_{CCD} = 1 cycle

ac timing requirements †

			'xSK64KPU-10		'xSK64KPU-12		UNIT
			MIN	MAX	MIN	MAX	
t_{CK2}	Cycle time, CK	CAS latency = 2	15		15		ns
t_{CK3}	Cycle time, CK	CAS latency = 3	10		12		ns
t_{CH}	Pulse duration, CK high		3		4		ns
t_{CL}	Pulse duraction, CK low		3		4		ns
t_{AC2}	Access time, CK high to data out (see Note 11)	CAS latency = 2		9		9.5	ns
t_{AC3}	Access time, CK high to data out (see Note 11)	CAS latency = 3		7.5		8	ns
t_{OH}	Hold time, CK high to data out		3		3		ns
t_{LZ}	Delay time, CK high to DQ in low–impedance state (see Note 12)		2		2		ns
t_{HZ}	Delay time, CK high to DQ in high–impedance state (see Note 13)			8		8	ns
t_{IS}	Setup time, address, control, and data input		3		3		ns
t_{IH}	Hold time, address, control, and data input		1		1		ns
t_{CESP}	Power down/self–refresh exit time		10		12		ns
t_{RAS}	Delay time, ACTV command to DEAC or DCAB command		50		60		ns
t_{RC}	Delay time, ACTV,MRS,REFR,or SLFR to ACTV,MRS,REFR,or SLFR command		80		90		ns
t_{RCD}	Delay time ACTV command to READ,READ–P,WRT,or WRT–P command (see Note 14)		30		30		ns
t_{RP}	Delay time, DEAC or DCAB command to ACTV,MRS,REFR, or SLFR command		30		30		ns
t_{RRD}	Delay time,ACTV command in one bank to ACTV command in the other bank		20		24		ns
t_{RSA}	Delay time,MRS command to ACTV,MRS,REFR,or SLFR command		20		24		ns
t_{APR}	Final data out of READ–P operation to ACTV,MRS,SLFR,or REFR command		$t_{RP} – (CL–1)* t_{CK}$				ns
t_{APW}	Final data in of WRT–P operation to ACTV,MRS,SLFR,or REFR command		$t_{RP} + 1\ t_{CK}$				ns
t_{WR}	Delay time, final data in of WRT operation to DEAC or DCAB command		10		12		ns
t_T	Transition time		1	5	1	5	ms

† All references are made to the rising transition of CK unless otherwise noted.

NOTES: 11. t_{AC} is referenced from the rising transition of CK that precedes the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CK that is read latency (one cycle after the READ command). Access time is measured at output reference level 1.4 V.

12. t_{LZ} is measured from the rising transition of CK that is read latency (one cycle after the READ command).
13. t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
14. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

PRODUCT PREVIEW

clock timing requirements†

			'xSK64KPU-10		'xSK64KPU-12		UNIT‡
			MIN	MAX	MIN	MAX	
t_{REF}	Refresh interval			64		64	ms
n_{CCD}	Delay time, READ or WRT command to an interrupting command		1		1		cycles
n_{CDD}	Delay time, CS low or high to input enabled or inhibited		0	0	0	0	cycles
n_{CLE}	Delay time, CKE high or low to CLK enabled or disabled		1	1	1	1	cycles
n_{CWL}	Delay time, final data in of WRT operation to READ, READ-P, WRT, or WRT-P		1		1		cycles
n_{DID}	Delay time, ENBL or MASK command to enabled or masked data in		0	0	0	0	cycles
n_{DOD}	Delay time, ENBL or MASK command to enabled or masked data out		2	2	2	2	cycles
n_{HZP2}	Delay time, DEAC or DCAB, command to DQ in high–impedance state	CAS latency = 2		2		2	cycles
n_{HZP3}	Delay time, DEAC or DCAB, command to DQ in high–impedance state	CAS latency = 3		3		3	cycles
n_{WCD}	Delay time, WRT command to first data in		0	0	0	0	cycles

† All references are made to the rising transition of CK unless otherwise noted.
‡ A CK cycle can be considered as contributing to a timing requirement for those parameters defined in cycle units only when not gated by CKE (those CK cycles occurring during the time when CKE is asserted low).

PRODUCT PREVIEW

serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follow:

Table 1—TM4SK64KPU. Table 2—TM8SK64KPU.

Table 1. Serial-Presence-Detect Data for the TM4SK64KPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SK64KPU-10		TM4SK64KPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	8	08h	8	08h
5	Number of module banks on this assembly	1 bank	01h	1 bank	01h
6	Data width of this assembly	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 10 ns	A0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 7.5 ns	75h	t_{AC} = 8 ns	80h
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8, full page	8Fh	1, 2, 4, 8, full page	8Fh
17	Number of banks on each SDRAM device	4 banks	04h	4 banks	04h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (±10%), Burst read/write, precharge all, auto precharge	0Eh	V_{DD} tolerance = (±10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	t_{CK} = 15 ns	F0h	t_{CK} = 15 ns	F0h

PRODUCT PREVIEW

serial presence detect (continued)

Table 1. Serial-Presence-Detect Data for the TM4SK64KPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM4SK64KPU-10		TM4SK64KPU-12	
		ITEM	DATA	ITEM	DATA
24	Maximum data-access time from clock at CL = X – 1	t_{AC} = 9 ns	90h	t_{AC} = 9.5ns	95h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 30 ns	1Eh
28	Minimum row-active to row-active delay	t_{RRD} = 20 ns	14h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{\text{RAS}}$x-to-$\overline{\text{CAS}}$x delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{\text{RAS}}$x pulse width	t_{RAS} = 50 ns	32h	t_{RAS} = 60 ns	3Ch
31	Density of each bank on module	32M Bytes	08h	32M Bytes	08h
32 – 61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0 – 62	60	3Ch	122	7Ah
64 – 71	Manufacturer's JEDEC ID code per JEP – 106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73 – 90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93 – 94	Manufacturing date†	TBD		TBD	
95 – 98	Assembly serial number†	TBD		TBD	
99 – 125	Manufacturer specific data†	TBD		TBD	
126 – 127	Vendor specific data†	TBD		TBD	
128–166	System integrator's specific data‡	TBD		TBD	
167–255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 2. Serial-Presence-Detect Data for the TM8SK64KPU

BYTE NO.	DESCRIPTION OF FUNCTION	TM8SK64KPU-10		TM8SK64KPU-12	
		ITEM	DATA	ITEM	DATA
0	Defines number of bytes written into serial memory during module manufacturing	128 bytes	80h	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h	256 bytes	08h
2	Fundamental memory type (FPM, EDO, SDRAM, . . .)	SDRAM	04h	SDRAM	04h
3	Number of row addresses on this assembly	12	0Ch	12	0Ch
4	Number of column addresses on this assembly	8	08h	8	08h
5	Number of module banks on this assembly	2 banks	02h	2 banks	02h
6	Data width of this assembly	64 bits	40h	64 bits	40h
7	Data width continuation		00h		00h
8	Voltage interface standard of this assembly	LVTTL	01h	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL = X	t_{CK} = 10 ns	A0h	t_{CK} = 12 ns	C0h
10	SDRAM access from clock at CL = X	t_{AC} = 7.5 ns	75h	t_{AC} = 8 ns	80h
11	SODIMM configuration type (non-parity, parity, error correcting code [ECC])	Non-Parity	00h	Non-Parity	00h
12	Refresh rate/type	15.6 µs/ self-refresh	80h	15.6 µs/ self-refresh	80h
13	SDRAM width, primary DRAM	x16	10h	x16	10h
14	Error-checking SDRAM data width	N/A	00h	N/A	00h
15	Minimum clock delay, back-to-back random column addresses	1 CK cycle	01h	1 CK cycle	01h
16	Burst lengths supported	1, 2, 4, 8, full page	8Fh	1, 2, 4, 8, full page	8Fh
17	Number of banks on each SDRAM device	4 banks	04h	4 banks	04h
18	CAS latencies supported	2, 3	06h	2, 3	06h
19	CS latency	0	01h	0	01h
20	Write latency	0	01h	0	01h
21	SDRAM module attributes	Non-buffered/ Non-registered	00h	Non-buffered/ Non-registered	00h
22	SDRAM device attributes: general	V_{DD} tolerance = (±10%), Burst read/write, precharge all, auto precharge	0Eh	V_{DD} tolerance = (±10%), Burst read/write, precharge all, auto precharge	0Eh
23	Minimum clock cycle time at CL = X – 1	t_{CK} = 15 ns	F0h	t_{CK} = 15 ns	F0h
24	Maximum data-access time from clock at CL = X – 1	t_{AC} = 9 ns	90h	t_{AC} = 9.5 ns	95h
25	Minimum clock cycle time at CL = X – 2	N/A	00h	N/A	00h
26	Maximum data-access time from clock at CL = X – 2	N/A	00h	N/A	00h

PRODUCT PREVIEW

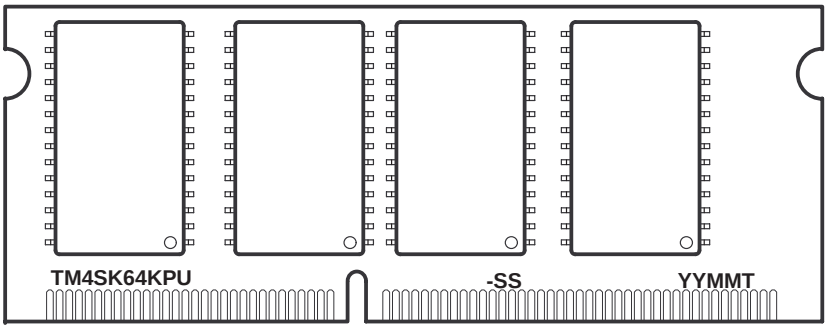
serial presence detect (continued)

Table 2. Serial-Presence-Detect Data for the TM8SK64KPU (Continued)

BYTE NO.	DESCRIPTION OF FUNCTION	TM8SK64KPU-10		TM8SK64KPU-12	
		ITEM	DATA	ITEM	DATA
27	Minimum row precharge time	t_{RP} = 30 ns	1Eh	t_{RP} = 30 ns	1Eh
28	Minimum row-active to row-active delay	t_{RRD} = 20 ns	14h	t_{RRD} = 24 ns	18h
29	Minimum $\overline{RAS}$-to-$\overline{CAS}$ delay	t_{RCD} = 30 ns	1Eh	t_{RCD} = 30 ns	1Eh
30	Minimum $\overline{RAS}$ pulse width	t_{RAS} = 50 ns	32h	t_{RAS} = 60 ns	3Ch
31	Density of each bank on module	32M Bytes	08h	32M Bytes	08h
32–61	Superset features (may be used in the future)				
62	SPD revision	Rev. 1	01h	Rev. 1	01h
63	Checksum for byte 0–62	61	3Dh	123	7Bh
64–71	Manufacturer's JEDEC ID code per JEP–106E	97h	9700...00h	97h	9700...00h
72	Manufacturing location†	TBD		TBD	
73–90	Manufacturer's part number†	TBD		TBD	
91	Die revision code†	TBD		TBD	
92	PCB revision code†	TBD		TBD	
93–94	Manufacturing date†	TBD		TBD	
95–98	Assembly serial number†	TBD		TBD	
99–125	Manufacturer specific data†	TBD		TBD	
126–127	Vendor specific data†	TBD		TBD	
128–166	System integrator's specific data‡	TBD		TBD	
167–255	Open				

† TBD indicates values are determined at manufacturing time and are module dependent.
‡ These TBD values are determined and programmed by the customer (optional).

device symbolization (TM4SK64KPU)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

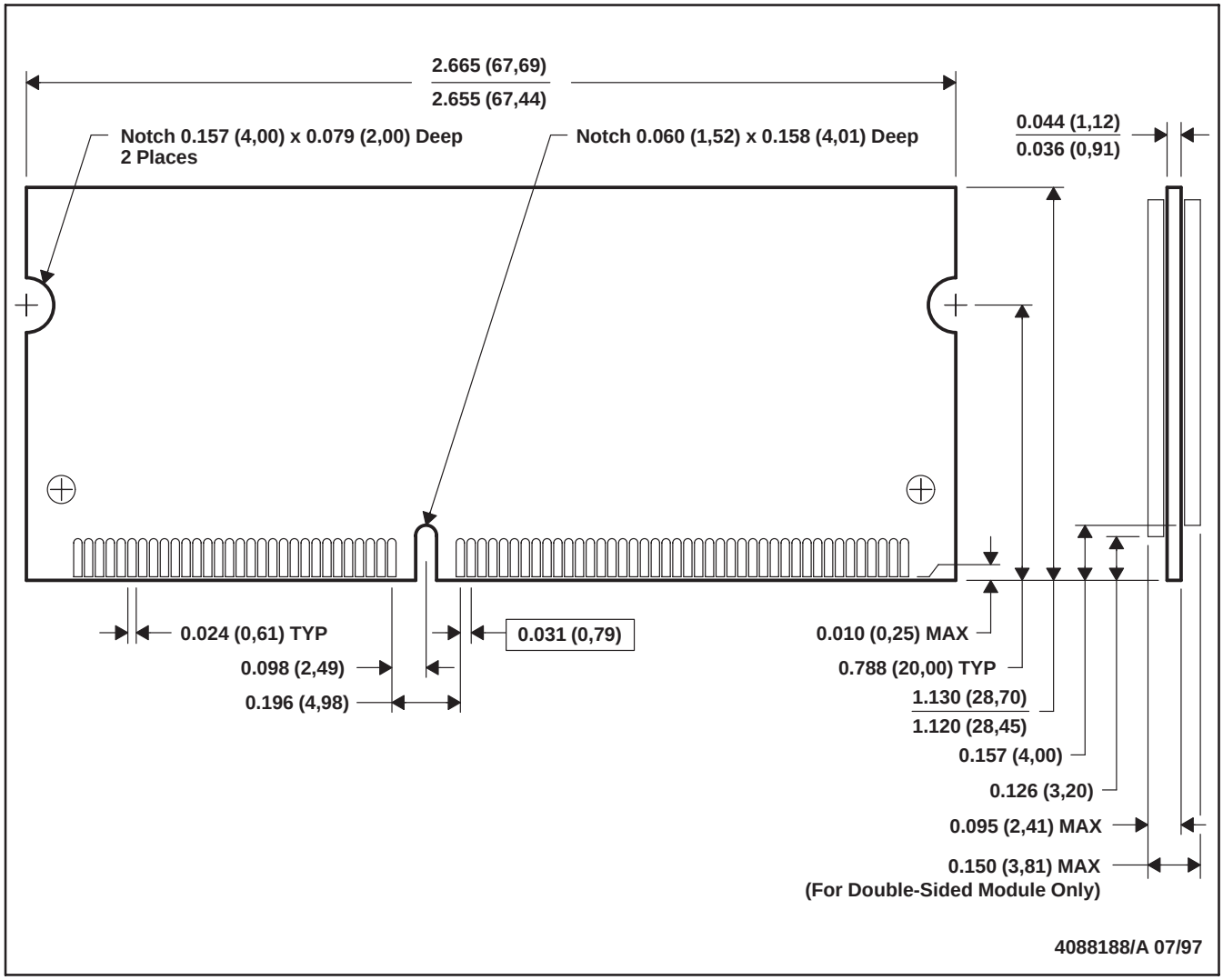
NOTE A: Location of symbolization may vary.

PRODUCT PREVIEW

PRODUCT PREVIEW

MECHANICAL DATA

BDQ (R-SODIMM-N144) **SMALL OUTLINE DUAL IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-190

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