

- **Organization**
  - TM2xJ64xPN-xx . . . 2097152 × 64 Bits
- **Single 3.3-V Power Supply**  
(±10% Tolerance)
- **JEDEC 144-Pin Small Outline Dual-In-Line Memory Module (SODIMM) Without Buffer for Use With Socket**
- **TM2xJ64xPN-xx — Utilizes Eight 16M-Bit (2M×8-Bit) Dynamic RAMs in TSOPs**
- **Performance ranges**

|              | ACCESS<br>TIME          | ACCESS<br>TIME          | ACCESS<br>TIME         | EDO<br>CYCLE            |
|--------------|-------------------------|-------------------------|------------------------|-------------------------|
|              | t <sub>RAC</sub><br>MAX | t <sub>CAC</sub><br>MAX | t <sub>AA</sub><br>MAX | t <sub>HPC</sub><br>MIN |
| '2xJ64xPN-50 | 50 ns                   | 13 ns                   | 25 ns                  | 20 ns                   |
| '2xJ64xPN-60 | 60 ns                   | 15 ns                   | 30 ns                  | 25 ns                   |
| '2xJ64xPN-70 | 70 ns                   | 18 ns                   | 35 ns                  | 30 ns                   |
- **High-Speed, Low-Noise LVTTTL Interface**
- **Long Refresh Period:**
  - TM2EJ64DPN: 32 ms (2048 cycles)
  - TM2EJ64EPN: 64 ms (4096 cycles)
- **Low-Power, Battery-Backup Refresh Available:**
  - TM2FJ64DPN: 128 ms (2048 cycles)
  - TM2FJ64EPN: 128 ms (4096 cycles)
- **3-State Output**
- **Extended-Data-Out (EDO) Operation With CAS-Before-RAS (CBR), RAS-Only, and Hidden Refresh**
- **Serial Presence-Detect (SPD) Using EEPROM**
- **Ambient Temperature Range**  
0°C to 70°C
- **Gold-Plated Contacts**

## description

The TM2EJ64DPN is a 16M-byte, 144-pin, small outline dual-in-line memory module (SODIMM). The SODIMM is composed of eight TMS427809A, 2097152 × 8-bit 2K-refresh EDO dynamic random-access memories (DRAMs), each in a 400-mil, 28-pin plastic thin small-outline package (TSOP) (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS427809A data sheet (literature number SMKS894).

The TM2EJ64EPN is an 16M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS426809A, 2097152 × 8-bit 4K-refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS426809A data sheet (literature number SMKS894).

The TM2FJ64DPN is a 16M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS427809AP, 2097152 × 8-bit 2K low-power battery-backup refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS427809AP data sheet (literature number SMKS894).

The TM2FJ64EPN is a 16M-byte, 144-pin SODIMM. The SODIMM is composed of eight TMS426809AP, 2097152 × 8-bit 4K low-power battery-backup refresh EDO DRAMs, each in a 400-mil, 28-pin plastic TSOP (DGC suffix) mounted on a substrate with decoupling capacitors. See the TMS426809AP data sheet (literature number SMKS894).

## operation

The TM2xJ64xPN operates as eight TMS42x809A/Ps, connected as shown in the functional block diagram.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

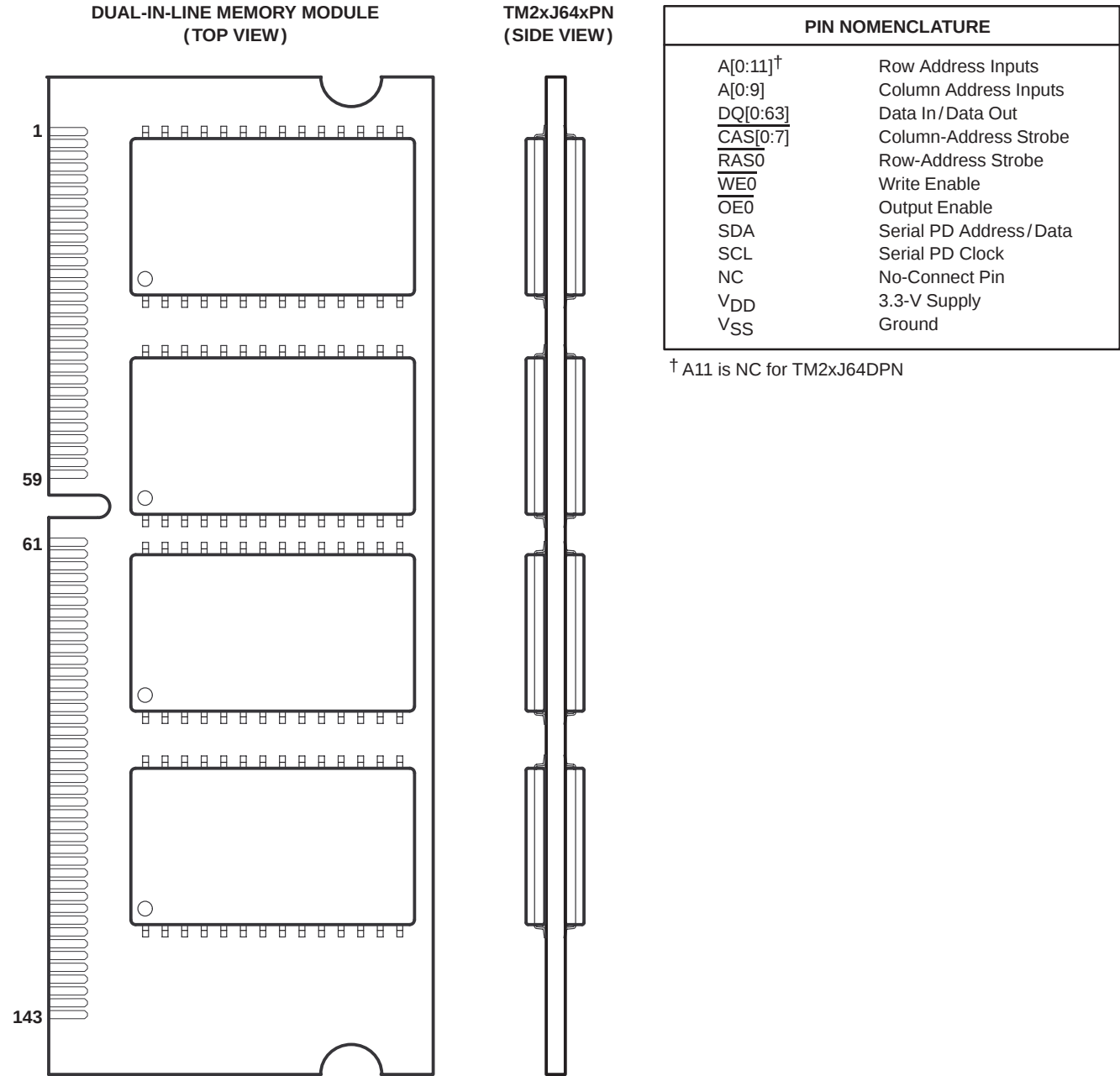


POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

Copyright © 1997, Texas Instruments Incorporated

TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT  
 TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT  
 EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM  
 SMMS685 – AUGUST 1997

PRODUCT PREVIEW



### Pin Assignments

| NO. | PIN<br>NAME              | NO. | PIN<br>NAME              | NO. | PIN<br>NAME            | NO. | PIN<br>NAME              |
|-----|--------------------------|-----|--------------------------|-----|------------------------|-----|--------------------------|
| 1   | V <sub>SS</sub>          | 37  | DQ8                      | 73  | $\overline{\text{OE}}$ | 109 | A9                       |
| 2   | V <sub>SS</sub>          | 38  | DQ40                     | 74  | NC                     | 110 | NC                       |
| 3   | DQ0                      | 39  | DQ9                      | 75  | V <sub>SS</sub>        | 111 | A10                      |
| 4   | DQ32                     | 40  | DQ41                     | 76  | V <sub>SS</sub>        | 112 | NC                       |
| 5   | DQ1                      | 41  | DQ10                     | 77  | NC                     | 113 | V <sub>DD</sub>          |
| 6   | DQ33                     | 42  | DQ42                     | 78  | NC                     | 114 | V <sub>DD</sub>          |
| 7   | DQ2                      | 43  | DQ11                     | 79  | NC                     | 115 | $\overline{\text{CAS2}}$ |
| 8   | DQ34                     | 44  | DQ43                     | 80  | NC                     | 116 | $\overline{\text{CAS6}}$ |
| 9   | DQ3                      | 45  | V <sub>DD</sub>          | 81  | V <sub>DD</sub>        | 117 | $\overline{\text{CAS3}}$ |
| 10  | DQ35                     | 46  | V <sub>DD</sub>          | 82  | V <sub>DD</sub>        | 118 | $\overline{\text{CAS7}}$ |
| 11  | V <sub>DD</sub>          | 47  | DQ12                     | 83  | DQ16                   | 119 | V <sub>SS</sub>          |
| 12  | V <sub>DD</sub>          | 48  | DQ44                     | 84  | DQ48                   | 120 | V <sub>SS</sub>          |
| 13  | DQ4                      | 49  | DQ13                     | 85  | DQ17                   | 121 | DQ24                     |
| 14  | DQ36                     | 50  | DQ45                     | 86  | DQ49                   | 122 | DQ56                     |
| 15  | DQ5                      | 51  | DQ14                     | 87  | DQ18                   | 123 | DQ25                     |
| 16  | DQ37                     | 52  | DQ46                     | 88  | DQ50                   | 124 | DQ57                     |
| 17  | DQ6                      | 53  | DQ15                     | 89  | DQ19                   | 125 | DQ26                     |
| 18  | DQ38                     | 54  | DQ47                     | 90  | DQ51                   | 126 | DQ58                     |
| 19  | DQ7                      | 55  | V <sub>SS</sub>          | 91  | V <sub>SS</sub>        | 127 | DQ27                     |
| 20  | DQ39                     | 56  | V <sub>SS</sub>          | 92  | V <sub>SS</sub>        | 128 | DQ59                     |
| 21  | V <sub>SS</sub>          | 57  | NC                       | 93  | DQ20                   | 129 | V <sub>DD</sub>          |
| 22  | V <sub>SS</sub>          | 58  | NC                       | 94  | DQ52                   | 130 | V <sub>DD</sub>          |
| 23  | $\overline{\text{CAS0}}$ | 59  | NC                       | 95  | DQ21                   | 131 | DQ28                     |
| 24  | $\overline{\text{CAS4}}$ | 60  | NC                       | 96  | DQ53                   | 132 | DQ60                     |
| 25  | $\overline{\text{CAS1}}$ | 61  | NC                       | 97  | DQ22                   | 133 | DQ29                     |
| 26  | $\overline{\text{CAS5}}$ | 62  | NC                       | 98  | DQ54                   | 134 | DQ61                     |
| 27  | V <sub>DD</sub>          | 63  | V <sub>DD</sub>          | 99  | DQ23                   | 135 | DQ30                     |
| 28  | V <sub>DD</sub>          | 64  | V <sub>DD</sub>          | 100 | DQ55                   | 136 | DQ62                     |
| 29  | A0                       | 65  | NC                       | 101 | V <sub>DD</sub>        | 137 | DQ31                     |
| 30  | A3                       | 66  | NC                       | 102 | V <sub>DD</sub>        | 138 | DQ63                     |
| 31  | A1                       | 67  | $\overline{\text{WE0}}$  | 103 | A6                     | 139 | V <sub>SS</sub>          |
| 32  | A4                       | 68  | NC                       | 104 | A7                     | 140 | V <sub>SS</sub>          |
| 33  | A2                       | 69  | $\overline{\text{RAS0}}$ | 105 | A8                     | 141 | SDA                      |
| 34  | A5                       | 70  | NC                       | 106 | A11                    | 142 | SCL                      |
| 35  | V <sub>SS</sub>          | 71  | NC                       | 107 | V <sub>SS</sub>        | 143 | V <sub>DD</sub>          |
| 36  | V <sub>SS</sub>          | 72  | NC                       | 108 | V <sub>SS</sub>        | 144 | V <sub>DD</sub>          |

PRODUCT PREVIEW

# TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM

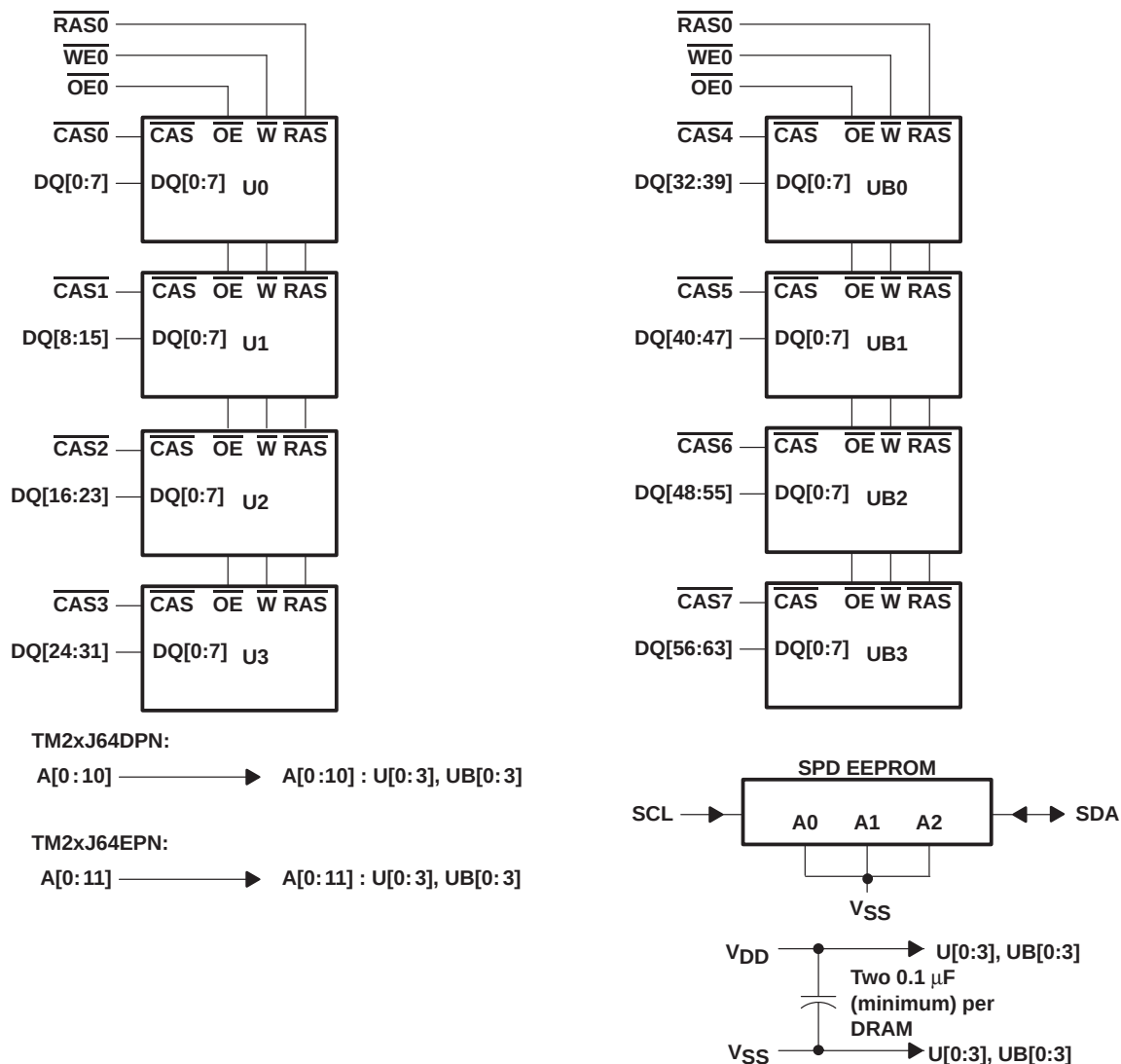
SMMS685 – AUGUST 1997

## small outline dual-in-line memory module and components

The small-outline dual-in-line memory module and components include:

- PC substrate:  $1,10 \pm 0,1$  mm (0.04 inch) nominal thickness
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

## functional block diagram for the TM2xJ64xPN



PRODUCT PREVIEW

**absolute maximum ratings over ambient temperature range (unless otherwise noted)<sup>†</sup>**

|                                       |                  |
|---------------------------------------|------------------|
| Supply voltage range, $V_{DD}$        | –0.5 V to 4.6 V  |
| Voltage range on any pin (see Note 1) | – 0.5 V to 4.6 V |
| Short-circuit output current          | 50 mA            |
| Power dissipation: TM2xP64DPN         | 8 W              |
| TM2xP64EPN                            | 8 W              |
| Ambient temperature range, $T_A$      | 0°C to 70°C      |
| Storage temperature range, $T_{stg}$  | – 55°C to 125°C  |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to  $V_{SS}$ .

**recommended operating conditions**

|                                                          | MIN  | NOM | MAX            | UNIT |
|----------------------------------------------------------|------|-----|----------------|------|
| $V_{DD}$ Supply voltage                                  | 3    | 3.3 | 3.6            | V    |
| $V_{SS}$ Supply voltage                                  |      | 0   |                | V    |
| $V_{IH}$ High-level input voltage                        | 2    |     | $V_{DD} + 0.3$ | V    |
| $V_{IH-SPD}$ High-level input voltage for the SPD device | 2    |     | 5.5            | V    |
| $V_{IL}$ Low-level input voltage                         | –0.3 |     | 0.8            | V    |
| $T_A$ Ambient temperature                                | 0    |     | 70             | °C   |

**capacitance over recommended ranges of supply voltage and ambient temperature,  $f = 1$  MHz (see Note 2)**

| PARAMETER                                                 | '2xJ64xPN |     | UNIT |
|-----------------------------------------------------------|-----------|-----|------|
|                                                           | MIN       | MAX |      |
| $C_{i(A)}$ Input capacitance, A0–A10                      |           | 42  | pF   |
| $C_{i(OE)}$ Input capacitance, $\overline{OE0}$           |           | 58  | pF   |
| $C_{i(CAS)}$ Input capacitance, $\overline{CASx}$         |           | 9   | pF   |
| $C_{i(RAS)}$ Input capacitance, $\overline{RAS0}$         |           | 58  | pF   |
| $C_{i(W)}$ Input capacitance, $\overline{WE0}$            |           | 58  | pF   |
| $C_o$ Output capacitance                                  |           | 9   | pF   |
| $C_{i/o(SDA)}$ Input/output capacitance, SDA input        |           | 9   | pF   |
| $C_{i(SPD)}$ Input capacitance, SA0, SA1, SA2, SCL inputs |           | 7   | pF   |

NOTE 2:  $V_{DD} = \text{NOM supply voltage} \pm 10\%$ , and the bias on pins under test is 0 V.

TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT  
 TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT  
 EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM

SMMS685 – AUGUST 1997

electrical characteristics over recommended ranges of supply voltage and ambient temperature  
 (unless otherwise noted)

TM2EJ64DPN

| PARAMETER                      |                                                   | TEST CONDITIONS <sup>†</sup>                                                                                      |         | '2EJ64DPN-50          |      | '2EJ64DPN-60          |      | '2EJ64DPN-70          |      | UNIT |
|--------------------------------|---------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|---------|-----------------------|------|-----------------------|------|-----------------------|------|------|
|                                |                                                   |                                                                                                                   |         | MIN                   | MAX  | MIN                   | MAX  | MIN                   | MAX  |      |
| V <sub>OH</sub>                | High-level output voltage                         | I <sub>OH</sub> = – 2 mA                                                                                          | LVTTL   | 2.4                   |      | 2.4                   |      | 2.4                   |      | V    |
|                                |                                                   | I <sub>OH</sub> = – 100 µA                                                                                        | LVC MOS | V <sub>DD</sub> – 0.2 |      | V <sub>DD</sub> – 0.2 |      | V <sub>DD</sub> – 0.2 |      |      |
| V <sub>OL</sub>                | Low-level output voltage                          | I <sub>OL</sub> = 2 mA                                                                                            | LVTTL   |                       | 0.4  |                       | 0.4  |                       | 0.4  | V    |
|                                |                                                   | I <sub>OL</sub> = 100 µA                                                                                          | LVC MOS |                       | 0.2  |                       | 0.2  |                       | 0.2  |      |
| I <sub>I</sub>                 | Input current (leakage)                           | V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = 0 V to 3.9 V, All others = 0 V to V <sub>DD</sub>                       |         |                       | ± 10 |                       | ± 10 |                       | ± 10 | µA   |
| I <sub>O</sub>                 | Output current (leakage)                          | V <sub>DD</sub> = 3.6 V, V <sub>O</sub> = 0 V to V <sub>DD</sub> , CASx high                                      |         |                       | ± 10 |                       | ± 10 |                       | ± 10 | µA   |
| I <sub>CC1</sub> <sup>‡§</sup> | Read- or write-cycle current                      | V <sub>DD</sub> = 3.6 V, Minimum cycle                                                                            |         |                       | 960  |                       | 800  |                       | 720  | mA   |
| I <sub>CC2</sub>               | Standby current                                   | V <sub>IH</sub> = 2 V (LVTTL), After one memory cycle, RAS0 and CASx high                                         |         |                       | 16   |                       | 16   |                       | 16   | mA   |
|                                |                                                   | V <sub>IH</sub> = V <sub>DD</sub> – 0.2 V (LVC MOS), After one memory cycle, RAS0 and CASx high                   |         |                       | 8    |                       | 8    |                       | 8    |      |
| I <sub>CC3</sub> <sup>‡§</sup> | Average refresh current (RAS-only refresh or CBR) | V <sub>DD</sub> = 3.6 V, Minimum cycle, RAS0 cycling, CASx high (RAS-only refresh), RAS0 low after CASx low (CBR) |         |                       | 960  |                       | 800  |                       | 720  | mA   |
| I <sub>CC4</sub> <sup>‡¶</sup> | Average EDO current                               | V <sub>DD</sub> = 3.6 V, RAS0 low, t <sub>HPC</sub> = MIN, CASx cycling                                           |         |                       | 880  |                       | 720  |                       | 640  | mA   |

<sup>†</sup> For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

<sup>‡</sup> Measured with outputs open

<sup>§</sup> Measured with a maximum of one address change while  $\overline{\text{RAS0}} = V_{IL}$

<sup>¶</sup> Measured with a maximum of one address change during each EDO cycle, t<sub>HPC</sub>

PRODUCT PREVIEW



electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted)

TM2EJ64EPN

| PARAMETER           |                                                   | TEST CONDITIONS†                                                                                                  |         | '2EJ64EPN-50          |      | '2EJ64EPN-60          |      | '2EJ64EPN-70          |      | UNIT |
|---------------------|---------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|---------|-----------------------|------|-----------------------|------|-----------------------|------|------|
|                     |                                                   |                                                                                                                   |         | MIN                   | MAX  | MIN                   | MAX  | MIN                   | MAX  |      |
| V <sub>OH</sub>     | High-level output voltage                         | I <sub>OH</sub> = – 2 mA                                                                                          | LVTTL   | 2.4                   |      | 2.4                   |      | 2.4                   |      | V    |
|                     |                                                   | I <sub>OH</sub> = – 100 µA                                                                                        | LVC MOS | V <sub>DD</sub> – 0.2 |      | V <sub>DD</sub> – 0.2 |      | V <sub>DD</sub> – 0.2 |      |      |
| V <sub>OL</sub>     | Low-level output voltage                          | I <sub>OL</sub> = 2 mA                                                                                            | LVTTL   |                       | 0.4  |                       | 0.4  |                       | 0.4  | V    |
|                     |                                                   | I <sub>OL</sub> = 100 µA                                                                                          | LVC MOS |                       | 0.2  |                       | 0.2  |                       | 0.2  |      |
| I <sub>I</sub>      | Input current (leakage)                           | V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = 0 V to 3.9 V, All others = 0 V to V <sub>DD</sub>                       |         |                       | ± 10 |                       | ± 10 |                       | ± 10 | µA   |
| I <sub>O</sub>      | Output current (leakage)                          | V <sub>DD</sub> = 3.6 V, V <sub>O</sub> = 0 V to V <sub>DD</sub> , CASx high                                      |         |                       | ± 10 |                       | ± 10 |                       | ± 10 | µA   |
| I <sub>CC1</sub> ‡§ | Read- or write-cycle current                      | V <sub>DD</sub> = 3.6 V, Minimum cycle                                                                            |         |                       | 720  |                       | 560  |                       | 480  | mA   |
| I <sub>CC2</sub>    | Standby current                                   | V <sub>IH</sub> = 2 V (LVTTL), After one memory cycle, RAS0 and CASx high                                         |         |                       | 16   |                       | 16   |                       | 16   | mA   |
|                     |                                                   | V <sub>IH</sub> = V <sub>DD</sub> – 0.2 V (LVC MOS), After one memory cycle, RAS0 and CASx high                   |         |                       | 8    |                       | 8    |                       | 8    | mA   |
| I <sub>CC3</sub> ‡§ | Average refresh current (RAS-only refresh or CBR) | V <sub>DD</sub> = 3.6 V, Minimum cycle, RASx cycling, CASx high (RAS-only refresh), RAS0 low after CASx low (CBR) |         |                       | 720  |                       | 560  |                       | 480  | mA   |
| I <sub>CC4</sub> ‡¶ | Average EDO current                               | V <sub>DD</sub> = 3.6 V, RAS0 low, t <sub>HPC</sub> = MIN, CASx cycling                                           |         |                       | 800  |                       | 720  |                       | 640  | mA   |

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while RAS0 = V<sub>IL</sub>

¶ Measured with a maximum of one address change during each EDO cycle, t<sub>HPC</sub>

PRODUCT PREVIEW

TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT  
 TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT  
 EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM

SMMS685 – AUGUST 1997

electrical characteristics over recommended ranges of supply voltage and ambient temperature  
 (unless otherwise noted) (continued)

TM2FJ64DPN

| PARAMETER           |                                                                                         | TEST CONDITIONS†                                                                                                                                                                                 |         | '2FJ64DPN-50          |      | '2FJ64DPN-60          |      | '2FJ64DPN-70          |      | UNIT |
|---------------------|-----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------------|------|-----------------------|------|-----------------------|------|------|
|                     |                                                                                         |                                                                                                                                                                                                  |         | MIN                   | MAX  | MIN                   | MAX  | MIN                   | MAX  |      |
| V <sub>OH</sub>     | High-level output voltage                                                               | I <sub>OH</sub> = – 2 mA                                                                                                                                                                         | LVTTL   | 2.4                   |      | 2.4                   |      | 2.4                   |      | V    |
|                     |                                                                                         | I <sub>OH</sub> = – 100 µA                                                                                                                                                                       | LVC MOS | V <sub>DD</sub> – 0.2 |      | V <sub>DD</sub> – 0.2 |      | V <sub>DD</sub> – 0.2 |      |      |
| V <sub>OL</sub>     | Low-level output voltage                                                                | I <sub>OL</sub> = 2 mA                                                                                                                                                                           | LVTTL   |                       | 0.4  |                       | 0.4  |                       | 0.4  | V    |
|                     |                                                                                         | I <sub>OL</sub> = 100 µA                                                                                                                                                                         | LVC MOS |                       | 0.2  |                       | 0.2  |                       | 0.2  |      |
| I <sub>I</sub>      | Input current (leakage)                                                                 | V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = 0 V to 3.9 V, All others = 0 V to V <sub>DD</sub>                                                                                                      |         |                       | ± 10 |                       | ± 10 |                       | ± 10 | µA   |
| I <sub>O</sub>      | Output current (leakage)                                                                | V <sub>DD</sub> = 3.6 V, V <sub>O</sub> = 0 V to V <sub>DD</sub> , CASx high                                                                                                                     |         |                       | ± 10 |                       | ± 10 |                       | ± 10 | µA   |
| I <sub>CC1</sub> ‡§ | Read- or write-cycle current                                                            | V <sub>DD</sub> = 3.6 V, Minimum cycle                                                                                                                                                           |         |                       | 960  |                       | 800  |                       | 720  | mA   |
| I <sub>CC2</sub>    | Standby current                                                                         | V <sub>IH</sub> = 2 V (LVTTL), After one memory cycle, RAS0 and CASx high                                                                                                                        |         |                       | 8    |                       | 8    |                       | 8    | mA   |
|                     |                                                                                         | V <sub>IH</sub> = V <sub>DD</sub> – 0.2 V (LVC MOS), After one memory cycle, RAS0 and CASx high                                                                                                  |         |                       | 1.2  |                       | 1.2  |                       | 1.2  | mA   |
| I <sub>CC3</sub> ‡§ | Average refresh current (RAS-only refresh or CBR)                                       | V <sub>DD</sub> = 3.6 V, Minimum cycle, RAS0 cycling, CASx high (RAS-only refresh), RAS0 low after CASx low (CBR)                                                                                |         |                       | 960  |                       | 800  |                       | 720  | mA   |
| I <sub>CC4</sub> ‡¶ | Average EDO current                                                                     | V <sub>DD</sub> = 3.6 V, RAS0 low, t <sub>HPC</sub> = MIN, CASx cycling                                                                                                                          |         |                       | 880  |                       | 720  |                       | 640  | mA   |
| I <sub>CC6</sub>    | Average self-refresh current                                                            | CASx < 0.2 V, RAS0 < 0.2 V, Measured after t <sub>RASS</sub> min                                                                                                                                 |         |                       | 1.6  |                       | 1.6  |                       | 1.6  | mA   |
| I <sub>CC10</sub>   | Average battery back-up operating current (equivalent refresh time is 128 ms), CBR only | t <sub>RC</sub> = 31.25 µs, t <sub>RAS</sub> ≤ 300 ns, V <sub>DD</sub> – 0.2 V ≤ V <sub>IH</sub> ≤ 3.9 V, 0 V ≤ V <sub>IL</sub> ≤ 0.2 V, WE0 and OE0 = V <sub>IH</sub> , Address and data stable |         |                       | 2.8  |                       | 2.8  |                       | 2.8  | mA   |

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

‡ Measured with outputs open

§ Measured with a maximum of one address change while RAS0 = V<sub>IL</sub>

¶ Measured with a maximum of one address change during each EDO cycle, t<sub>HPC</sub>

**electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (continued)**

**TM2FJ64EPN**

| PARAMETER |                                                                                         | TEST CONDITIONS†                                                                                                       |        | '2FJ64EPN-50 |     | '2FJ64EPN-60 |     | '2FJ64EPN-70 |     | UNIT |
|-----------|-----------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|--------|--------------|-----|--------------|-----|--------------|-----|------|
|           |                                                                                         |                                                                                                                        |        | MIN          | MAX | MIN          | MAX | MIN          | MAX |      |
| VOH       | High-level output voltage                                                               | IOH = − 2 mA                                                                                                           | LVTTL  | 2.4          |     | 2.4          |     | 2.4          |     | V    |
|           |                                                                                         | IOH = − 100 μA                                                                                                         | LVCMOS | VDD−0.2      |     | VDD−0.2      |     | VDD−0.2      |     |      |
| VOL       | Low-level output voltage                                                                | IOL = 2 mA                                                                                                             | LVTTL  | 0.4          |     | 0.4          |     | 0.4          |     | V    |
|           |                                                                                         | IOL = 100 μA                                                                                                           | LVCMOS | 0.2          |     | 0.2          |     | 0.2          |     |      |
| II        | Input current (leakage)                                                                 | VDD = 3.6 V, VI = 0 V to 3.9 V, All others = 0 V to VDD                                                                |        | ± 10         |     | ± 10         |     | ± 10         |     | μA   |
| IO        | Output current (leakage)                                                                | VDD = 3.6 V, VO = 0 V to VDD, CASx high                                                                                |        | ± 10         |     | ± 10         |     | ± 10         |     | μA   |
| ICC1‡§    | Read- or write-cycle current                                                            | VDD = 3.6 V, Minimum cycle                                                                                             |        | 720          |     | 560          |     | 480          |     | mA   |
| ICC2      | Standby current                                                                         | VIH = 2 V (LVTTL), After one memory cycle, RAS0 and CASx high                                                          |        | 8            |     | 8            |     | 8            |     | mA   |
|           |                                                                                         | VIH = VDD − 0.2 V (LVCMOS), After one memory cycle, RAS0 and CASx high                                                 |        | 1.2          |     | 1.2          |     | 1.2          |     | mA   |
| ICC3‡§    | Average refresh current (RAS-only refresh or CBR)                                       | VDD = 3.6 V, Minimum cycle, RAS0 cycling, CASx high (RAS-only refresh), RAS0 low after CASx low (CBR)                  |        | 720          |     | 560          |     | 480          |     | mA   |
| ICC4‡¶    | Average EDO current                                                                     | VDD = 3.6 V, RAS0 low, tHPC = MIN, CASx cycling                                                                        |        | 800          |     | 720          |     | 640          |     | mA   |
| ICC6      | Average self-refresh current                                                            | CASx < 0.2 V, RAS0 < 0.2 V, Measured after tRASS min                                                                   |        | 2            |     | 2            |     | 2            |     | mA   |
| ICC10     | Average battery back-up operating current (equivalent refresh time is 128 ms), CBR only | tRC = 31.25 μs, tRAS ≤ 300 ns VDD − 0.2 V ≤ VIH ≤ 3.9 V, 0 V ≤ VIL ≤ 0.2 V, WE0 and OE0 = VIH, Address and data stable |        | 2.8          |     | 2.8          |     | 2.8          |     | mA   |

<sup>†</sup> For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

<sup>‡</sup> Measured with outputs open

<sup>§</sup> Measured with a maximum of one address change while RAS0 = V<sub>IL</sub>

<sup>¶</sup> Measured with a maximum of one address change during each EDO cycle, t<sub>HPC</sub>

**PRODUCT PREVIEW**

TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT  
 TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT  
 EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM

SMMS685 – AUGUST 1997

switching characteristics over recommended ranges of supply voltage and ambient temperature  
 (see Note 3)

| PARAMETER                                                                                | '2XJ64xPN-50 |     | '2XJ64xPN-60 |     | '2XJ64xPN-70 |     | UNIT |
|------------------------------------------------------------------------------------------|--------------|-----|--------------|-----|--------------|-----|------|
|                                                                                          | MIN          | MAX | MIN          | MAX | MIN          | MAX |      |
| t <sub>AA</sub> Access time from column address (see Note 4)                             | 25           |     | 30           |     | 35           |     | ns   |
| t <sub>CAC</sub> Access time from $\overline{\text{CASx}}$ (see Note 4)                  | 13           |     | 15           |     | 18           |     | ns   |
| t <sub>CPA</sub> Access time from $\overline{\text{CASx}}$ precharge (see Note 4)        | 28           |     | 35           |     | 40           |     | ns   |
| t <sub>RAC</sub> Access time from $\overline{\text{RAS0}}$ (see Note 4)                  | 50           |     | 60           |     | 70           |     | ns   |
| t <sub>OEa</sub> Access time from $\overline{\text{OE0}}$ (see Note 4)                   | 13           |     | 15           |     | 18           |     | ns   |
| t <sub>CLZ</sub> Delay time, $\overline{\text{CASx}}$ to output in low impedance         | 0            |     | 0            |     | 0            |     | ns   |
| t <sub>REZ</sub> Output buffer turn off delay from $\overline{\text{RAS0}}$ (see Note 5) | 3            | 13  | 3            | 15  | 3            | 18  | ns   |
| t <sub>CEZ</sub> Output buffer turn off delay from $\overline{\text{CASx}}$ (see Note 5) | 3            | 13  | 3            | 15  | 3            | 18  | ns   |
| t <sub>OEZ</sub> Output buffer turn off delay from $\overline{\text{OE0}}$ (see Note 5)  | 3            | 13  | 3            | 15  | 3            | 18  | ns   |
| t <sub>WEZ</sub> Output buffer turn off delay from $\overline{\text{WE0}}$ (see Note 5)  | 3            | 13  | 3            | 15  | 3            | 18  | ns   |

NOTES: 3. With ac parameters, it is assumed that  $t_T = 2$  ns.

4. Access times are measured with output reference levels of  $V_{OH} = 2$  V and  $V_{OL} = 0.8$  V.

5. The maximum values of t<sub>REZ</sub>, t<sub>CEZ</sub>, t<sub>OEZ</sub>, and t<sub>WEZ</sub> are specified when the outputs are no longer driven. Data-in should not be driven until one of the applicable maximum values is satisfied.

EDO timing requirements (see Note 3)

|                                                                                                    | '2XJ64xPN-50 |        | '2XJ64xPN-60 |        | '2XJ64xPN-70 |        | UNIT |
|----------------------------------------------------------------------------------------------------|--------------|--------|--------------|--------|--------------|--------|------|
|                                                                                                    | MIN          | MAX    | MIN          | MAX    | MIN          | MAX    |      |
| t <sub>HPC</sub> Cycle time, EDO page mode, read-write                                             | 20           |        | 25           |        | 30           |        | ns   |
| t <sub>PRWC</sub> Cycle time, EDO read-write                                                       | 57           |        | 68           |        | 78           |        | ns   |
| t <sub>CSH</sub> Delay time, $\overline{\text{RAS0}}$ active to $\overline{\text{CASx}}$ precharge | 40           |        | 48           |        | 58           |        | ns   |
| t <sub>CHO</sub> Hold time, $\overline{\text{OE0}}$ from $\overline{\text{CASx}}$                  | 7            |        | 10           |        | 10           |        | ns   |
| t <sub>DOH</sub> Hold time, output from $\overline{\text{CASx}}$                                   | 5            |        | 5            |        | 5            |        | ns   |
| t <sub>CAS</sub> Pulse duration, $\overline{\text{CASx}}$ active                                   | 8            | 10 000 | 10           | 10 000 | 12           | 10 000 | ns   |
| t <sub>WPE</sub> Pulse duration, $\overline{\text{WE0}}$ active (output disable only)              | 7            |        | 7            |        | 7            |        | ns   |
| t <sub>CP</sub> Pulse duration, $\overline{\text{CASx}}$ precharge                                 | 8            |        | 10           |        | 10           |        | ns   |
| t <sub>OCH</sub> Setup time, $\overline{\text{OE0}}$ before $\overline{\text{CASx}}$               | 8            |        | 10           |        | 10           |        | ns   |
| t <sub>OEP</sub> Precharge time, $\overline{\text{OE0}}$                                           | 5            |        | 5            |        | 5            |        | ns   |

NOTE 3: With ac parameters, it is assumed that  $t_T = 2$  ns.

PRODUCT PREVIEW



ac timing requirements (see Note 3)

|                   |                                                                                                 | '2xJ64xPN-50 |         | '2xJ64xPN-60 |         | '2xJ64xPN-70 |         | UNIT |
|-------------------|-------------------------------------------------------------------------------------------------|--------------|---------|--------------|---------|--------------|---------|------|
|                   |                                                                                                 | MIN          | MAX     | MIN          | MAX     | MIN          | MAX     |      |
| t <sub>RC</sub>   | Cycle time, random read or write                                                                | 84           |         | 104          |         | 124          |         | ns   |
| t <sub>RWC</sub>  | Cycle time, read-write                                                                          | 111          |         | 135          |         | 160          |         | ns   |
| t <sub>RASP</sub> | Pulse duration, $\overline{\text{RAS0}}$ active, fast page mode (see Note 6)                    | 50           | 100 000 | 60           | 100 000 | 70           | 100 000 | ns   |
| t <sub>RAS</sub>  | Pulse duration, $\overline{\text{RAS0}}$ active, non-page mode (see Note 6)                     | 50           | 10 000  | 60           | 10 000  | 70           | 10 000  | ns   |
| t <sub>RP</sub>   | Pulse duration, $\overline{\text{RAS0}}$ precharge                                              | 30           |         | 40           |         | 50           |         | ns   |
| t <sub>WP</sub>   | Pulse duration, write command                                                                   | 8            |         | 10           |         | 10           |         | ns   |
| t <sub>RASS</sub> | Pulse duration, $\overline{\text{RAS0}}$ active, self refresh (see Note 7)                      | 100          |         | 100          |         | 100          |         | μs   |
| t <sub>RPS</sub>  | Pulse duration, $\overline{\text{RAS0}}$ precharge after self refresh                           | 90           |         | 110          |         | 130          |         | ns   |
| t <sub>ASC</sub>  | Setup time, column address                                                                      | 0            |         | 0            |         | 0            |         | ns   |
| t <sub>ASR</sub>  | Setup time, row address                                                                         | 0            |         | 0            |         | 0            |         | ns   |
| t <sub>DS</sub>   | Setup time, data in (see Note 8)                                                                | 0            |         | 0            |         | 0            |         | ns   |
| t <sub>RCS</sub>  | Setup time, read command                                                                        | 0            |         | 0            |         | 0            |         | ns   |
| t <sub>CWL</sub>  | Setup time, write command before $\overline{\text{CASx}}$ precharge                             | 8            |         | 10           |         | 12           |         | ns   |
| t <sub>RWL</sub>  | Setup time, write command before $\overline{\text{RAS0}}$ precharge                             | 8            |         | 10           |         | 12           |         | ns   |
| t <sub>WCS</sub>  | Setup time, write command before $\overline{\text{CASx}}$ active (early-write only)             | 0            |         | 0            |         | 0            |         | ns   |
| t <sub>WRP</sub>  | Setup time, $\overline{\text{WE0}}$ high before $\overline{\text{RAS0}}$ low (CBR refresh only) | 10           |         | 10           |         | 10           |         | ns   |
| t <sub>CSR</sub>  | Setup time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RAS0}}$ (CBR refresh only)  | 5            |         | 5            |         | 5            |         | ns   |
| t <sub>CAH</sub>  | Hold time, column address                                                                       | 8            |         | 10           |         | 12           |         | ns   |
| t <sub>DH</sub>   | Hold time, data in (see Note 8)                                                                 | 8            |         | 10           |         | 12           |         | ns   |
| t <sub>RAH</sub>  | Hold time, row address                                                                          | 8            |         | 10           |         | 10           |         | ns   |
| t <sub>RCH</sub>  | Hold time, read command referenced to $\overline{\text{CASx}}$ (see Note 9)                     | 0            |         | 0            |         | 0            |         | ns   |
| t <sub>RRH</sub>  | Hold time, read command referenced to $\overline{\text{RAS0}}$ (see Note 9)                     | 0            |         | 0            |         | 0            |         | ns   |
| t <sub>WCH</sub>  | Hold time, write command during $\overline{\text{CASx}}$ active (early-write only)              | 8            |         | 10           |         | 12           |         | ns   |
| t <sub>ROH</sub>  | Hold time, $\overline{\text{RAS0}}$ referenced to $\overline{\text{OE0}}$                       | 8            |         | 10           |         | 10           |         | ns   |
| t <sub>WRH</sub>  | Hold time, $\overline{\text{WE0}}$ high after $\overline{\text{RAS0}}$ low (CBR refresh only)   | 10           |         | 10           |         | 10           |         | ns   |
| t <sub>CHR</sub>  | Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RAS0}}$ (CBR refresh only)   | 10           |         | 10           |         | 10           |         | ns   |
| t <sub>OEH</sub>  | Hold time, $\overline{\text{OE0}}$ command                                                      | 13           |         | 15           |         | 18           |         | ns   |
| t <sub>RHCP</sub> | Hold time, $\overline{\text{RAS0}}$ active from $\overline{\text{CASx}}$ precharge              | 28           |         | 35           |         | 40           |         | ns   |
| t <sub>CHS</sub>  | Hold time, $\overline{\text{CASx}}$ referenced to $\overline{\text{RAS0}}$ (self refresh only)  | – 50         |         | – 50         |         | – 50         |         | ns   |
| t <sub>AWD</sub>  | Delay time, column address to write command (read-write only)                                   | 42           |         | 49           |         | 57           |         | ns   |
| t <sub>CRP</sub>  | Delay time, $\overline{\text{CASx}}$ precharge to $\overline{\text{RAS0}}$                      | 5            |         | 5            |         | 5            |         | ns   |

- NOTES: 3. With ac parameters, it is assumed that  $t_T = 2$  ns.  
 6. In a read-write cycle, t<sub>RWD</sub> and t<sub>RWL</sub> must be observed.  
 7. During the period of  $10\ \mu\text{s} \leq t_{\text{RASS}} \leq 100\ \mu\text{s}$ , the device is in a transition state from normal-operation mode to self-refresh mode.  
 8. Referenced to the later of  $\overline{\text{CASx}}$  or  $\overline{\text{WE0}}$  in write operations  
 9. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.

TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT  
 TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT  
 EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM  
 SMMS685 – AUGUST 1997

ac timing requirements (see Note 3) (continued)

|                  |                                                                                   | '2xJ64xPN-50 |     | '2xJ64xPN-60 |     | '2xJ64xPN-70 |     | UNIT |
|------------------|-----------------------------------------------------------------------------------|--------------|-----|--------------|-----|--------------|-----|------|
|                  |                                                                                   | MIN          | MAX | MIN          | MAX | MIN          | MAX |      |
| t <sub>CWD</sub> | Delay time, $\overline{\text{CASx}}$ to write command (read-write only)           | 0            |     | 0            |     | 0            |     | ns   |
| t <sub>OED</sub> | Delay time, $\overline{\text{OE0}}$ to data in                                    | 0            |     | 0            |     | 0            |     | ns   |
| t <sub>RAD</sub> | Delay time, $\overline{\text{RAS0}}$ to column address (see Note 10)              | 8            |     | 10           |     | 12           |     | ns   |
| t <sub>RAL</sub> | Delay time, column address to $\overline{\text{RAS0}}$ precharge                  | 8            |     | 10           |     | 12           |     | ns   |
| t <sub>CAL</sub> | Delay time, column address to $\overline{\text{CASx}}$ precharge                  | 0            |     | 0            |     | 0            |     | ns   |
| t <sub>RCD</sub> | Delay time, $\overline{\text{RAS0}}$ to $\overline{\text{CASx}}$ (see Note 10)    | 5            |     | 5            |     | 5            |     | ns   |
| t <sub>RPC</sub> | Delay time, $\overline{\text{RAS0}}$ precharge to $\overline{\text{CASx}}$        | 5            |     | 5            |     | 5            |     | ns   |
| t <sub>RSH</sub> | Delay time, $\overline{\text{CASx}}$ active to $\overline{\text{RAS0}}$ precharge | 8            |     | 10           |     | 12           |     | ns   |
| t <sub>RWD</sub> | Delay time, $\overline{\text{RAS0}}$ to write command (read-write only)           | 67           |     | 79           |     | 92           |     | ns   |
| t <sub>CPW</sub> | Delay time, $\overline{\text{CASx}}$ precharge to write command (read-write only) | 45           |     | 54           |     | 62           |     | ns   |
| t <sub>REF</sub> | Refresh time interval                                                             | '2EJ64DPN    | 32  | '2xJ64xPN-50 | 32  | '2xJ64xPN-70 | 32  | ms   |
|                  |                                                                                   | '2EJ64EPN    | 64  | '2xJ64xPN-60 | 64  | '2xJ64xPN-70 | 64  |      |
|                  |                                                                                   | '2FJ64xPN    | 128 | '2xJ64xPN-60 | 128 | '2xJ64xPN-70 | 128 |      |
| t <sub>T</sub>   | Transition time                                                                   | 2            | 30  | 2            | 30  | 2            | 30  | ns   |

NOTES: 3. With ac parameters, it is assumed that t<sub>T</sub> = 2 ns.  
 10. The maximum value is specified only to ensure access time.

## serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, DRAM organization, and timing parameters (see tables below). Only the first 128 bytes are programmed by Texas Instruments, while the remaining 128 bytes are available for customer use. Programming is done through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the *Texas Instruments Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

Tables in this section list the SPD contents as follows:

Table 1—TM2EJ64DPN  
Table 3—TM2FJ64DPN

Table 2—TM2EJ64EPN  
Table 4—TM2FJ64EPN

**TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT**  
**TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT**  
**EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM**

SMMS685 – AUGUST 1997

**serial presence detect (continued)**

**Table 1. Serial Presence-Detect Data for the TM2EJ64DPN**

| BYTE NO. | FUNCTION DESCRIBED                                                             | '2EJ64DPN-50                     |            | '2EJ64DPN-60                     |            | '2EJ64DPN-70                     |            |
|----------|--------------------------------------------------------------------------------|----------------------------------|------------|----------------------------------|------------|----------------------------------|------------|
|          |                                                                                | ITEM                             | DATA       | ITEM                             | DATA       | ITEM                             | DATA       |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                        | 80h        | 128 bytes                        | 80h        | 128 bytes                        | 80h        |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                        | 08h        | 256 bytes                        | 08h        | 256 bytes                        | 08h        |
| 2        | Fundamental memory type (FPM, EDO, SDRAM)                                      | EDO                              | 02h        | EDO                              | 02h        | EDO                              | 02h        |
| 3        | Number of row addresses on this assembly                                       | 11                               | 0Bh        | 11                               | 0Bh        | 11                               | 0Bh        |
| 4        | Number of column addresses on this assembly                                    | 10                               | 0Ah        | 10                               | 0Ah        | 10                               | 0Ah        |
| 5        | Number of module banks on this assembly                                        | 1 bank                           | 01h        | 1 bank                           | 01h        | 1 bank                           | 01h        |
| 6        | Data width of this assembly                                                    | 64 bits                          | 40h        | 64 bits                          | 40h        | 64 bits                          | 40h        |
| 7        | Data width continuation                                                        |                                  | 00h        |                                  | 00h        |                                  | 00h        |
| 8        | Voltage interface standard of this assembly                                    | LVTTL                            | 01h        | LVTTL                            | 01h        | LVTTL                            | 01h        |
| 9        | $\overline{\text{RAS0}}$ access time of module                                 | $t_{\text{RAC}} = 50 \text{ ns}$ | 32h        | $t_{\text{RAC}} = 60 \text{ ns}$ | 3Ch        | $t_{\text{RAC}} = 70 \text{ ns}$ | 46h        |
| 10       | $\text{CASx}$ access time of module                                            | $t_{\text{CAC}} = 13 \text{ ns}$ | 0Dh        | $t_{\text{CAC}} = 15 \text{ ns}$ | 0Fh        | $t_{\text{CAC}} = 18 \text{ ns}$ | 12h        |
| 11       | SODIMM configuration type (non-parity, parity, ECC)                            | Non-parity                       | 00h        | Non-parity                       | 00h        | Non-parity                       | 00h        |
| 12       | Refresh rate/type                                                              | 15.6 $\mu\text{s}$               | 00h        | 15.6 $\mu\text{s}$               | 00h        | 15.6 $\mu\text{s}$               | 00h        |
| 13       | DRAM width, primary DRAM                                                       | x8                               | 08h        | x8                               | 08h        | x8                               | 08h        |
| 14       | Error-checking SDRAM data width                                                | N/A                              | 00h        | N/A                              | 00h        | N/A                              | 00h        |
| 62       | SPD revision                                                                   | Rev. 1                           | 01h        | Rev. 1                           | 01h        | Rev. 1                           | 01h        |
| 63       | Checksum for bytes 0–62                                                        | 41                               | 29h        | 53                               | 35h        | 66                               | 42h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP-106E                                      | 97h                              | 9700...00h | 97h                              | 9700...00h | 97h                              | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>                                            | TBD                              |            | TBD                              |            | TBD                              |            |
| 73–90    | Manufacturer's part number <sup>†</sup>                                        | TBD                              |            | TBD                              |            | TBD                              |            |
| 91       | Die revision code <sup>†</sup>                                                 | TBD                              |            | TBD                              |            | TBD                              |            |
| 92       | PCB revision code <sup>†</sup>                                                 | TBD                              |            | TBD                              |            | TBD                              |            |
| 93–94    | Manufacturing date <sup>†</sup>                                                | TBD                              |            | TBD                              |            | TBD                              |            |
| 95–98    | Assembly serial number <sup>†</sup>                                            | TBD                              |            | TBD                              |            | TBD                              |            |
| 99–125   | Manufacturer specific data <sup>†</sup>                                        | TBD                              |            | TBD                              |            | TBD                              |            |
| 126–127  | Vendor specific data <sup>†</sup>                                              | TBD                              |            | TBD                              |            | TBD                              |            |
| 128–166  | System integrator's specific data <sup>‡</sup>                                 | TBD                              |            | TBD                              |            | TBD                              |            |
| 167–255  | Open                                                                           |                                  |            |                                  |            |                                  |            |

<sup>†</sup> TBD indicates values are determined at manufacturing time and are module dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 2. Serial Presence-Detect Data for the TM2EJ64EPN

| BYTE NO. | FUNCTION DESCRIBED                                                             | '2EJ64EPN-50                     |            | '2EJ64EPN-60                     |            | '2EJ64EPN-70                     |            |
|----------|--------------------------------------------------------------------------------|----------------------------------|------------|----------------------------------|------------|----------------------------------|------------|
|          |                                                                                | ITEM                             | DATA       | ITEM                             | DATA       | ITEM                             | DATA       |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                        | 80h        | 128 bytes                        | 80h        | 128 bytes                        | 80h        |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                        | 08h        | 256 bytes                        | 08h        | 256 bytes                        | 08h        |
| 2        | Fundamental memory type (FPM, EDO, SDRAM)                                      | EDO                              | 02h        | EDO                              | 02h        | EDO                              | 02h        |
| 3        | Number of row addresses on this assembly                                       | 12                               | 0Ch        | 12                               | 0Ch        | 12                               | 0Ch        |
| 4        | Number of column addresses on this assembly                                    | 9                                | 09h        | 9                                | 09h        | 9                                | 09h        |
| 5        | Number of module banks on this assembly                                        | 1 bank                           | 01h        | 1 bank                           | 01h        | 1 bank                           | 01h        |
| 6        | Data width of this assembly                                                    | 64 bits                          | 40h        | 64 bits                          | 40h        | 64 bits                          | 40h        |
| 7        | Data width continuation                                                        |                                  | 00h        |                                  | 00h        |                                  | 00h        |
| 8        | Voltage interface standard of this assembly                                    | LVTTL                            | 01h        | LVTTL                            | 01h        | LVTTL                            | 01h        |
| 9        | $\overline{\text{RAS0}}$ access time of module                                 | $t_{\text{RAC}} = 50 \text{ ns}$ | 32h        | $t_{\text{RAC}} = 60 \text{ ns}$ | 3Ch        | $t_{\text{RAC}} = 70 \text{ ns}$ | 46h        |
| 10       | $\overline{\text{CASx}}$ access time of module                                 | $t_{\text{CAC}} = 13 \text{ ns}$ | 0Dh        | $t_{\text{CAC}} = 15 \text{ ns}$ | 0Fh        | $t_{\text{CAC}} = 18 \text{ ns}$ | 12h        |
| 11       | SODIMM configuration type (non-parity, parity, ECC)                            | Non-parity                       | 00h        | Non-parity                       | 00h        | Non-parity                       | 00h        |
| 12       | Refresh rate/type                                                              | 15.6 $\mu\text{s}$               | 00h        | 15.6 $\mu\text{s}$               | 00h        | 15.6 $\mu\text{s}$               | 00h        |
| 13       | DRAM width, primary DRAM                                                       | x8                               | 08h        | x8                               | 08h        | 08h                              | 08h        |
| 14       | Error-checking SDRAM data width                                                | N/A                              | 00h        | N/A                              | 00h        | N/A                              | 00h        |
| 62       | SPD revision                                                                   | Rev. 1                           | 01h        | Rev. 1                           | 01h        | Rev. 1                           | 01h        |
| 63       | Checksum for bytes 0–62                                                        | 41                               | 29h        | 53                               | 35h        | 66                               | 42h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP-106E                                      | 97h                              | 9700...00h | 97h                              | 9700...00h | 97h                              | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>                                            | TBD                              |            | TBD                              |            | TBD                              |            |
| 73–90    | Manufacturer's part number <sup>†</sup>                                        | TBD                              |            | TBD                              |            | TBD                              |            |
| 91       | Die revision code <sup>†</sup>                                                 | TBD                              |            | TBD                              |            | TBD                              |            |
| 92       | PCB revision code <sup>†</sup>                                                 | TBD                              |            | TBD                              |            | TBD                              |            |
| 93–94    | Manufacturing date <sup>†</sup>                                                | TBD                              |            | TBD                              |            | TBD                              |            |
| 95–98    | Assembly serial number <sup>†</sup>                                            | TBD                              |            | TBD                              |            | TBD                              |            |
| 99–125   | Manufacturer specific data <sup>†</sup>                                        | TBD                              |            | TBD                              |            | TBD                              |            |
| 126–127  | Vendor specific data <sup>†</sup>                                              | TBD                              |            | TBD                              |            | TBD                              |            |
| 128–166  | System integrator's specific data <sup>‡</sup>                                 | TBD                              |            | TBD                              |            | TBD                              |            |
| 167–255  | Open                                                                           |                                  |            |                                  |            |                                  |            |

<sup>†</sup> TBD indicates values are determined at manufacturing time and are module dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

TM2EJ64DPN, TM2FJ64DPN 2097152 BY 64-BIT  
 TM2EJ64EPN, TM2FJ64EPN 2097152 BY 64-BIT  
 EXTENDED-DATA-OUT DYNAMIC RAM MODULES — SODIMM

SMMS685 – AUGUST 1997

serial presence detect (continued)

Table 3. Serial Presence-Detect Data for the TM2FJ64DPN

| BYTE NO. | FUNCTION DESCRIBED                                                             | '2FJ64DPN-50                |            | '2FJ64DPN-60                |            | '2FJ64DPN-70                |            |
|----------|--------------------------------------------------------------------------------|-----------------------------|------------|-----------------------------|------------|-----------------------------|------------|
|          |                                                                                | ITEM                        | DATA       | ITEM                        | DATA       | ITEM                        | DATA       |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                   | 80h        | 128 bytes                   | 80h        | 128 bytes                   | 80h        |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                   | 08h        | 256 bytes                   | 08h        | 256 bytes                   | 08h        |
| 2        | Fundamental memory type (FPM, EDO, SDRAM)                                      | EDO                         | 02h        | EDO                         | 02h        | EDO                         | 02h        |
| 3        | Number of row addresses on this assembly                                       | 11                          | 0Bh        | 11                          | 0Bh        | 11                          | 0Bh        |
| 4        | Number of column addresses on this assembly                                    | 10                          | 0Ah        | 10                          | 0Ah        | 10                          | 0Ah        |
| 5        | Number of module banks on this assembly                                        | 1 bank                      | 01h        | 1 bank                      | 01h        | 1 bank                      | 01h        |
| 6        | Data width of this assembly                                                    | 64 bits                     | 40h        | 64 bits                     | 40h        | 64 bits                     | 40h        |
| 7        | Data width continuation                                                        |                             | 00h        |                             | 00h        |                             | 00h        |
| 8        | Voltage interface standard of this assembly                                    | LVTTL                       | 01h        | LVTTL                       | 01h        | LVTTL                       | 01h        |
| 9        | RAS0 access time of module                                                     | t <sub>RAC</sub> = 50 ns    | 32h        | t <sub>RAC</sub> = 60 ns    | 3Ch        | t <sub>RAC</sub> = 70 ns    | 46h        |
| 10       | CASx access time of module                                                     | t <sub>CAC</sub> = 13 ns    | 0Dh        | t <sub>CAC</sub> = 15 ns    | 0Fh        | t <sub>CAC</sub> = 18 ns    | 12h        |
| 11       | SODIMM configuration type (non-parity, parity, ECC)                            | Non-parity                  | 00h        | Non-parity                  | 00h        | Non-parity                  | 00h        |
| 12       | Refresh rate/type                                                              | 15.6 $\mu$ s / self-refresh | 80h        | 15.6 $\mu$ s / self-refresh | 80h        | 15.6 $\mu$ s / self-refresh | 80h        |
| 13       | DRAM width, primary DRAM                                                       | x8                          | 08h        | x8                          | 08h        | x8                          | 08h        |
| 14       | Error-checking SDRAM data width                                                | N/A                         | 00h        | N/A                         | 00h        | N/A                         | 00h        |
| 62       | SPD revision                                                                   | Rev. 1                      | 01h        | Rev. 1                      | 01h        | Rev. 1                      | 01h        |
| 63       | Checksum for bytes 0–62                                                        | 169                         | A9h        | 181                         | B5h        | 194                         | C2h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP-106E                                      | 97h                         | 9700...00h | 97h                         | 9700...00h | 97h                         | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>                                            | TBD                         |            | TBD                         |            | TBD                         |            |
| 73–90    | Manufacturer's part number <sup>†</sup>                                        | TBD                         |            | TBD                         |            | TBD                         |            |
| 91       | Die revision code <sup>†</sup>                                                 | TBD                         |            | TBD                         |            | TBD                         |            |
| 92       | PCB revision code <sup>†</sup>                                                 | TBD                         |            | TBD                         |            | TBD                         |            |
| 93–94    | Manufacturing date <sup>†</sup>                                                | TBD                         |            | TBD                         |            | TBD                         |            |
| 95–98    | Assembly serial number <sup>†</sup>                                            | TBD                         |            | TBD                         |            | TBD                         |            |
| 99–125   | Manufacturer specific data <sup>†</sup>                                        | TBD                         |            | TBD                         |            | TBD                         |            |
| 126–127  | Vendor specific data <sup>†</sup>                                              | TBD                         |            | TBD                         |            | TBD                         |            |
| 128–166  | System integrator's specific data <sup>‡</sup>                                 | TBD                         |            | TBD                         |            | TBD                         |            |
| 167–255  | Open                                                                           |                             |            |                             |            |                             |            |

<sup>†</sup> TBD indicates values are determined at manufacturing time and are module dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

serial presence detect (continued)

Table 4. Serial Presence-Detect Data for the TM2FJ64EPN

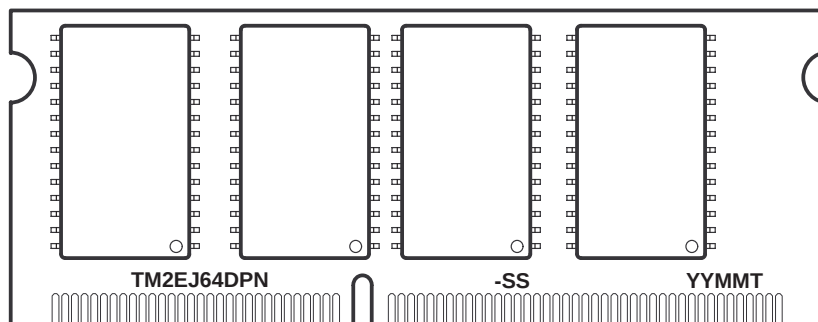
| BYTE NO. | FUNCTION DESCRIBED                                                             | '2FJ64EPN-50                      |            | '2FJ64EPN-60                      |            | '2FJ64EPN-70                      |            |
|----------|--------------------------------------------------------------------------------|-----------------------------------|------------|-----------------------------------|------------|-----------------------------------|------------|
|          |                                                                                | ITEM                              | DATA       | ITEM                              | DATA       | ITEM                              | DATA       |
| 0        | Defines number of bytes written into serial memory during module manufacturing | 128 bytes                         | 80h        | 128 bytes                         | 80h        | 128 bytes                         | 80h        |
| 1        | Total number of bytes of SPD memory device                                     | 256 bytes                         | 08h        | 256 bytes                         | 08h        | 256 bytes                         | 08h        |
| 2        | Fundamental memory type (FPM, EDO, SDRAM)                                      | EDO                               | 02h        | EDO                               | 02h        | EDO                               | 02h        |
| 3        | Number of row addresses on this assembly                                       | 12                                | 0Ch        | 12                                | 0Ch        | 12                                | 0Ch        |
| 4        | Number of column addresses on this assembly                                    | 9                                 | 09h        | 9                                 | 09h        | 9                                 | 09h        |
| 5        | Number of module banks on this assembly                                        | 1 bank                            | 02h        | 1 bank                            | 02h        | 1 bank                            | 02h        |
| 6        | Data width of this assembly                                                    | 64 bits                           | 40h        | 64 bits                           | 40h        | 64 bits                           | 40h        |
| 7        | Data width continuation                                                        |                                   | 00h        |                                   | 00h        |                                   | 00h        |
| 8        | Voltage interface standard of this assembly                                    | LVTTL                             | 01h        | LVTTL                             | 01h        | LVTTL                             | 01h        |
| 9        | $\overline{\text{RAS0}}$ access time of module                                 | $t_{\text{RAC}} = 50 \text{ ns}$  | 32h        | $t_{\text{RAC}} = 60 \text{ ns}$  | 3Ch        | $t_{\text{RAC}} = 70 \text{ ns}$  | 46h        |
| 10       | $\overline{\text{CASx}}$ access time of module                                 | $t_{\text{CAC}} = 13 \text{ ns}$  | 0Dh        | $t_{\text{CAC}} = 15 \text{ ns}$  | 0Fh        | $t_{\text{CAC}} = 18 \text{ ns}$  | 12h        |
| 11       | SODIMM configuration type (non-parity, parity, ECC)                            | Non-parity                        | 00h        | Non-parity                        | 00h        | Non-parity                        | 00h        |
| 12       | Refresh rate/type                                                              | 15.6 $\mu\text{s}$ / self-refresh | 80h        | 15.6 $\mu\text{s}$ / self-refresh | 80h        | 15.6 $\mu\text{s}$ / self-refresh | 80h        |
| 13       | DRAM width, primary DRAM                                                       | x8                                | 08h        | x8                                | 08h        | x8                                | 08h        |
| 14       | Error-checking SDRAM data width                                                | N/A                               | 00h        | N/A                               | 00h        | N/A                               | 00h        |
| 62       | SPD revision                                                                   | Rev. 1                            | 01h        | Rev. 1                            | 01h        | Rev. 1                            | 01h        |
| 63       | Checksum for bytes 0–62                                                        | 169                               | A9h        | 181                               | B5h        | 194                               | C2h        |
| 64–71    | Manufacturer's JEDEC ID code per JEP-106E                                      | 97h                               | 9700...00h | 97h                               | 9700...00h | 97h                               | 9700...00h |
| 72       | Manufacturing location <sup>†</sup>                                            | TBD                               |            | TBD                               |            | TBD                               |            |
| 73–90    | Manufacturer's part number <sup>†</sup>                                        | TBD                               |            | TBD                               |            | TBD                               |            |
| 91       | Die revision code <sup>†</sup>                                                 | TBD                               |            | TBD                               |            | TBD                               |            |
| 92       | PCB revision code <sup>†</sup>                                                 | TBD                               |            | TBD                               |            | TBD                               |            |
| 93–94    | Manufacturing date <sup>†</sup>                                                | TBD                               |            | TBD                               |            | TBD                               |            |
| 95–98    | Assembly serial number <sup>†</sup>                                            | TBD                               |            | TBD                               |            | TBD                               |            |
| 99–125   | Manufacturer specific data <sup>†</sup>                                        | TBD                               |            | TBD                               |            | TBD                               |            |
| 126–127  | Vendor specific data <sup>†</sup>                                              | TBD                               |            | TBD                               |            | TBD                               |            |
| 128–166  | System integrator's specific data <sup>‡</sup>                                 | TBD                               |            | TBD                               |            | TBD                               |            |
| 167–255  | Open                                                                           |                                   |            |                                   |            |                                   |            |

<sup>†</sup> TBD indicates values are determined at manufacturing time and are module dependent.

<sup>‡</sup> These TBD values are determined and programmed by the customer (optional).

PRODUCT PREVIEW

device symbolization (TM2EJ64DPN illustrated)



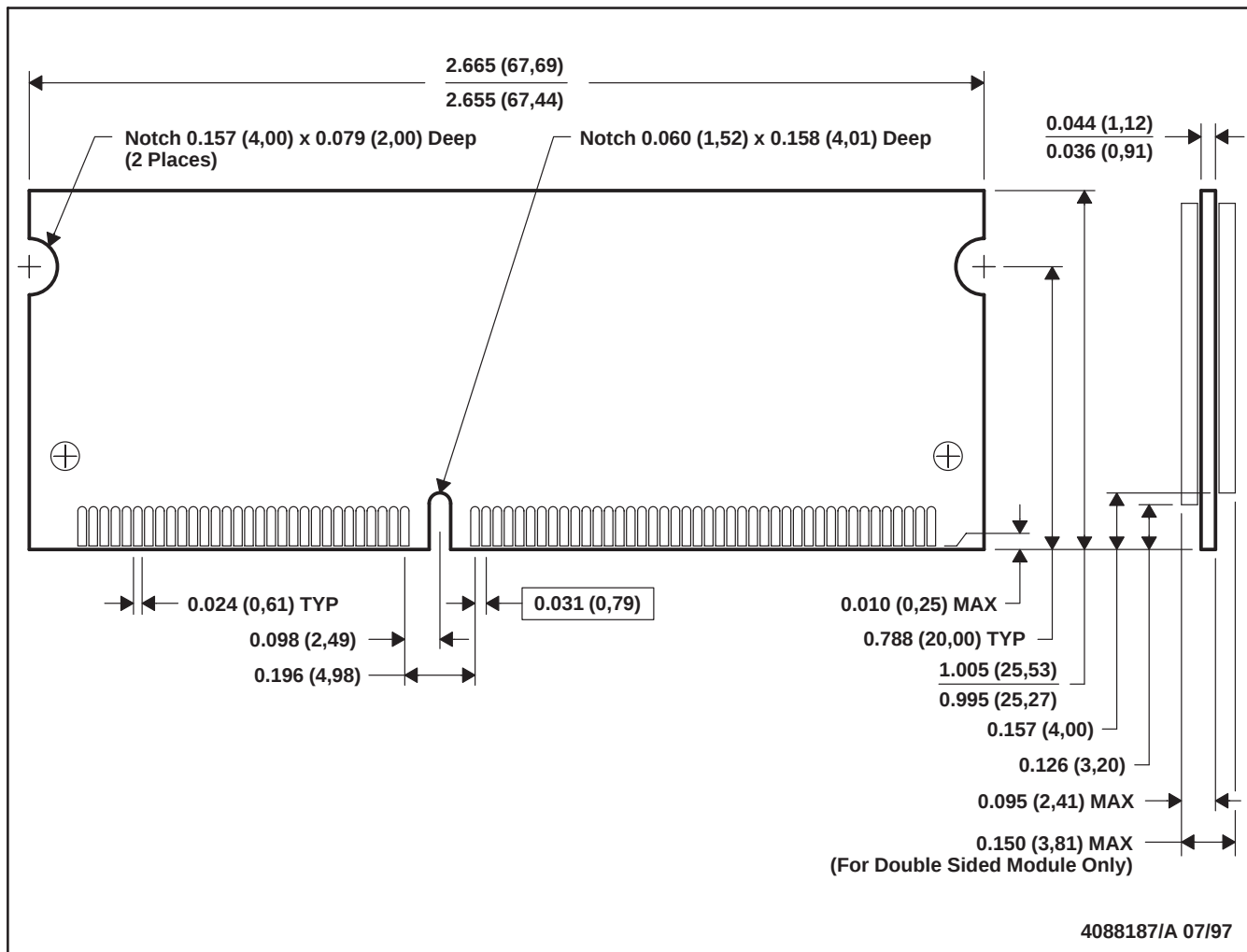
YY = Year Code  
 MM = Month Code  
 T = Assembly Site Code  
 -SS = Speed Code

NOTE A: Location of symbolization may vary.

## MECHANICAL DATA

BDM (R-SODIMM-N144)

SMALL OUTLINE DUAL IN-LINE MEMORY MODULE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MO-190

PRODUCT PREVIEW

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.