DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

TISP6L7591 SLIC Protector

Rated for Standard Lightning Wave Shapes

Wave Shape	Standard	I_{PP} A
2/10	GR-1089-CORE	±80
10/700	ITU-T K.20 & K.21	±40
10/1000	GR-1089-CORE	±30

Rated for AC Fault Currents

AC Hz	Time s	I_{TSM} A
50/60	0.01	±5
	1	±3.5

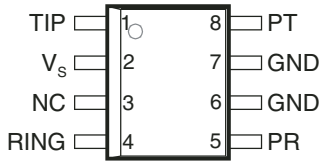
Gate Trigger Current ..... 15 mA max.

High V_S Voltage ..... -80 V max.

High Holding Current ..... 150 mA min.

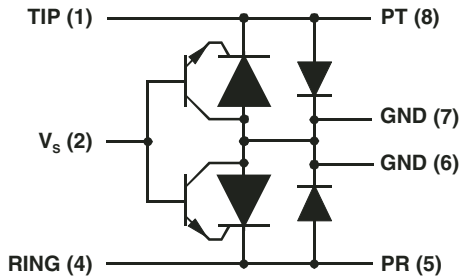
..... UL Recognized Components

D Package (Top View)



MD6XAND

Device Symbol



SD6XAEE

Pin	Symbol	Comment	Pin	Symbol	Comment
1	TIP	Line-side TIP	8	PT	Protected TIP to SLIC
2	V_S	Supply voltage to Gate	7	GND	Ground
3	NC	No Internal connection	6	GND	Ground
4	RING	Line-side RING	5	PR	Protected RING to SLIC

Note: Pins 1 and 4 must always be connected to the protection resistors shown in Figures 2 and 3 (Line Feed Circuitry). The SLIC can be connected either to the protected outputs (pins 5 and 8) or to the inputs (pins 1 and 4).

Description

The TISP6L7591 is a dual forward-conducting buffered p-gate overvoltage protector. It is designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The TISP6L7591 limits voltages that exceed the SLIC supply rail voltage.

The SLIC line driver section is typically powered from 0 V (ground) and a negative voltage, V_S, in the region of -20 V to -80 V. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. The negative protection voltage will then track the negative supply voltage and the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector will switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of TISP6L7591 crowbar prevents d.c. latchup.

These monolithic protection devices are fabricated in ion-implanted planar vertical power structures for high reliability and in normal system operation they are virtually transparent. The TISP6L7591 is available in 8-pin plastic small-outline surface mount package.

How To Order

Device	Package	Carrier	For Standard Termination Finish Order As	For Lead Free Termination Finish Order As
TISP6L7591	D (8-pin Small-Outline)	R (Embossed Tape Reeled)	TISP6L7591DR	TISP6L7591DR-S

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

MAY 2002 - REVISED FEBRUARY 2005

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak TIP or RING off-state voltage, $V_{(VS)(TIP)}$ = 0, $V_{(VS)(RING)}$ = 0	$V_{(TIP)M}$, $V_{(RING)M}$	-100	V
Repetitive peak V_S voltage, V_{TIP} = 0, V_{RING} = 0	$V_{(VS)M}$	-80	V
Non-repetitive peak pulse current (see Notes 1, 2 and 3) 10/1000 μs (Bellcore GR-1089-CORE, open-circuit voltage wave shape 10/1000 μs) 5/320 μs (ITU-T K.20 & K.21, open-circuit voltage wave shape 10/700 μs) 2/10 μs (Bellcore GR-1089-CORE, open-circuit voltage wave shape 2/10 μs)	I_{PP}	 30 40 80	A
Non-repetitive peak on-state current, 50 Hz to 60 Hz (see Notes 1, 2 and 3) 10 ms 1 s	I_{TSM}	 5 3.5	A
Non-repetitive peak V_S current, half sine wave 10 ms, cathodes commoned (see Note 1)	$I_{(VS)M}$	+2	A
Operating free-air temperature range	T_A	-40 to +85	°C
Storage temperature range	T_{stg}	-40 to +125	°C

NOTES: 1. Initially the protector must be in thermal equilibrium. The surge may be repeated after the device returns to its initial conditions.
2. These non-repetitive rated currents are peak values for either polarity. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair).
3. Supply Voltage, V_S, range -20 V to -80 V.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
V_F	Forward voltage	I_P = 5 A, t_P = 1 ms				3	V
V_{FP}	Peak forward voltage	I_{PP} = 30 A, 10/1000				15	V
I_{GT}	Gate trigger current	V_S = -48 V		0.2		15	mA
I_H	Holding current	t_P = 10 ms, V_S = -48 V		-150			mA
V_T	Trip voltage	d.c.				V_S-2.8	V
V_{SGL}	Dynamic trip voltage	I_{PP} = -30 A, 10/1000, V_S = -48 V				-63	V
I_{RG}	Reverse gate current	V_S = -75 V, V_{TIP} = 0, V_{RING} = 0	T_A = 25 °C			-5	μA
			T_A = 70 °C			-50	μA
dv_R/dt	Critical rate of voltage rise	TIP or RING lead		±1000			V/μs
V_{ON}	On-state voltage	I_T = -0.5 A, t_P = 1 ms I_T = -3.0 A, t_P = 1 ms				-3 -4	V
I_R	Reverse current (Gate open)	V_R = -85 V, I_G = 0	T_A = 25 °C			-5	μA
			T_A = 70 °C			-50	μA
C_{off}	TIP or RING to GND off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 4)	V_R = -3 V			50	pF
			V_R = -48 V			40	pF

NOTE 4: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Parameter Measurement Information

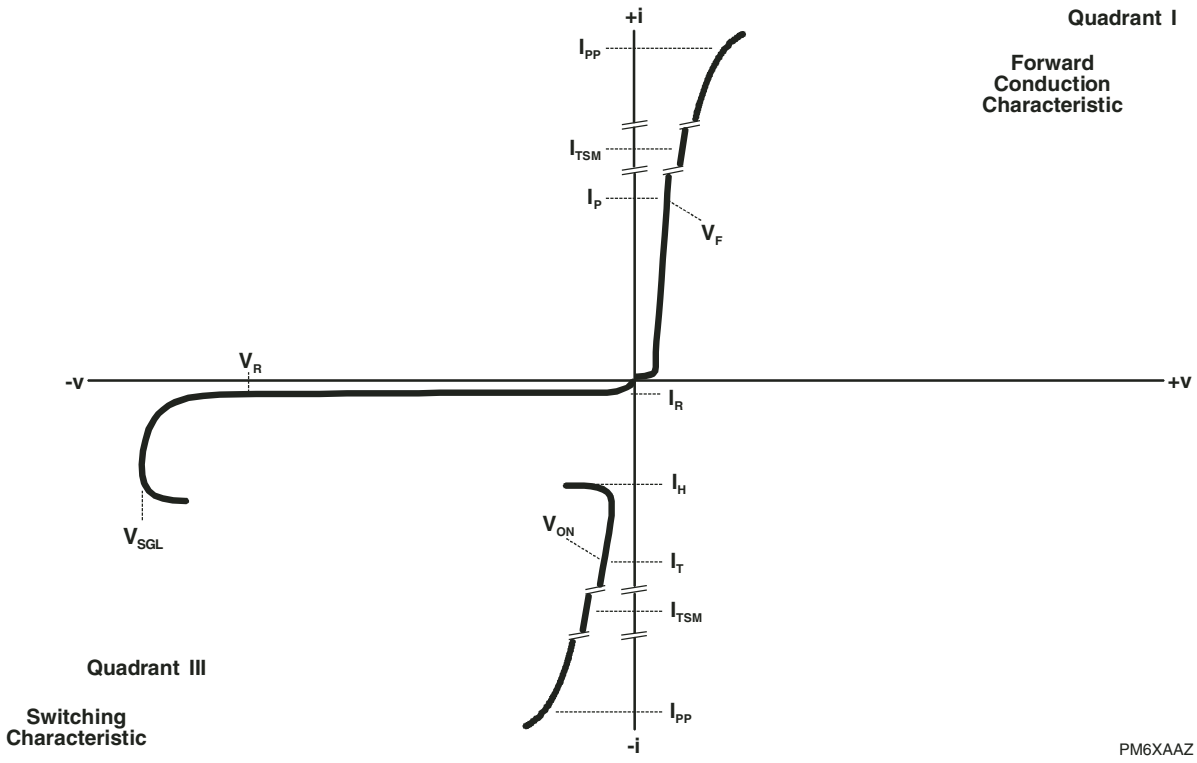
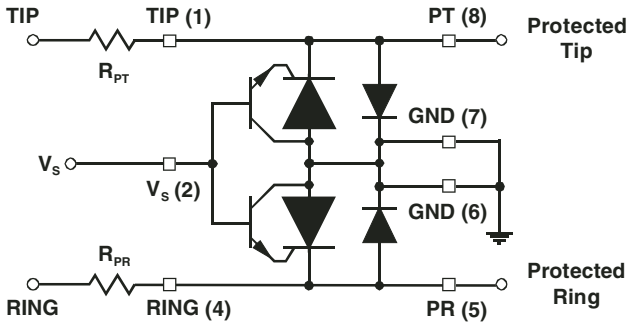


Figure 1. Typical Voltage-Current Characteristic of the SLIC Protector
Unless Otherwise Noted, All Voltages are Referenced to the Anode

Letter Symbol Definitions

Symbol	Parameter
I_H	Thyristor holding current
I_{GT}	Gate trigger current into V_S pin
I_P	Pulse current
I_{PP}	Peak pulse current
I_{RG}	Reverse current V_S to TIP or RING
I_T	TIP or RING current when thyristor is on
I_R	Reverse current, TIP or RING to GND
V_F	Forward voltage, TIP or RING to GND
V_{FP}	Peak forward voltage, TIP or RING to GND
V_T	Trip voltage, TIP or RING to V_S
V_{SGL}	Dynamic trip voltage, TIP or RING to V_S
V_{ON}	Thyristor on voltage at I_T
V_R	TIP or RING voltage when thyristor is off
C_{off}	Off-state capacitance, TIP or RING to Ground

APPLICATIONS INFORMATION



R_{PT} and R_{PR} must be properly selected for proper operation and/or response.

AI6XDN

Figure 2. Standard Configuration

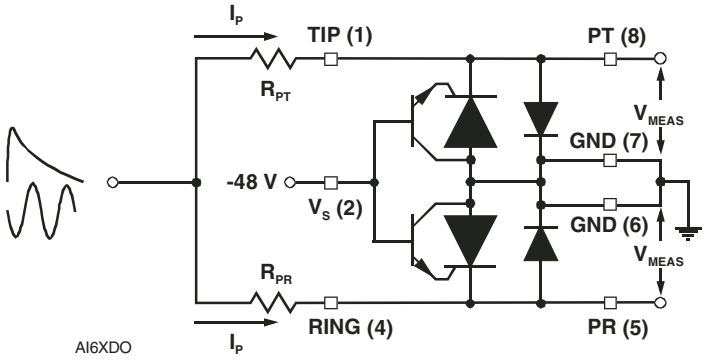


Figure 3. Test Circuit

MECHANICAL DATA

Device Symbolization Code

Devices will be coded as below.

Device	Symbolization Code
TISP6L7591D	L7591

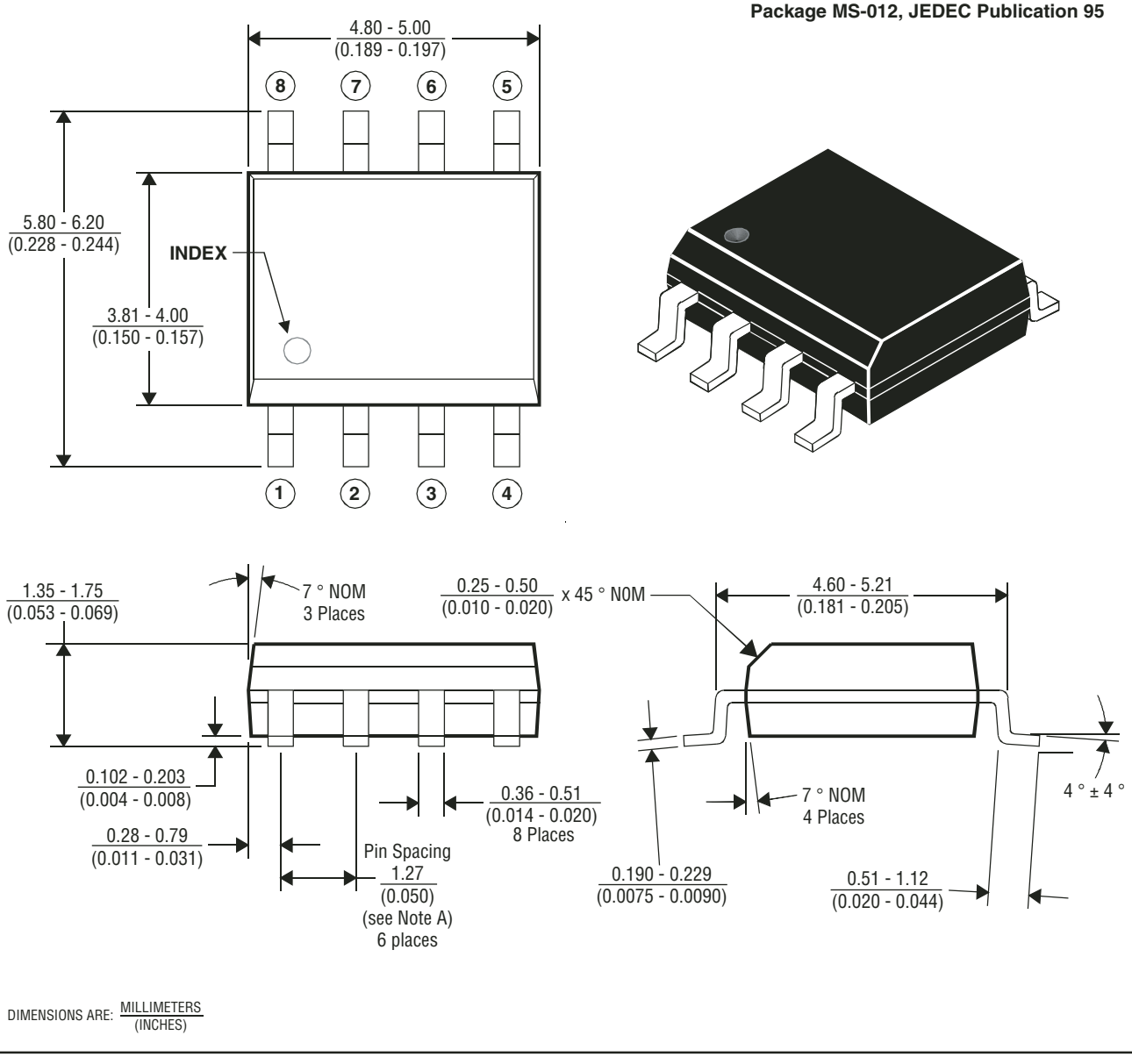
MECHANICAL DATA

D008 Plastic Small-outline Package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound is designed to withstand normal soldering temperatures with no deformation and circuit performance characteristics will remain stable when operated in most high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008

8-pin Small Outline Microelectronic Standard Package MS-012, JEDEC Publication 95



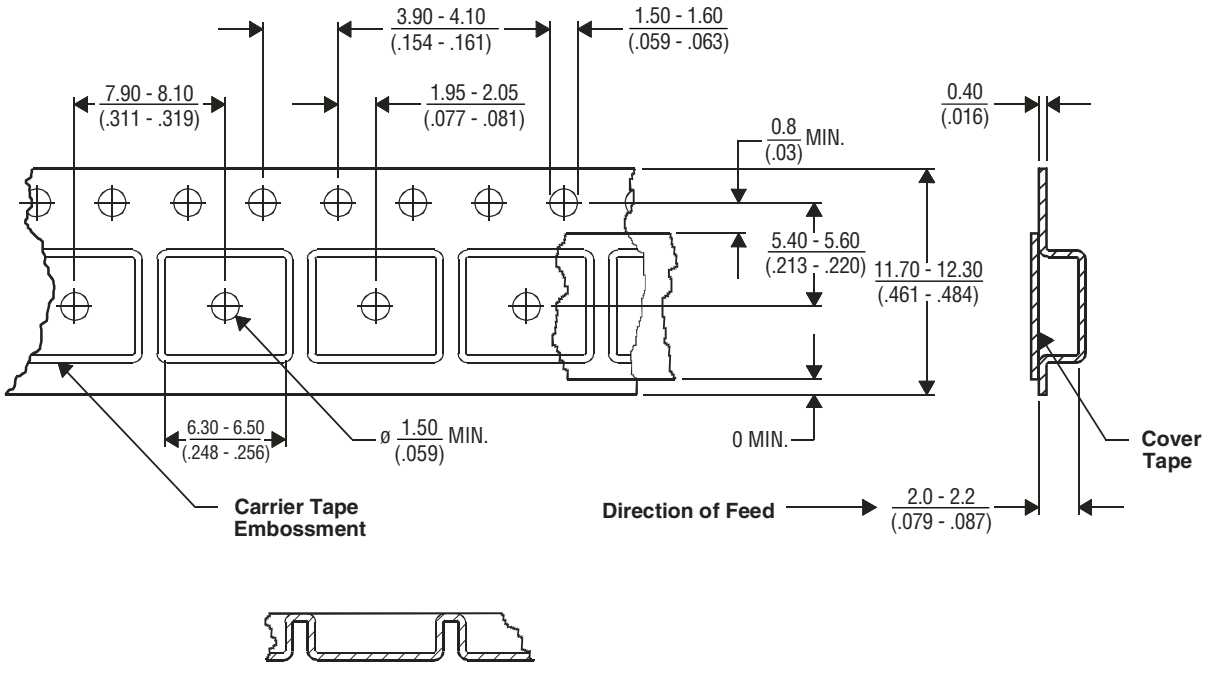
MDXXAAE

NOTES: A. Leads are within 0.25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0.15 (0.006).
D. Lead tips to be planar within ±0.051 (0.002).

MECHANICAL DATA

D008 Tape DImensions

D008 Package (8-pin Small Outline) Single-Sprocket Tape



DIMENSIONS ARE: MILLIMETERS / (INCHES)

NOTES: A. Taped devices are supplied on a reel of the following dimensions:- MDXXATC

Reel diameter: 330 +0.0/-4.0 (12.99 +0.0/-.157)

Reel hub diameter: 100 ± 2.0 (3.937 ± .079)

Reel axial hole: 13.0 ± 0.2 (.512 ± .008)

B. 2500 devices are on a reel.