

**TC74AC521P, TC74AC521F, TC74AC521FW**

(Note) The JEDEC SOP (FW) is not available in Japan.

**8-BIT EQUALITY COMPARATOR**

The TC74AC521 is an advanced high speed CMOS 8-BIT DIGITAL COMPARATOR fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

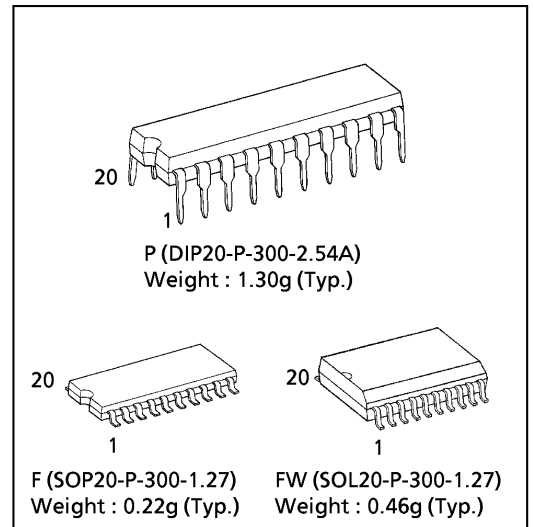
It compares two 8-bit binary or BCD words applied inputs P<sub>0</sub>~P<sub>7</sub>, and inputs Q<sub>0</sub>~Q<sub>7</sub>, and indicates whether or not they are equal.

A signal active low enable is provided to facilitate cascading of several packages to compare of words greater than 8 bits.

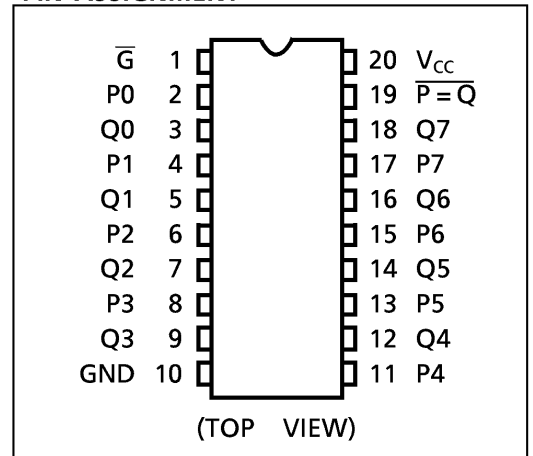
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES:**

- High Speed..... $t_{pd} = 6.4ns( \text{typ.} )$  at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 8\mu A( \text{Max.} )$  at  $T_a = 25^{\circ}C^*$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\%V_{CC} ( \text{Min.} )$
- Symmetrical Output Impedance...  $|I_{OH}| = |I_{OL}| = 24mA( \text{Min.} )$   
 Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC}( \text{opr.} ) = 2V \sim 5.5V$
- Pin and Function Compatible with 74F521



**PIN ASSIGNMENT**

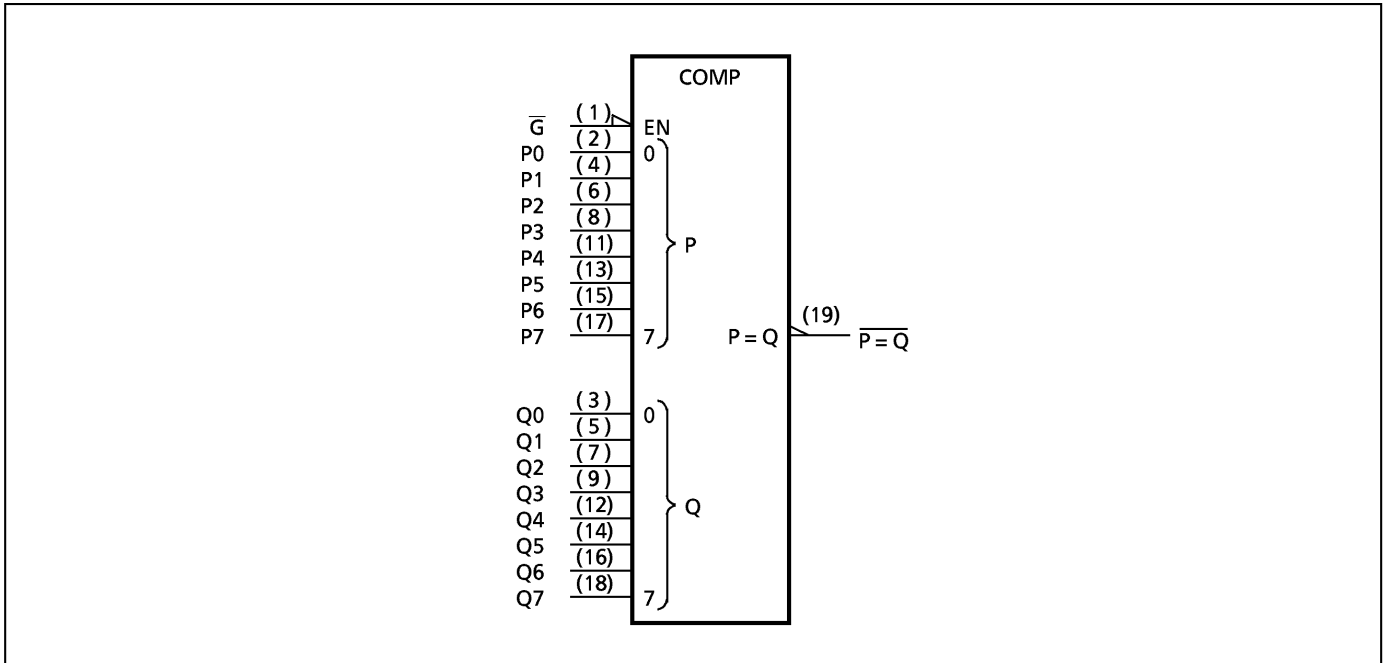


**TRUTH TABLE**

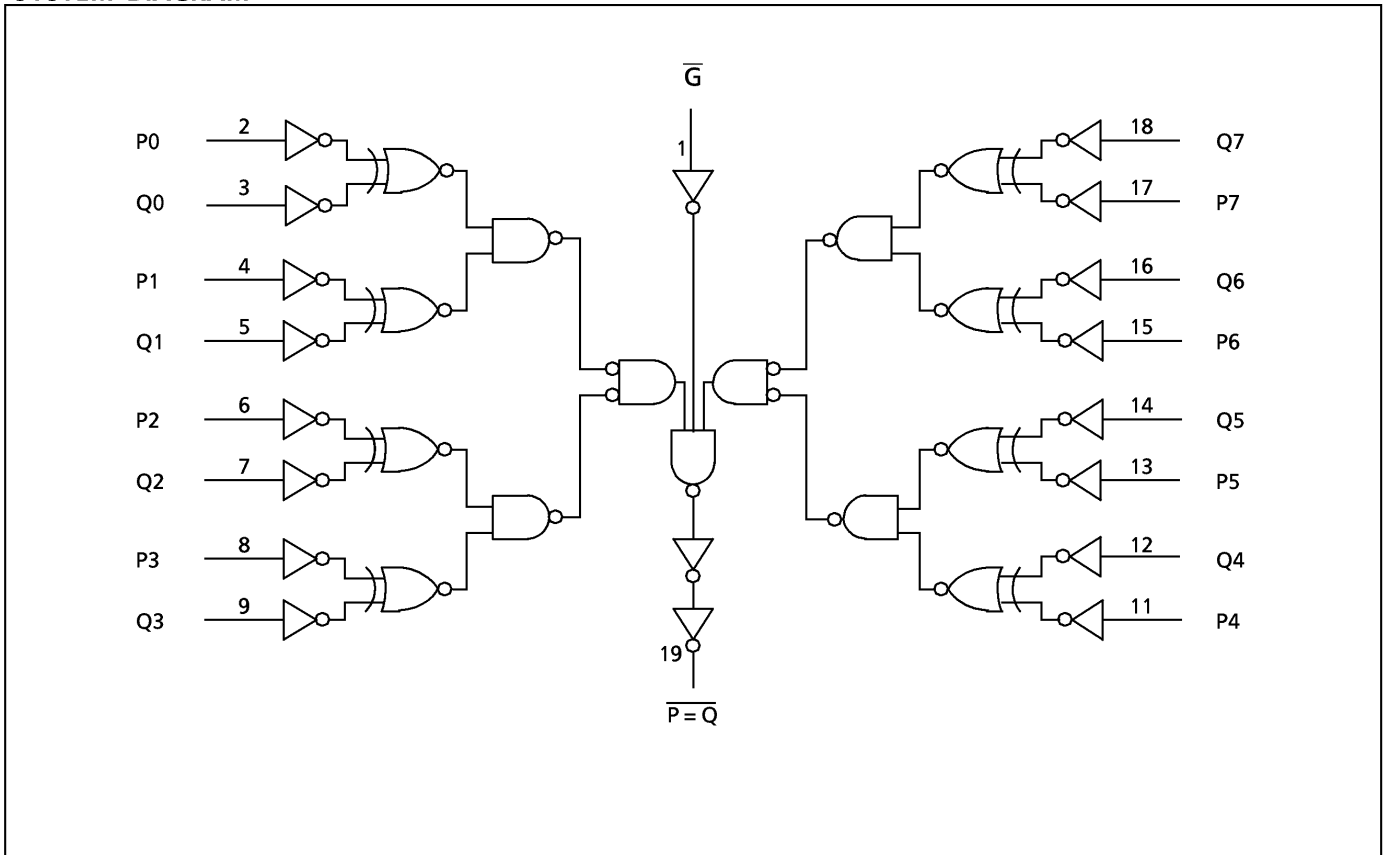
INPUTS		OUTPUT
P, Q	$\bar{G}$	$\overline{P=Q}$
P = Q	L	L
P ≠ Q	L	H
X	H	H

X : Don't Care

**IEC LOGIC SYMBOL**



**SYSTEM DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V <sub>CC</sub>	-0.5~7.0	V
DC Input Voltage	V <sub>IN</sub>	-0.5~V <sub>CC</sub> +0.5	V
DC Output Voltage	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> +0.5	V
Input Diode Current	I <sub>IK</sub>	±20	mA
Output Diode Current	I <sub>OK</sub>	±50	mA
DC Output Current	I <sub>OUT</sub>	±50	mA
DC V <sub>CC</sub> /Ground Current	I <sub>CC</sub>	±100	mA
Power Dissipation	P <sub>D</sub>	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T <sub>stg</sub>	-65~150	°C

\*500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V <sub>CC</sub>	2.0~5.5	V
Input Voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	V
Output Voltage	V <sub>OUT</sub>	0~V <sub>CC</sub>	V
Operating Temperature	T <sub>opr</sub>	-40~85	°C
Input Rise and Fall Time	dt / dV	0~ 100 (V <sub>CC</sub> = 3.3 ± 0.3V) 0~ 20 (V <sub>CC</sub> = 5 ± 0.5V)	ns / V

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT			
				MIN.	TYP.	MAX.	MIN.	MAX.				
High - Level Input Voltage	V <sub>IH</sub>		2.0	1.50	—	—	1.50	—	V			
			3.0	2.10	—	—	2.10	—				
			5.5	3.85	—	—	3.85	—				
Low - Level Input Voltage	V <sub>IL</sub>		2.0	—	—	0.50	—	0.50	V			
			3.0	—	—	0.90	—	0.90				
			5.5	—	—	1.65	—	1.65				
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	2.0	1.9	2.0	—	1.9	—	V		
				3.0	2.9	3.0	—	2.9	—			
				4.5	4.4	4.5	—	4.4	—			
				3.0	2.58	—	—	2.48	—			
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	2.0	—	0.0	0.1	—	0.1	V		
				3.0	—	0.0	0.1	—	0.1			
				4.5	—	0.0	0.1	—	0.1			
				3.0	—	—	0.36	—	0.44			
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.1	—	±1.0	μA			
			Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—		8.0	—	80.0

\* : This spec indicates the capability of driving 50Ω transmission lines.  
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ , Input  $t_r = t_f = 3\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time ( Pn, Qn - $\overline{P=Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		3.3 ± 0.3	—	10.5	17.5	1.0	20.0	ns
			5.0 ± 0.5	—	7.2	11.0	1.0	12.5	
Propagation Delay Time ( $\overline{G} - \overline{P=Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		3.3 ± 0.3	—	7.2	11.5	1.0	13.0	ns
			5.0 ± 0.5	—	4.8	7.0	1.0	8.0	
Input Capacitance	C <sub>IN</sub>		—	5	10	—	10	pF	
Power Dissipation Capacitance	C <sub>PD</sub> (1)		—	34	—	—	—		

Note(1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(\text{opr.})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

**DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)**

Unit in mm



**SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)**

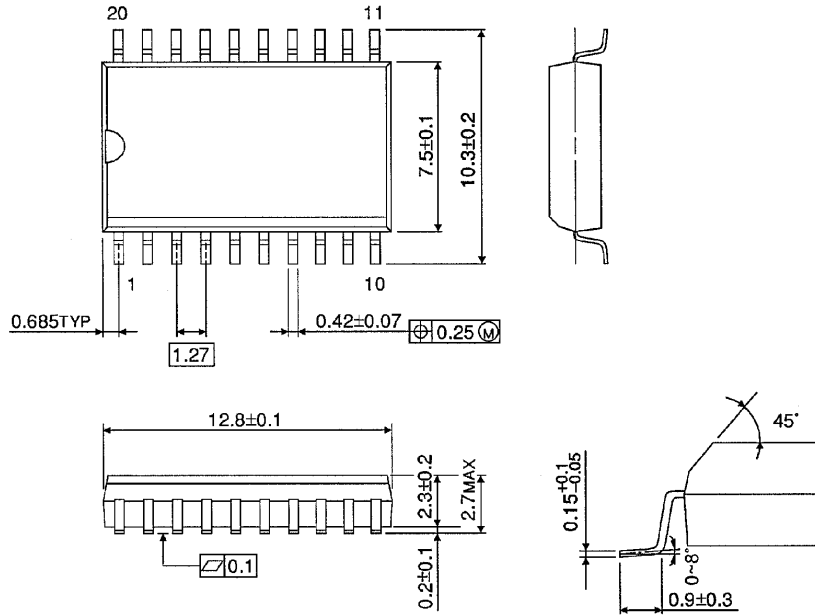
Unit in mm



**SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

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