SIEMENS

ICs for Communications

Mini IOM®-2 Controller
MICO

PEF 2015 Version 1.1

Data Sheet 12.97

DS 1

PEF 2015 Revision History: Current Version: Data Sheet 12.97		
Previous Version: Preliminary Data Sheet 05.97		
Page (in previous Version)	Page (in new Version)	Subjects (major changes since last revision)
34, 58	34, 58	MFAIR: new reset value = 00xx $xxxx_B$
34, 60	34, 60	CIFIFO: new reset value = 0xxx $xxxx_B$
34, 69, 70	34, 69, 70	VNSR register: Reset value corrected to 02H (Version bits for MICO V1.1: 0010)
-	75, 78	New timing in Motorola mode: t_{RWh} = 10 ns max. (R/$\overline{W}$ hold time from $\overline{DS}$)
77, 78, 80	75, 76, 78	Timing value and definition changed: t_{DW} = 0 ns min. (Data set-up time to $\overline{CS}$xWR / $\overline{CS}$x$\overline{DS}$ in write access)

Edition 12.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
HL DT CE

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.
For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

1 Overview

The Mini IOM-2 Controller MICO (PEF 2015) is an interface controller optimized for small line card applications or Intelligent NTs. It is derived from the EPIC core. The MICO supports up to 16 analog subscribers (up to 8 using the SLICOFI) or up to 8 ISDN-BA subscribers.

The MICO is used as an interface device on linecards between the subscriber circuits and the network. Therefore it provides one IOM-2 interface for connection of up to 8 ISDN-BA subscribers or up to 16 analog subscribers (up to 8 using the SLICOFI).The MICO also provides one PCM interface for connection to the main system. Additionally the MICO is used to control the subscriber circuits via the C/I and monitor channel as specified in the IOM-2 specification. A parallel µP interface is provided for device programming.

Furthermore the MICO contains a nonblocking switching unit with a flexible time slot assignment between the IOM-2 and the PCM interface.

The MICO may substitute the EPIC (PEB 2055) or EPIC-S (PEB 2054) in applications that deal with a maximum number of 8 ISDN or 16 analog (8 using the SLICOFI) subscribers connected via one IOM-2 port.

The MICO is fabricated using SIEMENS advanced CMOS technology and is available in a P-DSO-28 package.

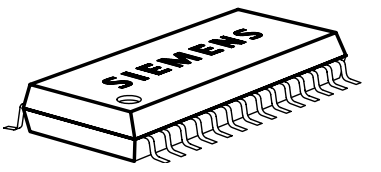
SIEMENS

Mini IOM®-2 Controller MICO

PEF 2015

Data Sheet for the Version 1.1 **CMOS**

1.1 Features



P-DSO-28

Functions

- Interface controller between IOM-2 and PCM for up to 8 ISDN-BA or 16 analog subscribers (up to 8 analog subscribers using the SLICOFI)
- B-channel (64 kbit/s) and D-channel (16 kbit/s) switching
- Configurable Interface (1 port)
  - Configurable for IOM-, SLD- and PCM-applications
  - Programmable clock shift
  - Single or double data clock
- PCM interface (1 port)
  - Freely programmable time slot assignment to up to 128 PCM time slots
  - Tristate control signal for external driver
  - Single or double data clock
- C/I-channel Handler with a 9-Byte FIFO
- Buffered Monitor Handler with a 16-Byte FIFO
- 7-bit hardware timer

General

- Siemens/Intel or Motorola type µP interface
- Supply Voltage: 5 V
- Extended temperature range -40°C to +85°C
- P-DSO-28 package

Type	Package
PEF 2015	P-DSO-28

1.2 Pinning Diagram

(top view)

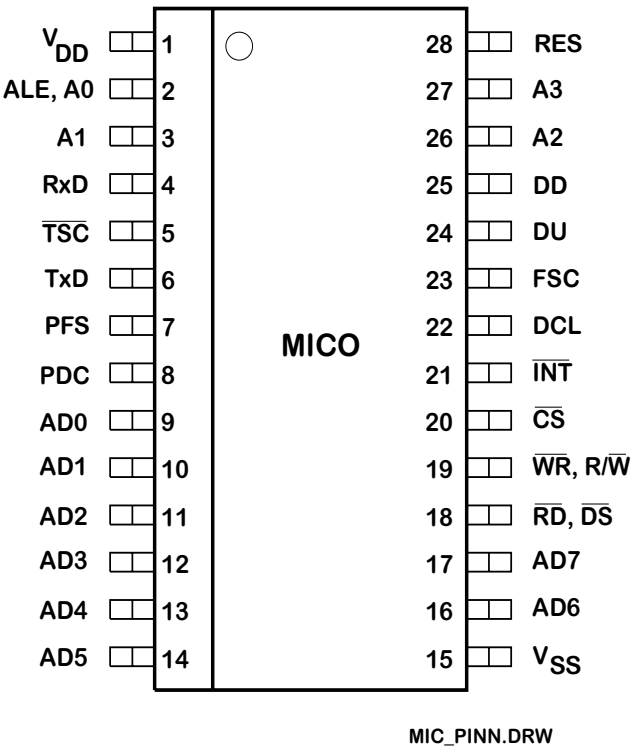


Figure 1 Pinning Diagram

1.3 Pin Description

Pin No.	Symbol	Input (I) Output (O)	Function
23	FSC	I/O	Frame Synchronization Input or output in IOM-configuration. Direction indication in SLD-mode.
22	DCL	I/O	Data Clock Input or output in IOM-configuration. Slave clock in SLD mode. Single or double data rate in IOM-configuration, single data rate in SLD-mode.
24	DU, SIP4	I, I/O (OD)	Data Upstream, Input IOM- or PCM-configuration. Serial Interface Port, SLD configuration.
25	DD, SIP0	O, I/O (OD)	Data Downstream, Output IOM- or PCM-configuration Serial Interface Port, SLD configuration. **Depending on the bit OMDR:COS this line has push-pull or open drain characteristic.** **For unused or unassigned channels or when bit OMDR:CSB is reset the pin is in the state high impedance.**
7	PFS	I	PCM-Interface Frame Synchronization
8	PDC	I	PCM-Interface Data Clock Single or double data rate.
6	TxD	O	Transmit PCM-Interface Data Time-slot oriented data is shifted out of the MICOs upstream data memory on this line. **For time-slots which are flagged in the tristate data memory or when bit OMDR:PSB is reset the pin is set in the state high impedance.**
5	$\overline{\text{TSC}}$	O	Tristate Control Supplies a control signal for an external driver. This line is 'low' when corresponding TxD outputs are valid. During reset this line is high.
4	RxD	I	Receive PCM-Interface Data Time-slot oriented data is received on this pin and forwarded into the downstream data memory of the MICO.

Pin No.	Symbol	Input (I) Output (O)	Function
9 10 11 12 13 14 16 17	AD0, D0 AD1, D1 AD2, D2 AD3, D3 AD4, D4 AD5, D5 AD6, D6 AD7, D7	I/O	Address/Data Bus; multiplexed bus mode. Transfers addresses from the µP to the MICO and data between the µP and the MICO. Data Bus; demultiplexed bus mode. Transfers data between the µP and the MICO. **When driving data the pins have push pull characteristic, otherwise they are in the state high impedance.**
2 3 26 27	A0/ALE A1 A2 A3	I	Address Bus, demultiplexed mode. Transfers addresses from the µP to the MICO. Address Latch Enable, multiplexed mode. ALE controls the on chip address latch in multiplexed bus mode. While ALE is 'high' the latch is transparent. The falling edge latches the current address. *Note: During reset A0 and A1 are evaluated to determine the bus mode.*
18	$\overline{RD}$, $\overline{DS}$	I	Read, active low, Siemens/Intel bus mode. When 'low' a read operation is indicated. Data Strobe, Motorola bus mode. A rising edge marks the end of a read or write operation.
19	$\overline{WR}$, R/$\overline{W}$	I	Write, active low, Siemens/Intel bus mode. When 'low' a write operation is indicated. Read/Write, Motorola bus mode. When 'high' a valid µP access identifies a read operation, when 'low' it identifies a write access.
20	$\overline{CS}$	I	Chip Select, active 'low'. A low on this line selects the MICO for a read/write operation.

Pin No.	Symbol	Input (I) Output (O)	Function
21	$\overline{INT}$	O (OD)	Interrupt, active low. This line is activated when the MICO requests an interrupt. Due to the open drain (OD) characteristic of $\overline{INT}$ multiple interrupt sources can be connected together.
28	RES	I	Reset A 'high' forces the MICO into reset state.
15	V_{SS}	I	Ground (0 V)
1	V_{DD}	I	Supply Voltage (5 V +/- 5%)

1.4 Logic Symbol

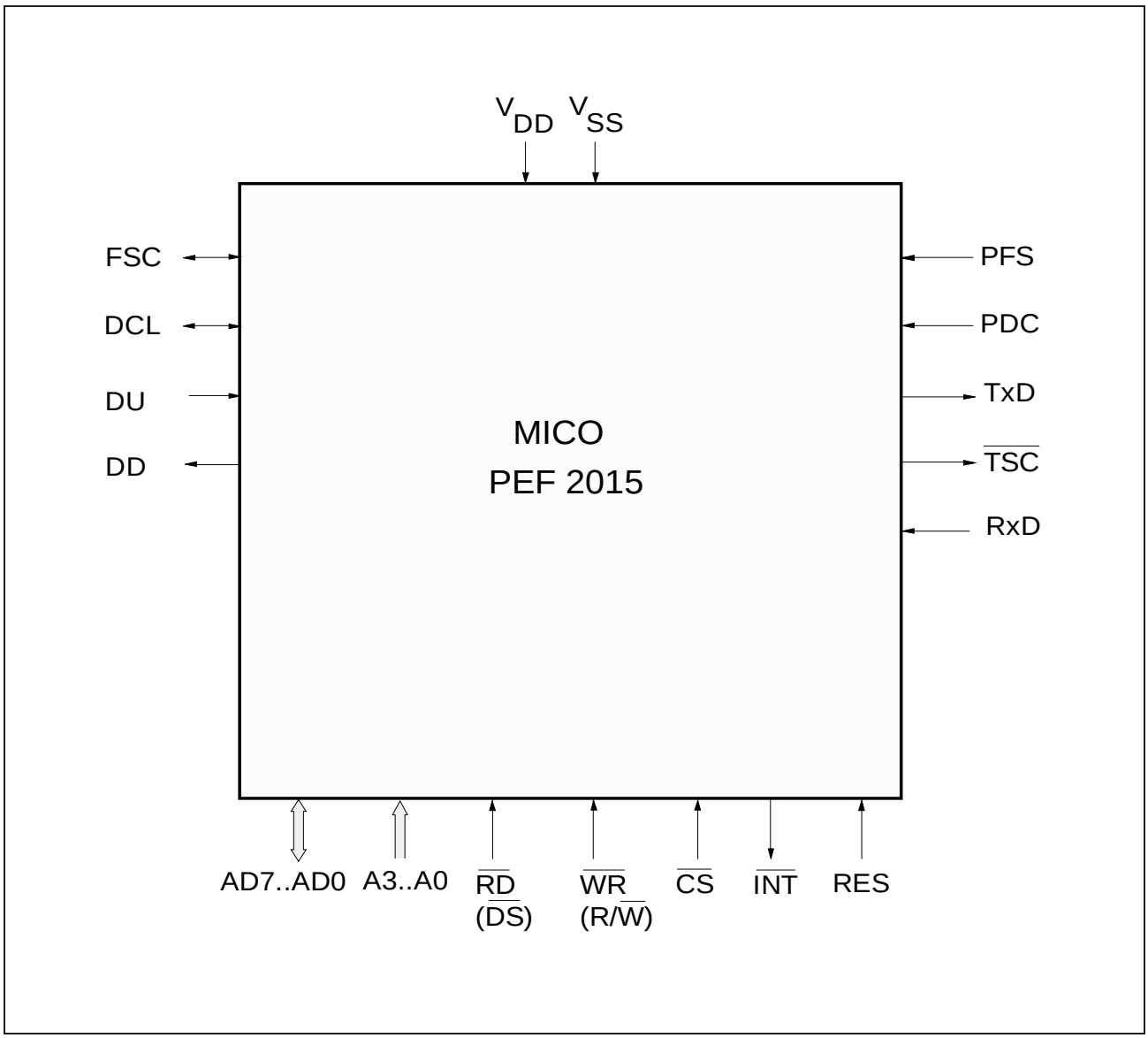


Figure 2 Logic Symbol

1.5 Functional Block Diagram

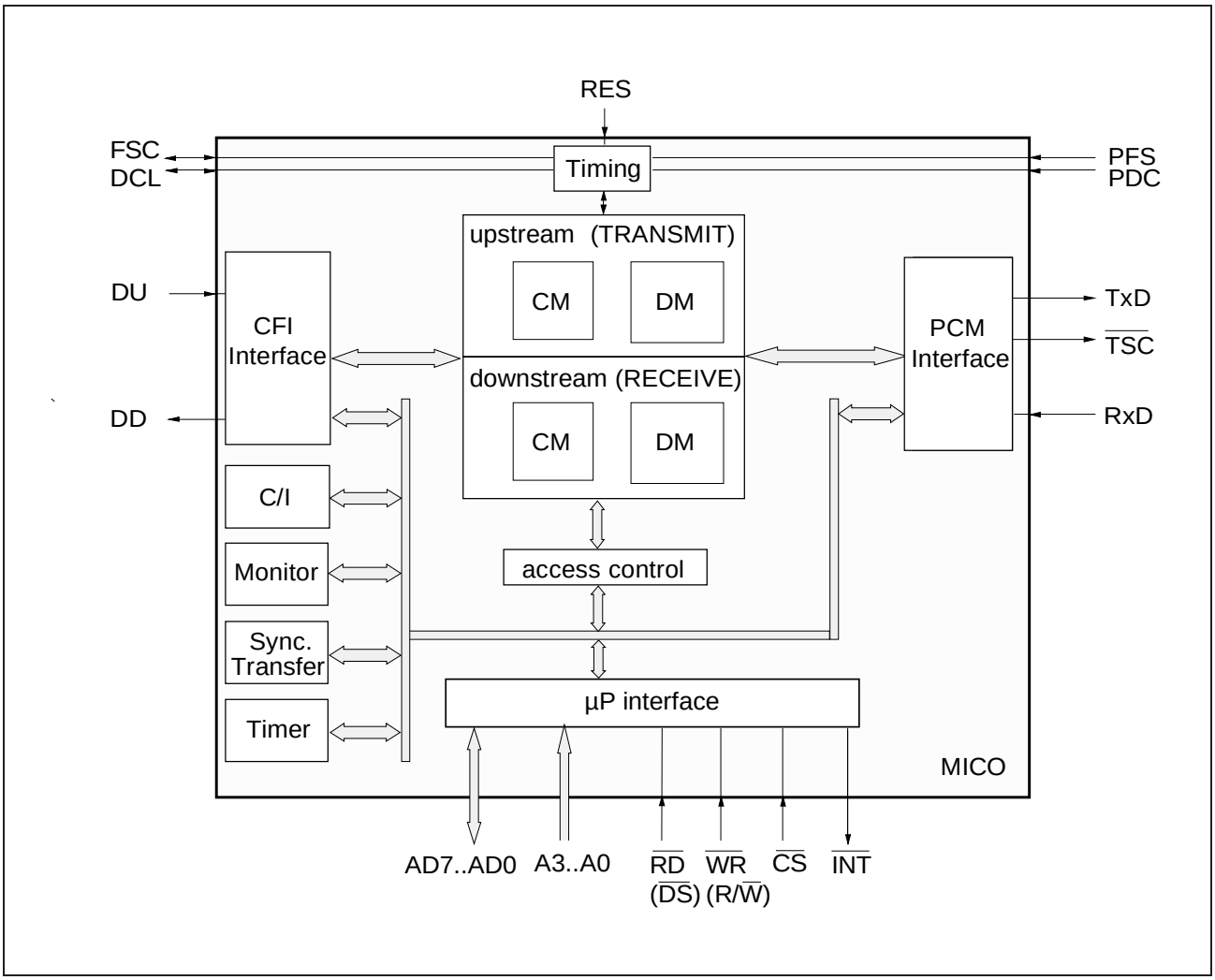


Figure 3 Functional Block Diagram

2 Functional Description

2.1 Configurable Interface CFI

The integrated CFI is a one port serial interface. It comprises two serial data lines (upstream DU and downstream DD), a data clock input or output DCL and a frame sync input or output FSC in IOM-applications. The clock frequency is either equal to the data rate or twice the data rate. The CFI can be configured to data rates up to 8.192 Mbit/s.

The CFI is typically used in IOM-2 or SLD configuration to connect layer-1 devices.

Figure 4 shows the IOM-2 Interface structure in Line Card Mode:

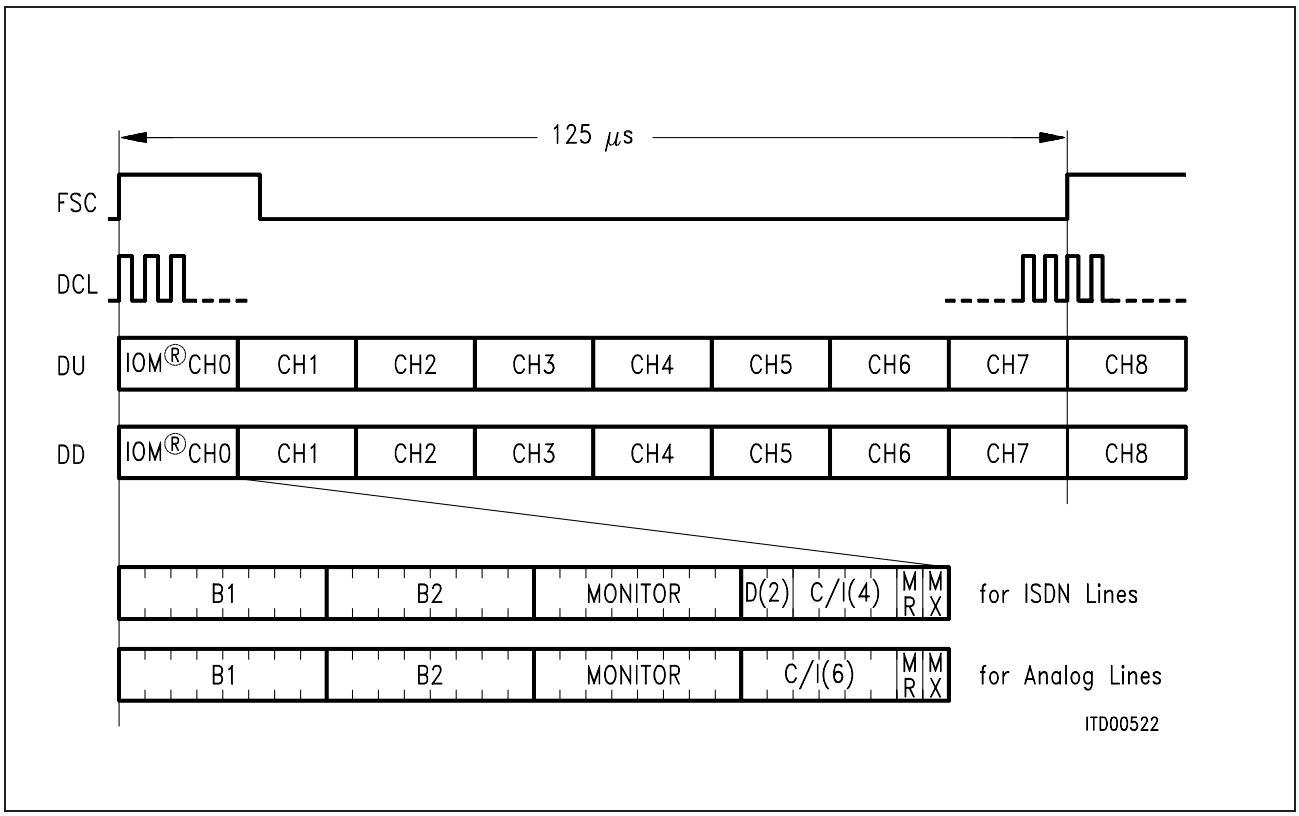


Figure 4 IOM®-2 Frame Structure with 2.048 Mbit/s Data Rate

2.2 Serial PCM Interface

The PCM interface formats the data transmitted or received at the PCM-highways. It consists of one port comprising a data receive (RxD), a data transmit (TxD) and an output tristate indication line ($\overline{\text{TSC}}$). The PCM interface is supplied with a frame signal (PFS) and a PCM clock (PDC).

Data rates up to 8.192 Mbit/s are supported. To properly clock the PCM interface a PDC signal with a frequency equal or twice the data rate has to be applied to the MICO.

2.3 Microprocessor Interface

The MICO supports Siemens/Intel and Motorola type microprocessors. In the Siemens/ Intel type µP interface either a multiplexed or a demultiplexed bus structure may be chosen.

The interface type is selected by pulling up or down two address pins during the reset state (refer to **Table 1, "Selection of Bus Interface," on page 18**). Pulling-up the appropriate pins selects the Motorola type µP interface, fixing them to ground chooses the Siemens/Intel type µP interface mode. In case of a multiplexed Siemens/Intel bus structure address pin A0 takes over the ALE functionality.

The microprocessor interface consists of the following lines:

- Data Bus, 8-bit wide, AD7..AD0
- Address bus, 4-bit wide, A3..A0
- Chip select, $\overline{CS}$
- Two read/write control lines: $\overline{RD}$ and $\overline{WR}$ (Intel mode) or $\overline{DS}$ and R/$\overline{W}$ (Motorola mode)
- Interrupt, $\overline{INT}$
- Reset, RES

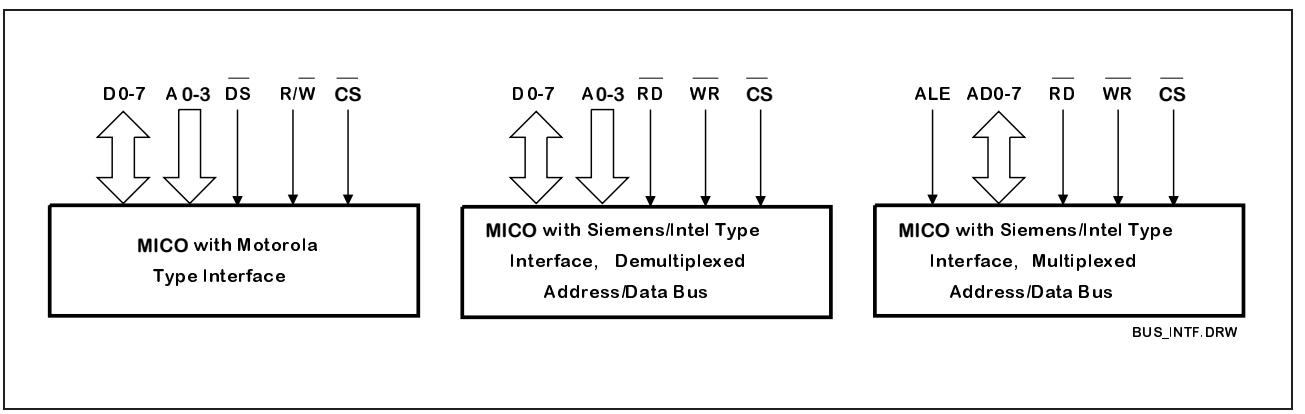


Figure 5 Selectable Bus Interface Structures

2.4 Memory Structure and Switching

The memory block of the MICO performs the switching functionality.
It consists of four sub blocks:

- Upstream data memory
- Downstream data memory
- Upstream control memory
- Downstream control memory.

The PCM-interface reads periodically from the upstream (writes periodically to the downstream) data memory (cyclical access), see **figure 6.**

The CFI reads periodically the control memory and uses the extracted values as a pointers to write to the upstream (read from the downstream) data memory (random

access). In the case of C/I- or signaling channel applications the corresponding data is stored in the control memory. In order to select the application of choice, the control memory provides a code portion.

The control memory is accessible via the µP-interface. In order to establish a connection between CFI time slot A and PCM-interface time slot B, the B-pointer has to be loaded into the control memory location A.

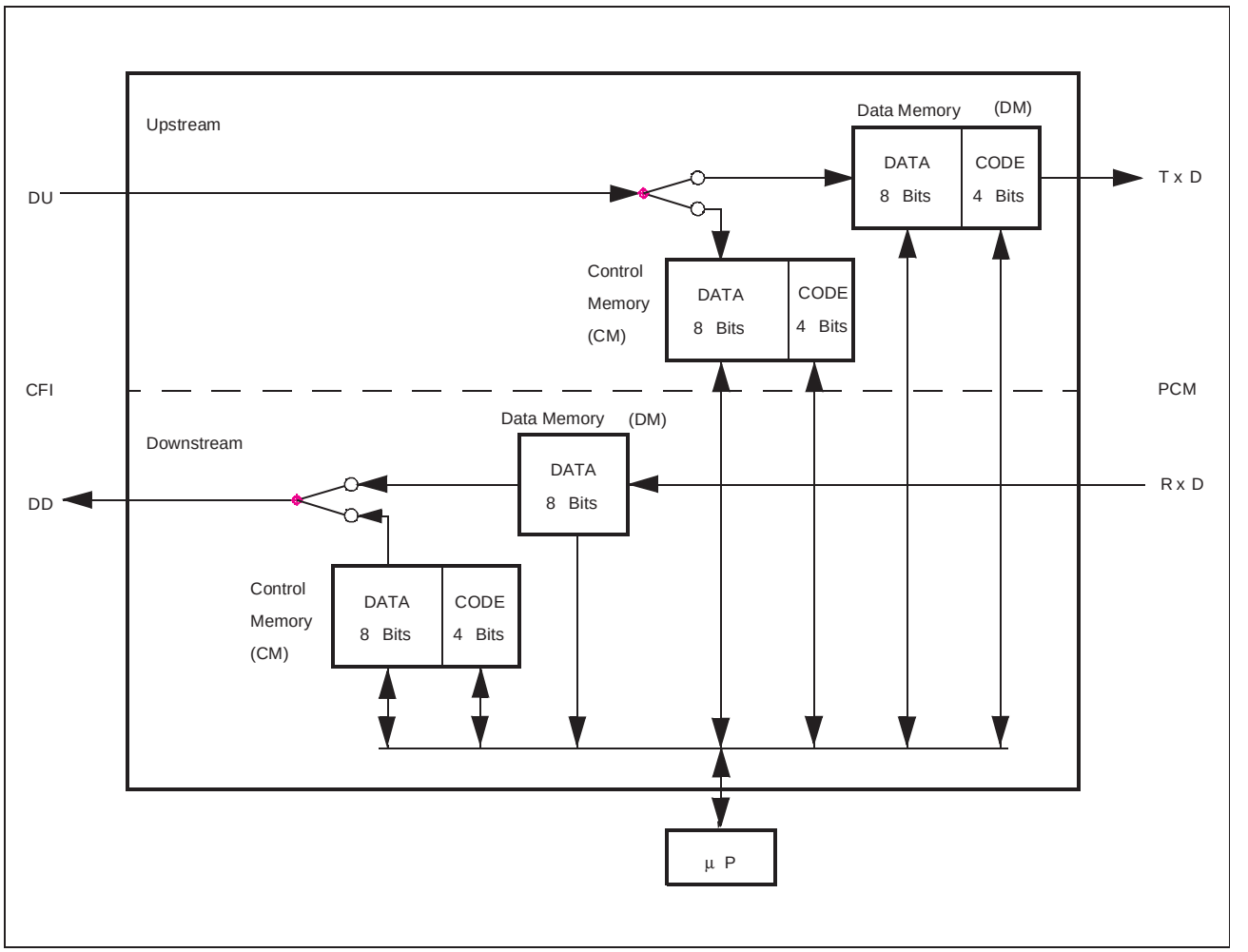


Figure 6 MICO Memory Structure

2.5 Pre-processed Channels, Layer-1 Support

The MICO supports the monitor/feature control and control/signaling channels according to SLD- or IOM-2 interface protocol.

The monitor handler controls the data flow on the monitor/feature control channel either with or without active handshake protocol. To reduce the dynamic load of the CPU a 16-byte transmit/receive FIFO is provided.

The signaling handler supports different schemes (D-channel + C/I-channel, 6-bit signaling, 8-bit signaling).

In downstream direction the relevant content of the control memory is transmitted in the appropriate CFI time slot. In the case of centralized ISDN D-channel handling, a 16-kbit/s D-channel received at the PCM-interface is included.

In upstream direction the signaling handler monitors the received data. Upon a change it generates an interrupt, the channel address is stored in the 9-byte deep C/I FIFO and the actual value is stored in the control memory. In 6-bit and 8-bit signaling schemes a double last look check is provided.

2.6 Special Functions

- Synchronous transfer.
  This utility allows the synchronous µP-access to two independent channels on the PCM- or CFI-interface. Interrupts are generated to indicate the appropriate access windows.
- 7-bit hardware timer.
  The MICO offers one hardware timer. It can be used to cyclically interrupt the CPU, to determine the double last look period or to generate a proper CFI-multiframe synchronization signal.
- Frame length checking.
  The PFS-period is internally checked against the programmed frame length.

3 Operational Description

The MICO, designed as a flexible line-card controller, has the following main applications:

- Digital line cards, with the CFI typically configured as IOM-2, IOM-1 (MUX) or SLD.
- Analog line cards, with the CFI typically configured as IOM-2 or SLD.
- Intelligent NTs, where the MICO's ability to configure the CFI as a PCM interface is utilized.

To operate the MICO the user must be familiar with the device's microprocessor interface, interrupt structure and reset logic.

The device is derived from the EPIC core. With some restrictions it is therefore programmable like the EPIC.

3.1 Microprocessor Interface Operation

The MICO is programmed via an 8-bit parallel interface that can be selected to be

(1) Motorola type, with control signals $\overline{DS}$, R/$\overline{W}$, and $\overline{CS}$.
(2) Siemens / Intel non-multiplexed bus type, with control signals $\overline{WR}$, $\overline{RD}$, and $\overline{CS}$.
(3) Siemens / Intel multiplexed address/data bus type, with control signals ALE, $\overline{WR}$, $\overline{RD}$, and $\overline{CS}$.

The selection is performed via supplying address pins A0 and A1 during reset as follows:

Table 1 Selection of Bus Interface

A1, A0 during reset	Bus Interface
11	Motorola type (1)
00	Siemens / Intel type, non-multiplexed (2)
01 or 10	Siemens / Intel type, multiplexed (3) Pin A0 will take over the ALE functionality

*Note: When selecting the multiplexed bus mode, it has to be ensured that during a MICO device reset the A0/ALE pin receives the appropriate level and no ALE transfers by the µC affect the interface type selection (refer also to figure **18**, page 75).*

When using the Siemens / Intel multiplexed interface, the MICO is addressed with even addresses only (i.e. AD0 always 0), which allows data always to be transferred in the low data byte. This simplifies the use of 16 bit Siemens / Intel type processors.

For a non-multiplexed bus structure the OMDR:RBS bit is needed in addition to the address lines A3..0. OMDR:RBS (Register Bank Selection) selects one of two register banks.

RBS = ’1’ selects a set of registers used for device initialization (e.g. CFI and PCM interface initialization).
RBS = ’0’ switches to a group of registers necessary during operation (e.g. connection programming).

The OMDR register containing the RBS bit can be accessed with either value of RBS.

Interrupts

An interrupt of the MICO is indicated by activating the $\overline{\text{INT}}$-line. The detailed cause of the request can be determined by reading the ISTA register.

The $\overline{\text{INT}}$-output is level active. It stays active until all interrupt sources have been serviced. If a new status bit is set while an interrupt is being serviced, the $\overline{\text{INT}}$ stays active. However, for the duration of a write access to the MASK-register the $\overline{\text{INT}}$-line is deactivated. When using an edge-triggered interrupt controller, it is thus recommended to rewrite the MASK-register at the end of any interrupt service routine.

Every interrupt source can be selectively masked by setting the respective bit of the MASK-register. Such masked interrupts will not be indicated in the ISTA-register, nor will they activate the $\overline{\text{INT}}$-line.

3.2 Clocking

To operate properly, the MICO always requires a PDC-clock.

To synchronize the PCM-side, the MICO should normally also be provided with a PFS-strobe. In most applications, the DCL and FSC will be output signals of the MICO, derived from the PDC via prescalers.

If the required CFI-data rate cannot be derived from the PDC, DCL and FSC can also be programmed as input signals. This is achieved by setting the MICO CMD1:CSS-bit. Frequency and phase of DCL and FSC may then be chosen almost independently of the frequency and phase of PDC and PFS. However, the CFI-clock source **must** still be synchronous to the PCM-interface clock source; i.e. the clock source for the CFI-interface and the clock source for the PCM-interface must be derived from the same master clock.

3.3 Reset

A reset pulse of at least 4 PDC clock cycles has to be applied at the RES pin. The reset pulse sets all registers to their reset values described in **section 4**.

The MICO is now in CM-reset mode (refer to **4.2.6.7**). As the hardware reset does not affect the MICO memories CM and DM, a ’software reset’ of the CM has to be performed.

Subsequently the MICO can be programmed to CM-initialization, normal operation or test mode.
During reset the address pins A0 and A1 are evaluated to determine the bus interface type.

3.4 MICO Operation

The MICO is principally an intelligent switch of PCM-data between two serial interfaces, the system interface (PCM-interface) and the configurable interface (CFI). Up to 128 channels per direction can be switched dynamically between the CFI and the PCM-interfaces. The MICO performs non-blocking space and time switching for these channels which may have a bandwidth of 16, 32, 64 or 128 kbit/s on a per device basis.

Both interfaces can be programmed to operate at different data rates of up to 8.192 Mbit/s. The PCM-interface consists of one duplex port with a tristate control signal. The configurable interface can be selected to provide either one duplex port or two bi-directional (I/O) ports.

The configurable interface incorporates a control block (layer-1 buffer) which allows the µP to gain access to the control channels of an IOM- (ISDN-Oriented Modular) or SLD- (Subscriber Line Data) interface. The MICO can handle the layer-1 functions buffering the C/I and monitor channels for IOM compatible devices and the feature control and signaling channels for SLD compatible devices. The layer-1 and codec devices are connected to the CFI, which is then configured to operate as IOM-2, SLD or multiplexed IOM-1 interface.

The configurable interface of the MICO can also be configured as plain PCM-interface i.e. without IOM- or SLD-frame structure. Since it’s possible to operate the two serial interfaces at different data rates, the MICO can then be used to adapt two different PCM-systems.

The MICO can handle up to 8 ISDN-subscribers with their 2B+D channel structure or up to 16 analog subscribers with their 1B channel structure in IOM-configuration. In SLD-configuration up to 4 analog subscribers can be accommodated.

The system interface is used for the connection to a PCM-back plane. On a typical digital line card, the MICO switches the ISDN B-channels and, if required, also the D-channels to the PCM-back plane. Due to its capability to dynamically switch the 16-kbit/s D-channel, the MICO is one of the fundamental building blocks for networks with either central, decentral or mixed signaling and packet data handling architecture.

3.4.1 PCM-Interface

The serial PCM-interface provides one port consisting of a data transmit (TxD), a data receive (RxD) and a tristate control ($\overline{TSC}$) line. The transmit direction is also referred to as the upstream direction, whereas the receive direction is referred to as the downstream direction.

Data is transmitted and received at normal TTL /CMOS-levels, the output drivers being of the tristate type. Unassigned time slots may either be tristated, or programmed to transmit a defined idle value. The selection of the states "high impedance" and "idle value" can be performed with a two bit resolution. This tristate capability allows several devices to be connected together for concentrator functions. If the output driver

capability of the MICO should prove to be insufficient for a specific application, an external driver controlled by the $\overline{\text{TSC}}$ can be connected.

The **PCM-standby function** makes it possible to switch all PCM-output lines to high impedance with a single command. Internally, the device still works normally. Only the output drivers are switched off.

The number of time slots per 8-kHz frame is programmable in a wide range (from 4 to 128). In other words, the **PCM-data rate can range between 256 kbit/s up to 8.192 Mbit/s**. For time slot encoding refer to **figure 7**.

The number of bits per frame is defined by the **PCM-mode.** There are three PCM-modes.

The timing characteristics at the PCM-interface (data rate, bit shift, etc.) can be varied in a wide range.

The PCM-interface has to be clocked with a **PCM-Data Clock (PDC)** signal having a frequency equal to or twice the selected PCM-data rate. In **single clock rate** operation, a frame consisting of 32 time slots, for example, requires a PDC of 2048 kHz. In **double clock rate** operation, however, the same frame structure would require a PDC of 4096 kHz.

For the synchronization of the time slot structure to an external PCM-system, a **PCM-Framing Signal (PFS)** must be applied. The MICO evaluates the rising PFS edge to reset the internal time slot counters. In order to adapt the PFS-timing to different timing requirements, the MICO can latch the PFS-signal with either the rising or the falling PDC-edge. The PFS-signal defines the position of the first bit of the internal PCM-frame. The actual position of the external upstream and downstream PCM-frames with respect to the framing signal PFS can still be adjusted using the **PCM-offset function** of the MICO. The offset can then be programmed such that PFS marks any bit number of the external frame.

Furthermore it is possible to select either the rising or falling PDC-clock edge for transmitting and sampling the PCM-data.

Usually, the repetition rate of the applied framing pulse PFS is identical to the frame period (125 µs). If this is the case, the **loss of synchronism indication function** can be used to supervise the clock and framing signals for missing or additional clock cycles. The MICO checks the PFS-period internally against the duration expected from the programmed data rate. If, for example, double clock operation with 32 time slots per frame is programmed, the MICO expects 512 clock periods within one PFS-period. The synchronous state is reached after the MICO has detected two consecutive correct frames. The synchronous state is lost if one bad clock cycle is found. The synchronization status (gained or lost) can be read from an internal register and each status change generates an interrupt.

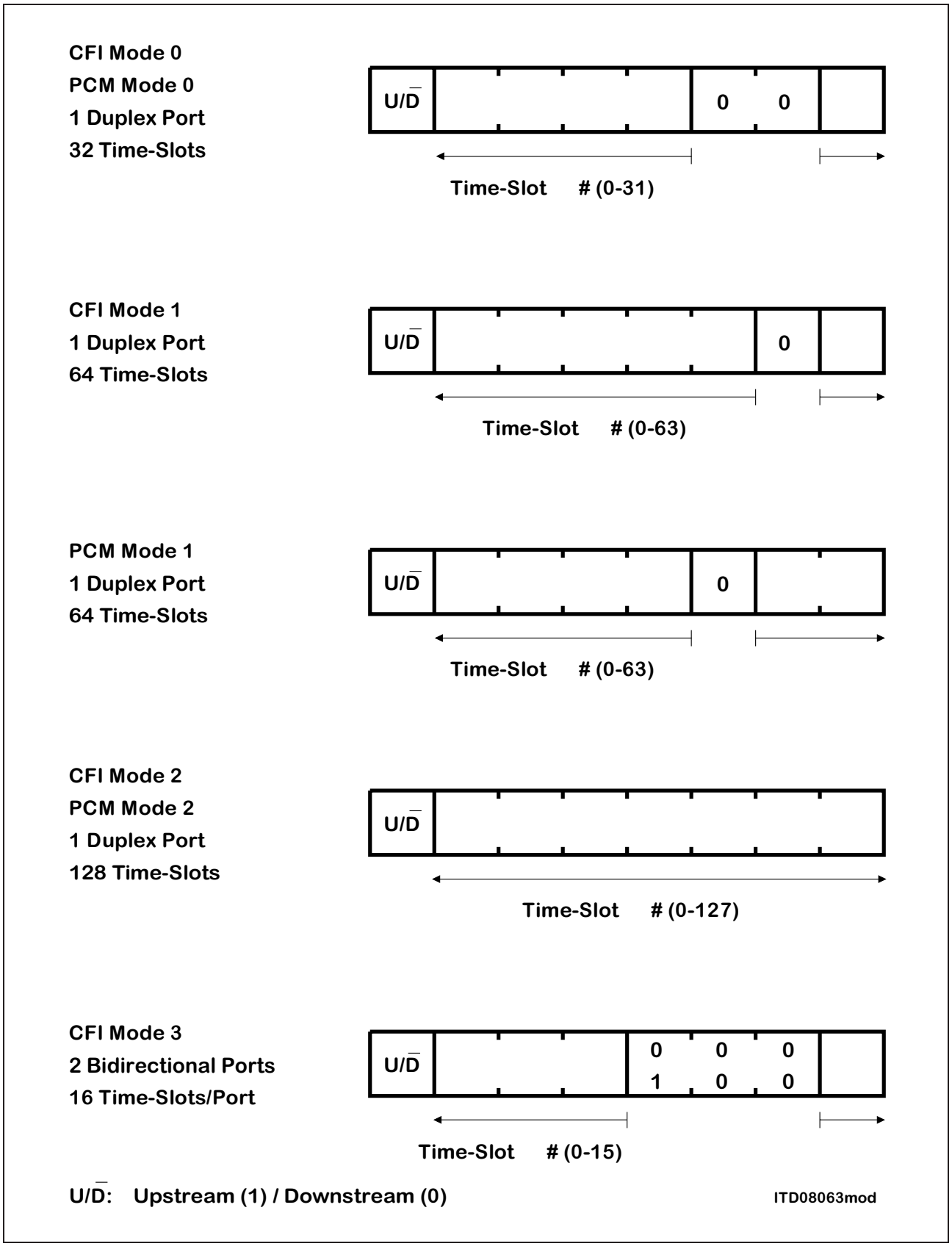


Figure 7 Time Slot Encoding for the Different PCM and CFI Modes

3.4.2 Configurable Interface

The serial configurable interface (CFI) can be operated either in duplex modes or in a bi-directional mode.

In **duplex modes** the MICO provides one port consisting of a data output (DD) and a data input (DU) line. The output pin is called "Data Downstream" pin and the input pin is called "Data Upstream" pin. These modes are especially suited to realize a standard serial PCM-interface (PCM-highway) or to implement an IOM (ISDN-Oriented Modular) interface. The IOM-interface generated by the MICO offers all the functionality like C/I- and monitor channel handling required for operating all kinds of IOM compatible layer-1 and codec devices.

In **bi-directional mode** the MICO provides two bi-directional ports (SIP). Each time slot at any of these ports can individually be programmed as input or output. This mode is mainly intended to realize an SLD-interface (Serial Line Data). In case of an SLD-interface the frame consists of eight time slots where the first four time slots serve as outputs (downstream direction) and the last four serve as inputs (upstream direction). The SLD-interface generated by the MICO offers signaling and feature control channel handling.

Data is transmitted and received at normal TTL/CMOS-levels at the CFI. **Tristate or open-drain output drivers** can be selected. In case of open-drain drivers, external pull-up resistors are required. Unassigned output time slots may be switched to high impedance or be programmed to transmit a defined idle value. The selection between the states "high impedance" or "idle value" can be performed on a per time slot basis.

The **CFI-standby function** switches all CFI-output lines to high impedance with a single command. Internally the device still works normally, only the output drivers are switched off.

The number of time slots per 8-kHz frame is programmable from 2 to 128. In other words, the **CFI-data rate can range between 128 kbit/s up to 8.192 Mbit/s**. Since the MICO offers one CFI-port the number of usable memory locations depends on the selected data rate. In duplex modes port ’0’ has to be programmed, in bi-directional mode I/O port ’0’ and ’4’ have to be programmed. For details refer to **figure 7**.

The timing characteristics at the CFI (data rate, bit shift, etc.) can be varied in a wide range.

The clock and framing signals necessary to operate the configurable interface may be derived either from the clock and framing signals of the PCM-interface (PDC and PFS pins), or may be fed in directly via the DCL- and FSC-pins.

In the first case, the CFI-data rate is obtained by internally dividing down the PCM-clock signal PDC. Several prescaler factors are available to obtain the most commonly used data rates. A CFI reference clock (CRCL) is generated out of the PDC-clock. The PCM-framing signal PFS is used to synchronize the CFI-frame structure. Additionally, the MICO generates clock and framing signals as outputs to operate the connected

subscriber circuits such as layer-1 and codec filter devices. The generated data clock DCL has a frequency equal to or twice the CFI-data rate. The generated framing signal FSC can be chosen from a great variety of types to suit the different applications: IOM-2, multiplexed IOM-1, SLD, etc.

Note that if PFS is selected as the framing signal source, the FSC-signal is an output with a fixed timing relationship with respect to the CFI-data lines. The relationship between FSC and the CFI-frame depends only on the selected FSC-output wave form (CMD2-register). The CFI-offset function shifts both the frame and the FSC-output signal with respect to the PFS-signal.

In the second case, the CFI-data rate is derived from the DCL-clock, which is now used as an input signal. The DCL-clock may also first be divided down by internal prescalers before it serves as the CFI reference clock CRCL and before defining the CFI-data rate. The framing signal FSC is used to synchronize the CFI-frame structure.

3.4.3 Switching Functions

The major tasks of the MICO is to dynamically switch PCM-data between the serial PCM-interface, the serial configurable interface (CFI) and the parallel µP-interface. All possible switching paths are shown in **figure 8**.

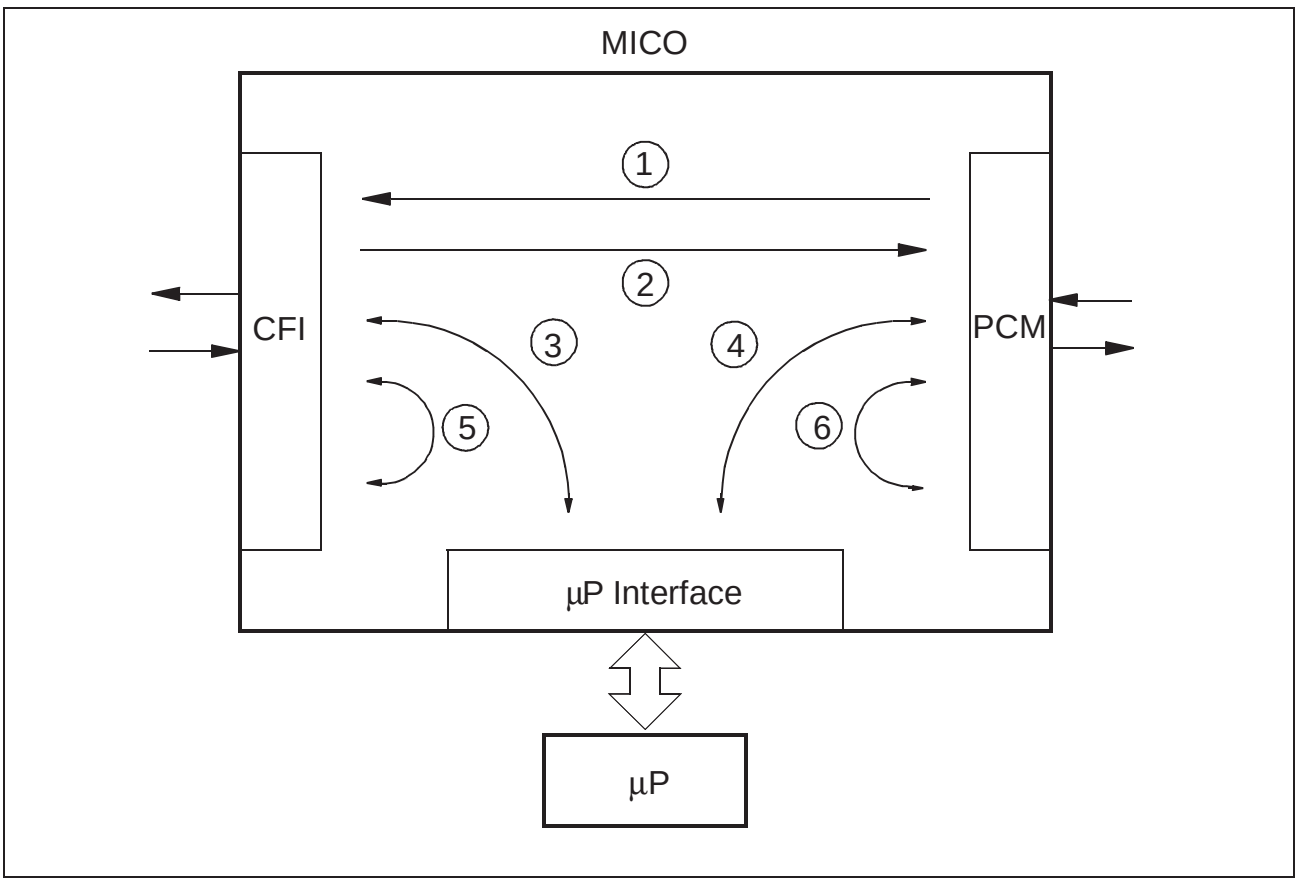


Figure 8 Switching Paths Inside the MICO

Note that the time slot selections in upstream direction are completely independent of the time slot selections in downstream direction.

CFI – PCM Time Slot Assignment

Switching paths 1 and 2 of **figure 8** can be realized for a total number of up to 128 channels per path, i.e. up to 128 time slots in upstream and up to 128 time slots in downstream direction. To establish a connection, the µP writes the addresses of the involved CFI and PCM time slots to the control memory. The actual transfer is then carried out frame by frame without further µP-intervention.

The switching paths 5 and 6 can be realized by programming time slot assignments in the control memory. The total number for such loops is limited to the number of available time slots at the respective opposite interface, i.e. looping back a time slot from CFI to CFI requires a spare upstream PCM time slot and looping back a time slot from PCM to PCM requires a spare downstream and upstream CFI time slot.

Time slot switching is always carried out on 8-bit time slots, the actual position and number of transferred bits can however be limited to 4-bit or 2-bit sub time slots within these 8-bit time slots. On the CFI-side, only one sub time slot per 8-bit time slot can be switched, whereas on the PCM-interface up to 4 independent sub time slots can be switched.

Examples are given in **section 4** of the EPIC Application Manual 10.92.

Sub Time Slot Switching

Sub time slot positions at the PCM-interface can be selected at random, i.e. each single PCM time slot may contain any mixture of 2- and 4-bit sub time slots. A PCM time slot may also contain more than one sub time slot. On the CFI however, two restrictions must be observed:

- Each CFI time slot may contain one and only one sub time slot.
- The sub-slot position for a given bandwidth within the time slot is fixed on a per port basis and therefore on a per device basis.

For more detailed information on sub-channel switching please refer to **chapter 5.2** of the EPIC-1 Application Manual 10.92.

µP-Transfer

Switching paths 3 and 4 of **figure 8** can be realized for all available time slots. Path 3 can be implemented by defining the corresponding CFI time slots as "µP-channels" or as "pre-processed channels".

Each single time slot can individually be declared as **"µP-channel"**. If this is the case, the µP can write a static 8-bit value to a downstream time slot which is then transmitted repeatedly in each frame until a new value is loaded. In upstream direction, the µP can read the received 8-bit value whenever required, no interrupts being generated.

The **"pre-processed channel"** option must always be applied to two consecutive time slots. The first of these time slots must have an even time slot number. If two time-slots are declared as "pre-processed channels", the first one can be accessed by the monitor/ feature control handler, which gives access to the frame via a 16-byte FIFO. Although this function is mainly intended for IOM- or SLD-applications, it could also be used to transmit or receive a "burst" of data to or from a 64-kbit/s channel. The second pre-processed time slot, the odd one, is also accessed by the µP. In downstream direction a 4-, 6- or 8-bit static value can be transmitted. In upstream direction the received 8-bit value can be read. Additionally, a change detection mechanism will generate an interrupt upon a change in any of the selected 4, 6 or 8 bits.

Pre-processed channels are usually programmed after Control Memory (CM) reset during device initialization. Resetting the CM sets all CFI time slots to unassigned channels (CM code '0000'). Of course, pre-processed channels can also be initialized or re-initialized in the operational phase of the device.

To program a pair of pre-processed channels the correct code for the selected handling scheme must be written to the CM. **Figure 9** gives an overview of the available pre-processing codes and their application. For further detail, please refer to **chapter 5.5** of the EPIC User's Manual 02.97.

DD Application	Even Control Memory Address MAAR = 0.....0 Code Field MACR = 0111... / Data Field MADR = ...	Odd Control Memory Address MAAR = 0.....1 Code Field MACR = 0111... / Data Field MADR = ...	Output at the Configurable Interface Downstream Preprocessed Channels Even Time-Slot / Odd Time-Slot
Decentral D Channel Handling	1 0 0 0 | 1 1 | C/I | 1 1	1 0 1 1 | X X X X X X X X	m m m m m m m m | - - | C/I | m m Monitor Channel / Control Channel
Central D Channel Handling	1 0 1 0 | 1 1 | C/I | 1 1	PCM Code for a 2Bit Sub. Time-Slot | Pointer to a PCM Time-Slot	m m m m m m m m | D D | C/I | m m Monitor Channel / Control Channel
6 Bit Signaling (e.g. analog IOM®)	1 0 1 0 | SIG | 1 1	1 0 1 1 | X X X X X X X X	m m m m m m m m | SIG | m m Monitor Channel / Control Channel
8 Bit Signaling (e.g. SLD)	1 0 1 0 | SIG	1 0 1 1 | X X X X X X X X	m m m m m m m m | SIG Feature Control Channel / Signaling Channel

DU Application	Even Control Memory Address MAAR = 1.....0 Code Field MACR = 0111... / Data Field MADR = ...	Odd Control Memory Address MAAR = 1.....1 Code Field MACR = 0111... / Data Field MADR = ...	Input from the Configurable Interface Upstream Preprocessed Channels Even Time-Slot / Odd Time-Slot
Decentral D Channel Handling	1 0 0 0 | 1 1 | C/I | 1 1	0 0 0 0 | X X X X X X X X	m m m m m m m m | - - | C/I | m m Monitor Channel / Control Channel
Central D Channel Handling	1 0 0 0 | 1 1 | C/I | 1 1	PCM Code for a 2Bit Sub. Time-Slot | Pointer to a PCM Time-Slot	m m m m m m m m | D D | C/I | m m Monitor Channel / Control Channel
6 Bit Signaling (e.g. analog IOM®)	1 0 1 0 | SIG Actual Value | X X	1 0 1 0 | SIG Stable Value | X X	m m m m m m m m | SIG | m m Monitor Channel / Control Channel
8 Bit Signaling (e.g. SLD)	1 0 1 1 | SIG Actual Value	1 0 1 1 | SIG Stable Value	m m m m m m m m | SIG Feature Control Channel / Signaling Channel

m : Monitor channel bits, these bits are treated by the monitor/feature control handler

\- : Inactive sub. time-slot, in downstream direction these bits are tristated (OMDR:COS = 0) or set to logical 1 (OMDR:COS = 1)

C/I : Command/Indication channel, these bits are exchanged between the CFI in/output and the CM data field. A change of the C/I bits in upstream direction causes an interrupt (ISTA : SFI). The address of the change is stored in the CIFIFO

D : D channel, these D channel bits are transparently switched to and from the PCM interface,

SIG actual value / stable value : Signaling Channel, these bits are exchanged between the CFI in/output and the CM data field. The SIG value which was present in the last frame is stored as the actual value in the even address CM location. The stable value is updated if a valid change in the actual value has been detected according to the last look algorithm. A change of the SIG stable value in upstream direction causes an interrupt (ISTA : CFI). The address of the change is stored in the CIFIFO.

ITD05846

Figure 9 Pre-processed Channel Codes

Synchronous Transfer

For two channels, all switching paths of **figure 8** can also be realized using Synchronous Transfer. The working principle is that the µP specifies an input time slot (source) and an output time slot (destination). Both source and destination time slots can be selected independently from each other at either the PCM- or CFI-interfaces. In each frame, the MICO first transfers the serial data from the source time slot to an internal data register from where it can be read and if required overwritten or modified by the µP. This data is then fed forward to the destination time slot.

Chapter 8 of the EPIC Application Manual 10.92 provides examples of such transfers.

3.4.4 Special Functions

Hardware Timer

The MICO provides one hardware timer which continuously interrupts the µP after a programmable time period. The timer period can be selected in the range of 250 µs up to 32 ms in multiples of 250 µs. Beside the interrupt generation, the timer can also be used to determine the last look period for 6 and 8-bit signaling channels on IOM-2 and SLD-interfaces and for the generation of an FSC-multiframe signal (see **chapter 9.1** of the EPIC Application Manual 10.92).

Power and Clock Supply Supervision

The Connection Memory CM is supervised to data falsfication due to clock or power failure. If such an inappropriate clocking or power failure occurs, the µP is requested to reinitialize the device.

3.5 Initialization Procedure

For proper initialization of the MICO the following procedure is recommended:

3.5.1 Hardware Reset

A reset pulse can be applied at the RES-pin for at least 4 PDC-clock cycles. The reset pulse sets all registers to their reset values (refer to **section 4.1**).
Note that in this state DCL and FSC do not deliver any clock signals.

3.5.2 MICO Initialization

3.5.2.1 Register Initialization

The PCM- and CFI-configuration registers (PMOD, PBNR, …, CMD1, CMD2, …) should be programmed to the values required for the application. The correct setting of the PCM- and CFI-registers is important in order to obtain a reference clock (RCL) which is consistent with the externally applied clock signals.
The state of the operation mode (OMDR:OMS1..0 bits) does not matter for this programming step.

PMOD	=	PCM-mode, timing characteristics, etc.
PBNR	=	Number of bits per PCM-frame
POFD	=	PCM-offset downstream
POFU	=	PCM-offset upstream
PCSR	=	PCM-timing
CMD1	=	CFI-mode, timing characteristics, etc.
CMD2	=	CFI-timing
CBNR	=	Number of bits per CFI-frame
CTAR	=	CFI-offset (time slots)
CBSR	=	CFI-offset (bits)
CSCR	=	CFI-sub channel positions

3.5.2.2 Control Memory Reset

Since the hardware reset does not affect the MICO memories (Control and Data Memories), it is mandatory to perform a "software reset" of the CM. The CM-code '0000' (unassigned channel) should be written to each location of the CM. The data written to the CM-data field is then don't care, e.g. FF_H.

OMDR:OMS1..0 must be to $'00'_B$ for this procedure (reset value).

MADR = FF_H
MACR = 70_H
Wait for STAR:MAC = 0

The resetting of the complete CM takes 256 RCL-clock cycles. During this time, the STAR:MAC-bit is set to logical 1.

3.5.2.3 Initialization of Pre-processed Channels

After the CM-reset, all CFI time slots are unassigned. If the CFI is used as a plain PCM-interface, i.e. containing only switched channels (B-channels), the initialization steps below are not required. The initialization of pre-processed channels applies only to IOM- or SLD-applications.

An IOM- or SLD-"channel" consists of four consecutive time slots. The first two time slots, the B-channels need not be initialized since they are already set to unassigned channels by the CM-reset command. Later, in the application phase of the software, the B-channels can be dynamically switched according to system requirements. The last two time slots of such an IOM- or SLD-channel, the pre-processed channels must be initialized for the desired functionality. There are four options that can be selected:

Table 2 Pre-Processed Channel Options at the CFI

Even CFI Time Slot	Odd CFI Time Slot	Main Application
Monitor/feature control channel	4-bit C/I-channel, D-channel not switched (decentral D-channel handling)	IOM-1 or IOM-2 digital subscriber
Monitor/feature control channel	4-bit C/I-channel, D-channel switched (central D-ch. handling)	IOM-1 or IOM-2 digital subscriber
Monitor/feature control channel	6-bit SIG-channel	IOM-2, analog subscriber
Monitor/feature control channel	8-bit SIG/channel	SLD, analog subscriber

Also refer to **figure 9**.

Example

In CFI-mode 0 the CFI-port shall be initialized as IOM-2 port with a 4-bit C/I-field.

CFI time slots 0, 1, 4, 5, 8, 9 … 28, 29 are B-channels and need not to be initialized.

CFI time slots 2, 3, 6, 7, 10, 11, …, 30, 31 are pre-processed channels and need to be initialized:

CFI-port, time slot 2 (even), downstream

MADR = FF_H ; the C/I-value '1111' will be transmitted upon CFI-activation
MAAR = 08_H ; addresses ts 2 down
MACR = $7A_H$; CM-code '1010'
Wait for STAR:MAC = 0

CFI-port, time slot 3 (odd), downstream

MADR = FF_H ; don't care
MAAR = 09_H ; addresses ts 3 down
MACR = $7B_H$; CM-code '1011'
Wait for STAR:MAC = 0

CFI-port, time slot 2 (even), upstream

MADR = FF_H ; the C/I-value '1111' is expected upon CFI-activation
MAAR = 88_H ; address ts 2 up
MACR = 78_H ; CM-code '1000'
Wait for STAR:MAC = 0

CFI-port, time slot 3 (odd), upstream

MADR = FF_H ; don't care
MAAR = 89_H ; address ts 3 up
MACR = 70_H ; CM-code '0000'
Wait for STAR:MAC = 0

Repeat the above programming steps for the remaining CFI-time slots.

This procedure can be speeded up by selecting the CM-initialization mode (OMDR:OMS1..0=10). If this selection is made, the access time to a single memory location is reduced to 2.5 RCL-cycles. The complete initialization time for 8 IOM-2 channels is then reduced to $32 \times 0.61\ \mu s = 19{,}5\ \mu s$

3.5.2.4 Initialization of the Upstream Data Memory (DM) Tristate Field

For each PCM time slot the tristate field defines whether the contents of the DM-data field are to be transmitted (low impedance), or whether the PCM time slot shall be set to high impedance. The content of the tristate field is not modified by a hardware reset. In order to have all PCM time slots set to high impedance upon the activation of the PCM-interface, each location of the tristate field must be loaded with the value '0000'. For this purpose, the "tristate reset" command can be used:

OMDR = $C0_H$; OMS1..0 = 11, normal mode
MADR = $0\mathbf{0}_H$; code field value $'0000'_B$
MACR = 68_H ; MOC-code to initialize all tristate locations (1101_B)
Wait for STAR:MAC = 0

The initialization of the complete tristate field takes 1035 RCL-cycles.

Note: It is also possible to program the value '1111' to the tristate field in order to have all time slots switched to low impedance upon the activation of the PCM-interface.

Note: While OMDR:PSB = 0, all PCM-output drivers are set to high impedance, regardless of the values written to the tristate field.

3.5.3 Activation of the PCM- and CFI-Interfaces

With the MICO configured to the system requirements, the PCM- and CFI-interface can be switched to the operational mode.

The OMDR:OMS1..0 bits must be set (if this has not already be done) to the normal operation mode (OMS1..0 = 11). When doing this, the PCM-framing interrupt (ISTA:PFI) will be enabled. If the applied clock and framing signals are in accordance with the values programmed to the PCM-registers, the PFI-interrupt will be generated (if not masked). When reading the status register, the STAR:PSS-bit will be set to logical 1.

To enable the PCM-output drivers set OMDR:PSB = 1. The CFI-interface is activated by programming OMDR:CSB = 1. This enables the output clock and framing signals (DCL and FSC), if these have been programmed as outputs. It also enables the CFI-output drivers. The output driver type can be selected between "open drain" and "tristate" with the OMDR:COS-bit.

Example: Activation of the MICO for a typical IOM-2 application:

OMDR = EE_H; Normal operation mode (OMS1..0 = 11)
PCM-interface active (PSB = 1)
PCM-test loop disabled (PTL = 0)
CFI-output drivers: open drain (COS = 1)
Monitor handshake protocol selected (MFPS = 1)
CFI active (CSB = 1)
Access to MICO registers via address pins A3..A0, used in demultiplexed mode only, normal operation (RBS = 0)

4 Registers Summary

4.1 Register Address Arrangement

Group	Reg Name	Access	Address mux AD7..0	Address demux OMDR:RBS/ A3..0	Reset Value	Comment	refer to page
1. MICO PCM	PMOD	RD/WR	20_H	$1/0_H$	00_H	PCM-mode reg.	35
	PBNR	RD/WR	22_H	$1/1_H$	FF_H	PCM-bit number reg.	36
	POFD	RD/WR	24_H	$1/2_H$	00_H	PCM-offset downstream reg.	36
	POFU	RD/WR	26_H	$1/3_H$	00_H	PCM-offset upstream reg.	37
	PCSR	RD/WR	28_H	$1/4_H$	00_H	PCM-clock shift reg.	38
	PICM	RD	$2A_H$	$1/5_H$	xx_H	dummy	38
2. MICO CFI	CMD1	RD/WR	$2C_H$	$1/6_H$	00_H	CFI-mode reg. 1	39
	CMD2	RD/WR	$2E_H$	$1/7_H$	00_H	CFI-mode reg. 2	41
	CBNR	RD/WR	30_H	$1/8_H$	FF_H	CFI-bit number reg.	44
	CTAR	RD/WR	32_H	$1/9_H$	00_H	CFI time slot adjustment reg.	44
	CBSR	RD/WR	34_H	$1/A_H$	00_H	CFI-bit shift reg.	45
	CSCR	RD/WR	36_H	$1/B_H$	00_H	CFI-subchannel reg.	47
3. MICO memory access	MACR	RD/WR	00_H	$0/0_H$	xx_H	memory access control reg.	48
	MAAR	RD/WR	02_H	$0/1_H$	xx_H	memory access address reg.	52
	MADR	RD/WR	04_H	$0/2_H$	xx_H	memory access data reg.	53

Registers Summary

Group	Reg Name	Access	Address mux AD7..0	Address demux OMDR:RBS/ A3..0	Reset Value	Comment	refer to page
4. MICO synchro nous transfer	STDA	RD/WR	06_H	$0/3_H$	xx_H	synchron transfer data reg. A	54
	STDB	RD/WR	08_H	$0/4_H$	xx_H	synchron transfer data reg. B	54
	SARA	RD/WR	$0A_H$	$0/5_H$	xx_H	synchron transfer receive address reg. A	55
	SARB	RD/WR	$0C_H$	$0/6_H$	xx_H	synchron transfer receive address reg. B	56
	SAXA	RD/WR	$0E_H$	$0/7_H$	xx_H	synchron transfer transmit address reg. A	56
	SAXB	RD/WR	10_H	$0/8_H$	xx_H	synchron transfer transmit address reg. B	57
	STCR	RD/WR	12_H	$0/9_H$	00xxxx xx	synchron transfer control reg.	57
5. MICO monitor/ feature control	MFAIR	RD	14_H	$0/A_H$	00xxxx xx	MF-channel active indication reg.	58
	MFSAR	WR	14_H	$0/A_H$	00_H	MF-channel subscriber address reg.	59
	MFFIFO	RD/WR	16_H	$0/B_H$	xx_H	MF-channel FIFO	60
6. MICO status/ control	CIFIFO	RD	18_H	$0/C_H$	0xxxxx xx	signaling channel FIFO	60
	TIMR	WR	18_H	$0/C_H$	00_H	timer reg.	61
	STAR	RD	$1A_H$	$0/D_H$	05_H	status register	62
	CMDR	WR	$1A_H$	$0/D_H$	00_H	command reg.	63
	ISTA	RD	$1C_H$	$0/E_H$	00_H	interrupt status	65
	MASK	WR	$1C_H$	$0/E_H$	04_H	mask register	66
	OMDR	RD/WR	$1E_H$ $3E_H$	x/F_H	00_H	operation mode reg.	67
	VNSR	RD	$3A_H$	$1/D_H$	02_H	version number status register	69

4.2 Detailed Register Description

Unused bits and registers are accessible as described below to facilitate software portation from existing EPIC designs. They have to be programmed to the specified values. Writing other than the specified values may cause undefined behaviour.

4.2.1 PCM-Interface Registers

4.2.1.1 PCM-Mode Register (PMOD)

Access in demultiplexed µP-interface mode: read/write address: 0_H, OMDR:RBS = 1

Access in multiplexed µP-interface mode: read/write address: 20_H

Reset value: 00_H

bit 7 bit 0

PMD1	PMD0	PCR	PSM	0	0	0	0

PMD1..0 PCM-Mode. Defines the actual number of PCM-ports, the data rate range and the data rate stepping.

PMD1..0	PCM-Mode	Data Rate [kbit/s]		Data Rate Stepping [kbit/s]
		min.	max.	
00	0	256	2048	256
01	1	512	4096	512
10	2	1024	8192	1024

PCR PCM-Clock Rate.

0… single clock rate, data rate is identical with the clock frequency supplied on pin PDC.

1… double clock rate, data rate is half the clock frequency supplied on pin PDC.

Note: Only single clock rate is allowed in PCM-mode 2!

PSM PCM Synchronization Mode.

A rising edge on PFS synchronizes the PCM-frame. PFS is not evaluated directly but is sampled with PDC.

0… the external PFS is evaluated with the falling edge of PDC. The internal PFS (internal frame start) occurs with the next rising edge of PDC.

1… the external PFS is evaluated with the rising edge of PDC. The internal PFS (internal frame start) occurs with this rising edge of PDC.

4.2.1.2 Bit Number per PCM-Frame (PBNR)

Access in demultiplexed µP-interface mode: read/write address: 1_H OMDR:RBS = 1
Access in multiplexed µP-interface mode: read/write address: 22_H
Reset value: FF_H

bit 7 bit 0

BNF7	BNF6	BNF5	BNF4	BNF3	BNF2	BNF1	BNF0

BNF7..0 Bit Number per PCM Frame.
PCM-mode 0: BNF7..0 = number of bits – 1
PCM-mode 1: BNF7..0 = (number of bits – 2) / 2
PCM-mode 2: BNF7..0 = (number of bits – 4) / 4

The value programmed in PBNR is also used to check the PFS-period.

4.2.1.3 PCM-Offset Downstream Register (POFD)

Access in demultiplexed µP-interface mode: read/write address: 2_H OMDR:RBS = 1
Access in multiplexed µP-interface mode: read/write address: 24_H
Reset value: 00_H

bit 7 bit 0

OFD9	OFD8	OFD7	OFD6	OFD5	OFD4	OFD3	OFD2

OFD9..2 Offset Downstream bit 9…2.
These bits together with PCSR:OFD1**..**0 determine the offset of the PCM-frame in downstream direction. The following formulas apply for calculating the required register value. BND is the bit number in downstream direction marked by the rising internal PFS-edge. BPF denotes the actual number of bits constituting a frame.

PCM-mode 0: OFD9..2 = mod_{BPF} (BND – 17 + BPF)
PCSR:OFD1..0 = 0
PCM-mode 1: PFD9..1 = mod_{BPF} (BND – 33 + BPF)
PCSR: PFD0 = 0
PCM-mode 2: OFD9..0 = mod_{BPF} (BND – 65 + BPF)

4.2.1.4 PCM-Offset Upstream Register (POFU)

Access in demultiplexed µP-interface mode: read/write address: 3_H OMDR:RBS = 1

Access in multiplexed µP-interface mode: read/write address: 26_H

Reset value: 00_H

bit 7							bit 0
OFU9	OFU8	OFU7	OFU6	OFU5	OFU4	OFU3	OFU2

OFU9..2 Offset Upstream bit 9…2.
These bits together with PCSR:OFU1**..**0 determine the offset of the PCM-frame in upstream direction. The following formulas apply for calculating the required register value. BNU is the bit number in upstream direction marked by the rising internal PFS-edge. BPF denotes the actual number of bits constituting a frame.

PCM-mode 0: OFU9..2 = mod_{BPF} (BNU + 23)
PCSR:OFU1..00 = 0

PCM-mode 1: OFU9..1 = mod_{BPF} (BNU + 47)
PCSR:OFU0 = 0

PCM-mode 2: OFU9..0 = mod_{BPF} (BNU + 95)

4.2.1.5 PCM-Clock Shift Register (PCSR)

Access in demultiplexed µP-interface mode: read/write address: 4_H OMDR:RBS = 1
Access in multiplexed µP-interface mode: read/write address: 28_H
Reset value: 00_H

bit 7							bit 0
DRCS	OFD1	OFD0	DRE	ADSRO	OFU1	OFU0	URE

DRCS Double Rate Clock Shift.
0...the PCM-input and output data are not delayed
1...the PCM-input and output data are delayed by one PDC-clock cycle

OFD1..0 Offset Downstream bits 1…0, **see POFD-register**.

DRE Downstream Rising Edge.
0…the PCM-data is sampled with the falling edge of PDC
1…the PCM-data is sampled with the rising edge of PDC

ADSRO Add Shift Register on Output.
0...the PCM-output data are not delayed
1...the PCM-output data are delayed by one PDC-clock cycle.

Note: If both DRCS and ADSRO are set to logical 1, the PCM-output data are delayed by two PDC-clock cycles.

OFU1..0 Offset Upstream bits 1…0, **see POFU-register**.

URE Upstream Rising Edge.
0…the PCM-data is transmitted with the falling edge of PDC
1…the PCM-data is transmitted with the rising edge of PDC

4.2.1.6 PCM-Input Comparison Mismatch Register (PICM)

Access in demultiplexed µP-interface mode: read address: 5_H OMDR:RBS = 1
Access in multiplexed µP-interface mode: read address: $2A_H$
Reset value: xx_H

Note: This register does not provide valid values for operation. It is a dummy register to facilitate software portation from the EPIC to the MICO.

4.2.2 Configurable Interface Registers

4.2.2.1 Configurable Interface Mode Register 1 (CMD1)

Access in demultiplexed µP-interface mode: read/write address: 6_H OMDR:RBS = 1

Access in multiplexed µP-interface mode: read/write address: $2C_H$

Reset value: 00_H

bit 7							bit 0
CSS	CSM	CSP1	CSP0	CMD1	CMD0	0	0

CSS Clock Source Selection.
0…PDC and PFS are used as clock and framing source for the CFI. Clock and framing signals derived from these sources are output on DCL and FSC.
1…DCL and FSC are selected as clock and framing source for the CFI.

CSM CFI-Synchronization Mode.
The rising FSC-edge synchronizes the CFI-frame.
0…FSC is evaluated with every falling edge of DCL.
1…FSC is evaluated with every rising edge of DCL.

Note: If CSS = 0 is selected, CSM and PMOD:PSM must be programmed identical.

CSP1..0 Clock Source Prescaler 1,0.
The clock source frequency is divided according to the following table to obtain the CFI-reference clock CRCL (refer to **figures 10 and 11**).

CSP1,0	**Prescaler Divisor**
00	2
01	1.5
10	1
11	not allowed

CMD1..0 CFI-Mode1,0.
Defines the actual configuration of the CFI-port.

CMD1..0	CFI Mode	CFI-Data Rate [kbit/s]		Min. Required CFI-Data Rate [kbit/s] Relative to PCM-Data Rate	Necessary Reference Clock (RCL)	DCL-Output Frequencies CMD1:CSS = 0
		min.	max.			
00	0	128	2048	32N/3	2xDR	DR, 2xDR
01	1	128	4096	64N/3	DR	DR
10	2	128	8192	64N/3	0.5xDR	DR
11	3	128	1024	16N/3	4xDR	DR, 2xDR

where N = number of time slots in a PCM-frame

*Note: For time slot encoding refer to **figure 7**.*

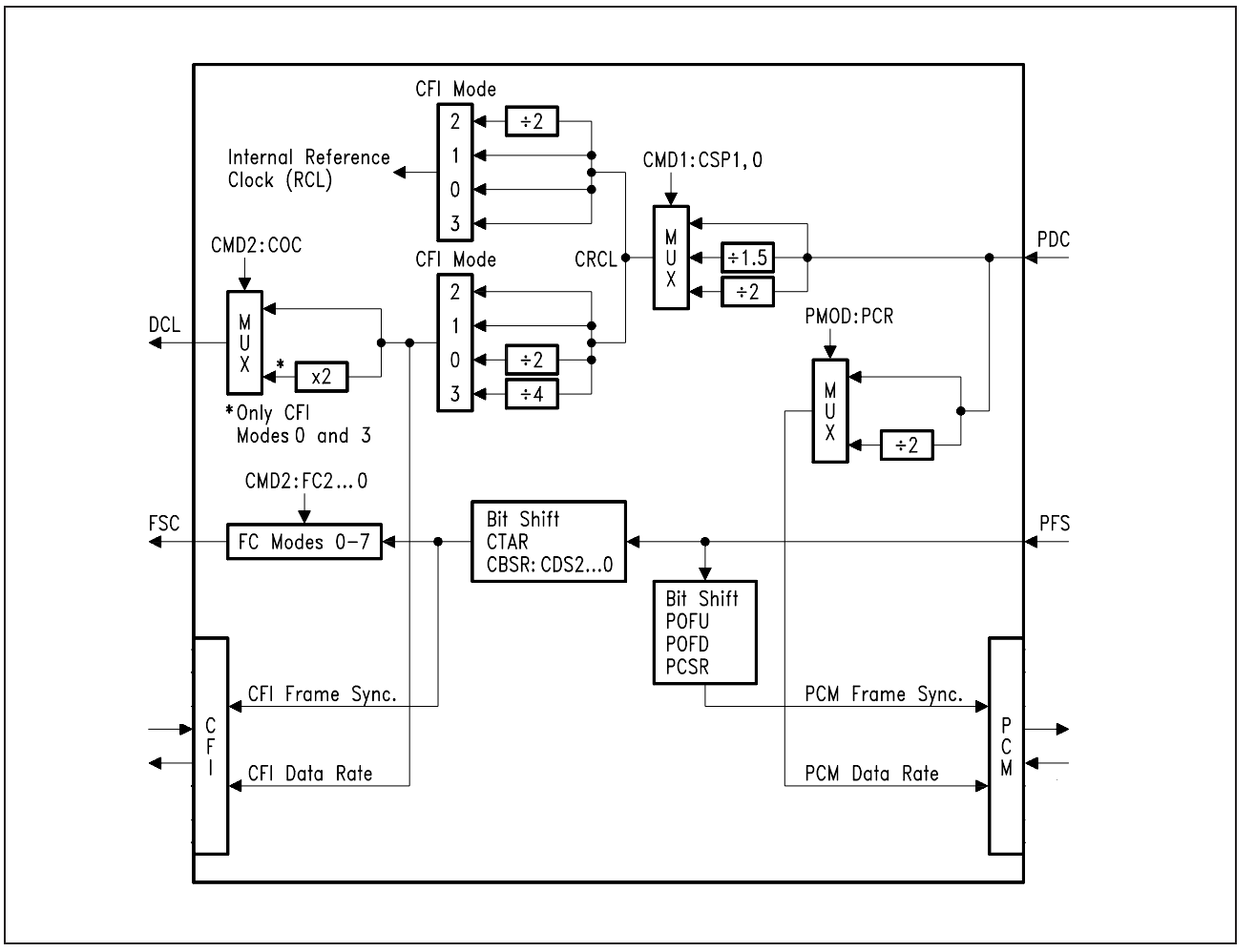


Figure 10 MICO Clock Sources for the CFI and PCM Interfaces if CMD1:CSS = 0

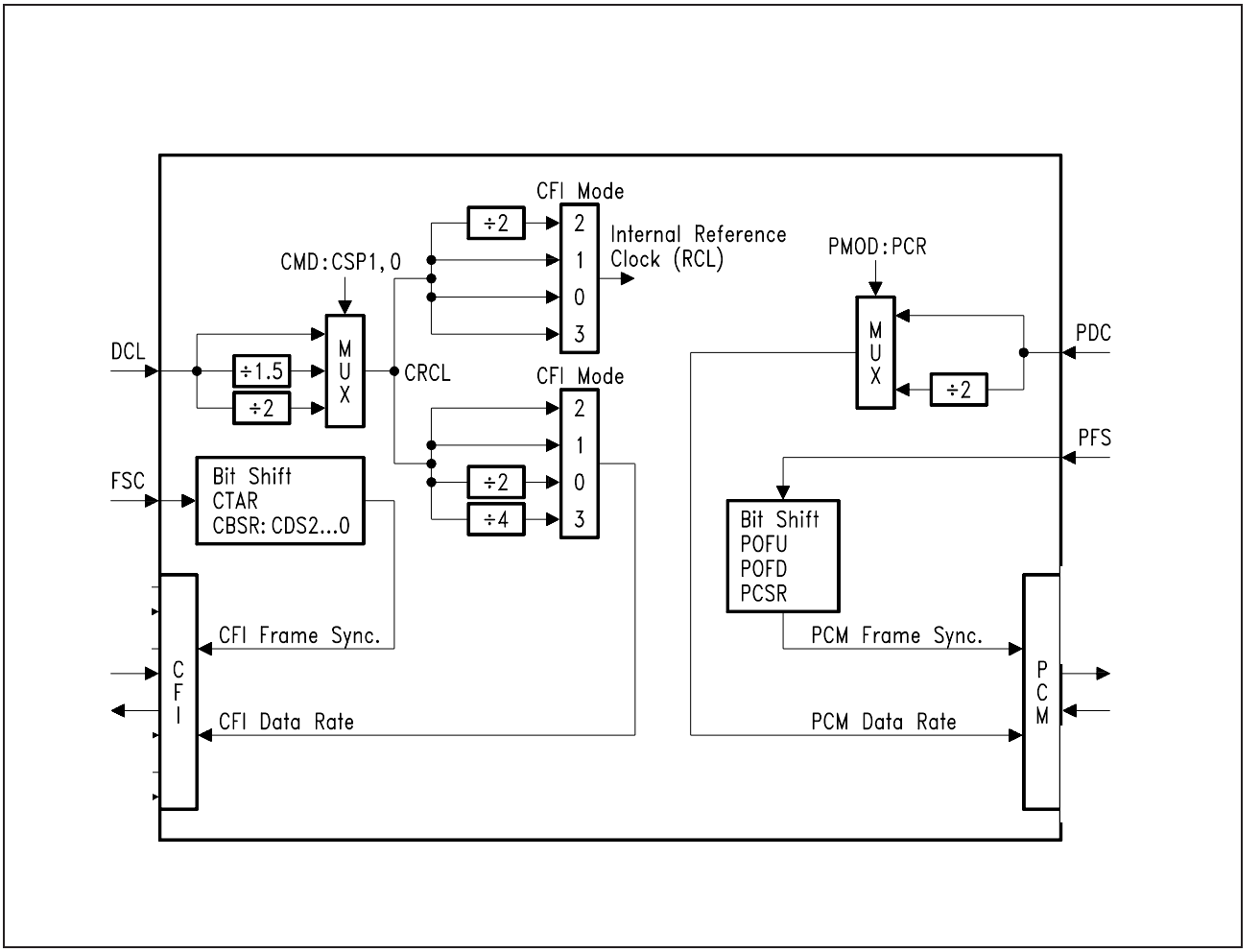


Figure 11
MICO Clock Sources for the CFI and PCM Interfaces if CMD1:CSS = 1

4.2.2.2 Configurable Interface Mode Register 2 (CMD2)

Access in demultiplexed µP-interface mode: read/write address: 7_H
OMDR:RBS = 1
Access in multiplexed µP-interface mode: read/write address: $2E_H$
Reset value: 00_H

bit 7 bit 0

FC2	FC1	FC0	COC	CXF	CRR	CBN9	CBN8

FC2..0 Framing output Control.
Given that CMD1:CSS = 0, these bits determine the position of the FSC-pulse relative to the CFI-frame, as well as the type of FSC-pulse generated. The position and width of the FSC-signal with respect to the CFI-frame can be found in the following two **figures 12** and **13**.

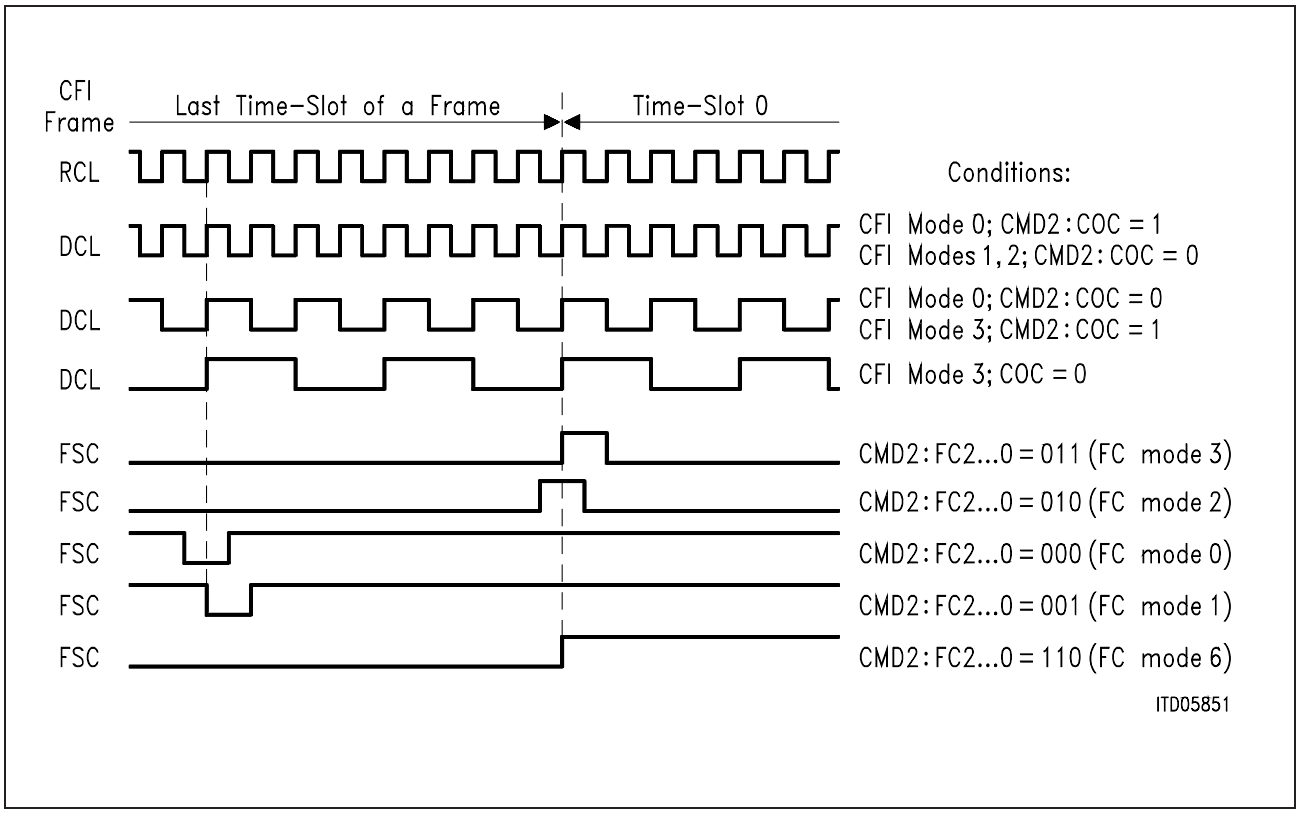


Figure 12 Position of the FSC-Signal for FC-Modes 0, 1, 2, 3 and 6

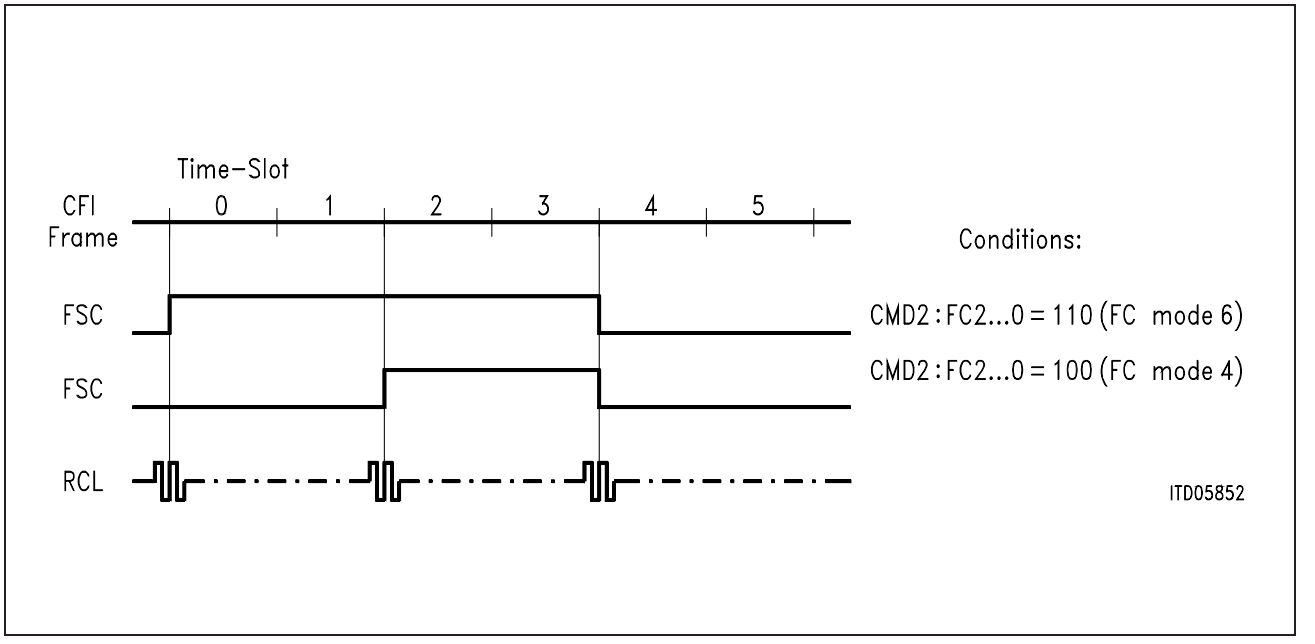


Figure 13 Position of the FSC-Signal for FC-Modes 4 and 6

Application examples:

FC2	FC1	FC0	FC-Mode	Main Applications
0	0	0	0	IOM-1 multiplexed (burst) mode
0	0	1	1	general purpose
0	1	0	2	general purpose
0	1	1	3	general purpose
1	0	0	4	2 ISAC-S per SLD-port
1	0	1	5	reserved
1	1	0	6	IOM-2 or SLD-modes
1	1	1	7	software timed multiplexed applications

For further details on the framing output control please refer to **section 2.2.3** of the EPIC Application Manual 10.92.

COC CFI-Output Clock rate.
0…the frequency of DCL is identical to the CFI-data rate (all CFI-modes),
1…the frequency of DCL is twice the CFI-data rate (CFI-modes 0 and 3 only!)

Note:Applies only if CMD1:CSS = 0.

CXF CFI-Transmit on Falling edge.
0…the data is transmitted with the rising CRCL edge,
1…the data is transmitted with the falling CRCL edge.

CRR CFI-Receive on Rising edge.
0…the data is received with the falling CRCL edge,
1…the data is received with the rising CRCL edge.

Note:CRR must be set to 0 in CFI mode 3.

CBN9..8 CFI Bit Number 9..8
these bits, together with the CBNR:CBN7..0, hold the number of bits per CFI frame.

4.2.2.3 Configurable Interface Bit Number Register (CBNR)

Access in demultiplexed µP-interface mode: read/write address: 8_H OMDR:RBS = 1
Access in multiplexed µP-interface mode: read/write address: 30_H
Reset value: FF_H

bit 7							bit 0
CBN7	CBN6	CBN5	CBN4	CBN3	CBN2	CBN1	CBN0

CBN7..0 CFI-Bit Number 7..0.
The number of bits that constitute a CFI-frame must be programmed to CBNR:CBN7..0 as indicated below.

CBN7..0 = number of bits – 1

For a 8-kHz frame structure, the number of bits per frame can be derived from the data rate by division with 8000.

4.2.2.4 Configurable Interface Time Slot Adjustment Register (CTAR)

Access in demultiplexed µP-interface mode: read/write address: 9_H OMDR:RBS = 1
Access in multiplexed µP-interface mode: read/write address: 32_H
Reset value: 00_H

bit 7							bit 0
0	TSN6	TSN5	TSN4	TSN3	TSN2	TSN1	TSN0

TSN6..0 Time Slot Number.
The CFI-framing signal (PFS if CMD1:CSS = 0 or FSC if CMD1:CSS = 1) marks the CFI time slot called TSN according to the following formula:

TSN6**..**0 = TSN + 2

E.g.: If the framing signal is to mark time slot 0 (bit 7), CTAR must be set to 02_H (CBSR to 20_H).

*Note: If CMD1:CSS = 0, the CFI-frame will be shifted – together with the FSC-output signal – with respect to PFS. The position of the CFI-frame relative to the FSC-output signal is not affected by these settings, but is instead determined by CMD2:FC2**..**0. If CMD1:CSS = 1, the CFI-frame will be shifted with respect to the FSC-input signal.*

4.2.2.5 Configurable Interface Bit Shift Register (CBSR)

Access in demultiplexed µP-interface mode: read/write address: A_H OMDR:RBS = 1

Access in multiplexed µP-interface mode: read/write address: 34_H

Reset value: 00_H

bit 7							bit 0
SFSC	CDS2	CDS1	CDS0	CUS3	CUS2	CUS1	CUS0

SFSC Shift FSC
0...default (behaviour like EPIC-1 PEB 2055)
1...with double clock rate the FSC input is delayed by one CFI clock cycle (IOM-2 compatibility)

If the bit CBSR:SFSC is set the internal FSC will be delayed by one DCL clock cycle. This enables synchronization in double clock mode with the rising DCL edge according to IOM-2. The position of the data bit can now be adjusted using the CFI bit shift functionality as described below.

CDS2..0 CFI-Downstream bit Shift 2..0.
From the zero offset bit position (CBSR = 20_H) the CFI-frame (downstream and upstream) can be shifted by up to 6 bits to the left (within the time slot number TSN programmed in CTAR) and by up to 2 bits to the right (within the previous time slot TSN - 1) by programming the CBSR:CDS2..0 bits:

CBSR:CDS2..0	Time Slot No.	Bit No.
000	TSN - 1	1
001	TSN - 1	0
010	TSN	7
011	TSN	6
100	TSN	5
101	TSN	4
110	TSN	3
111	TSN	2

The bit shift programmed to CBSR:CDS2..0 affects both the upstream and downstream frame position in the same way.

CUS3..0 CFI-Upstream bit Shift 3..0.
These bits shift the upstream CFI-frame relative to the downstream frame by up to 15 bits. For CUS3..0 = 0000, the upstream frame is aligned with the downstream frame (no bit shift).

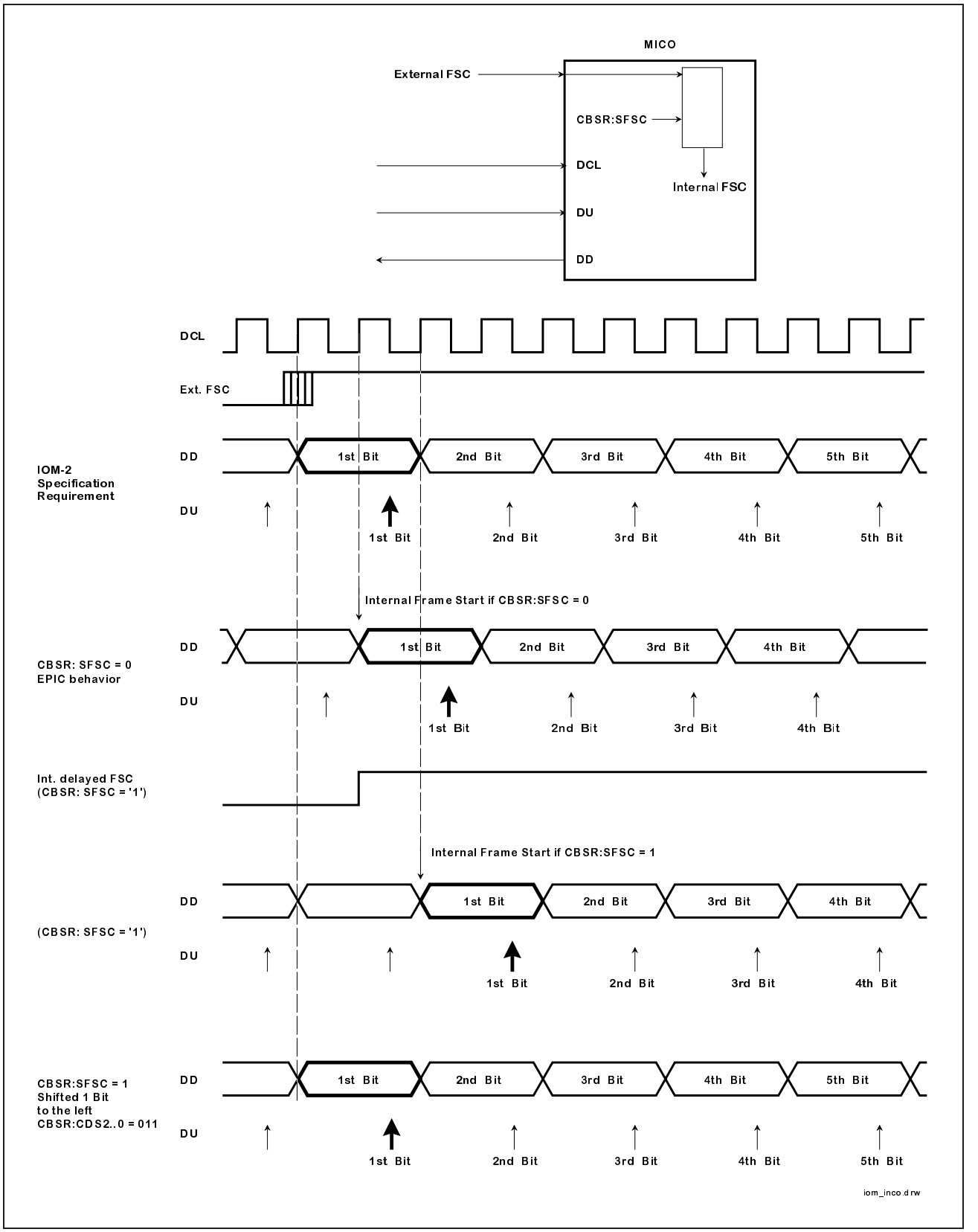


Figure 14 Internal FSC Shift to enable a Synchronization with the Rising Edge of DCL

4.2.2.6 Configurable Interface Subchannel Register (CSCR)

Access in demultiplexed µP-interface mode: read/write address: B_H OMDR:RBS = 1

Access in multiplexed µP-interface mode: read/write address: 36_H

Reset value: 00_H

bit 7							bit 0
0	0	0	0	0	0	SC01	SC00

SC01..00 CFI-Subchannel Control for the CFI port.
The subchannel control bits SC01..SC00 specify the bit positions to be exchanged with the data memory (DM) when a connection with a channel bandwidth as defined by the CM-code has been established:

SC01	**SC00**	**Bit Positions for CFI Subchannels having a Bandwidth of**		
		64 kbit/s	32 kbit/s	16 kbit/s
0	0	7..0	7..4	7..6
0	1	7..0	3..0	5..4
1	0	7..0	7..4	3..2
1	1	7..0	3..0	1..0

Note: In CFI mode 3 SC01 and SC00 control ports 0 and 4.

4.2.3 Memory Access Registers

4.2.3.1 Memory Access Control Register (MACR)

Access in demultiplexed µP-interface mode: read/write address: 0_H
OMDR:RBS = 0
Access in multiplexed µP-interface mode: read/write address: 00_H
Reset value: xx_H

bit 7 bit 0

RWS	MOC3	MOC2	MOC1	MOC0 CMC3	CMC2	CMC1	CMC0

With the MACR the µP selects the type of memory (CM or DM), the type of field (data or code) and the access mode (read or write) of the register access. When writing to the control memory code field, MACR also contains the 4 bit code (CMC3..0) defining the function of the addressed CFI time slot.

RWS Read/Write Select.
0…write operation on control or data memories
1…read operation on control or data memories

MOC3..0 Memory Operation Code.
These bits determine the type and destination of the memory operation as shown below.

CMC3..0 Control Memory Code.
These bits determine the type and destination of the memory operation as shown below.

Note: Prior to a new access to any memory location (i.e. writing to MACR) the STAR:MAC bit must be polled for '0'.

1. Writing data to the upstream DM-data field (e.g. PCM-idle code).
Reading data from the upstream or downstream DM-data field.

MACR:

RWS	MOC3	MOC2	MOC1	MOC0	0	0	0

MOC3..0 defines the bandwidth and the position of the subchannel as shown below:

MOC3..0	Transferred Bits	Channel Bandwidth
0000	–	–
0001	bits 7..0	64 kbit/s
0011	bits 7..4	32 kbit/s
0010	bits 3..0	32 kbit/s
0111	bits 7..6	16 kbit/s
0110	bits 5..4	16 kbit/s
0101	bits 3..2	16 kbit/s
0100	bits 1..0	16 kbit/s

Note: When reading a DM-data field location, all 8 bits are read regardless of the bandwidth selected by the MOC-bits.

2. **Writing to the upstream DM-code (tristate) field.**
Control-reading the upstream DM-code (tristate).

MACR:

RWS	MOC3	MOC2	MOC1	MOC0	0	0	0

MOC = 1100 Read/write tristate info from/to single PCM time slot

MOC = 1101 Write tristate info to all PCM time slots

Note: The tristate field is exchanged with the 4 least significant bits (LSBs) of the MADR. MADR:MD3 controls the PCM interface function of the bits 7 and 6, MD2 of bits 5 and 4, MD1 of bits 3 and 2, MD0 of bits 1 and 0 (0 = high impedance, 1 = low impedance).

3. **Writing data to the upstream or downstream CM-data field (e.g. signaling code).**
Reading data from the upstream or downstream CM-data field.

MACR:

RWS	1	0	0	1	0	0	0

4. **Writing data to the upstream or downstream CM-data and code field (e.g. switching a CFI to/from PCM-connection).**

MACR:

0	1	1	1	CMC3	CMC2	CMC1	CMC0

The 4-bit code field of the control memory (CM) defines the functionality of a CFI time slot and thus the meaning of the corresponding data field. This 4-bit code, written to the MACR:CMC3..0 bit positions, will be transferred to the CM-code field. The 8-bit MADR value is at the same time transferred to the CM-data field. There are codes for switching applications, pre-processed applications and for direct µP-access applications, as shown below:

a) Switching Applications

CMC = 0000	Unassigned channel (e.g. cancelling an assigned channel)	
CMC = 0001	Bandwidth 64 kbit/s	PCM time slot bits transferred: 7..0
CMC = 0010	Bandwidth 32 kbit/s	PCM time slot bits transferred: 3..0
CMC = 0011	Bandwidth 32 kbit/s	PCM time slot bits transferred: 7..4
CMC = 0100	Bandwidth 16 kbit/s	PCM time slot bits transferred: 1..0
CMC = 0101	Bandwidth 16 kbit/s	PCM time slot bits transferred: 3..2
CMC = 0110	Bandwidth 16 kbit/s	PCM time slot bits transferred: 5..4
CMC = 0111	Bandwidth 16 kbit/s	PCM time slot bits transferred: 7..6

Note: The corresponding CFI time slot bits to be transferred are chosen in the CSCR-register.

b) Pre-processed Applications

Downstream:

Application	Even CM Address	Odd CM Address
Decentral D-channel handling	CMC = 1000	CMC = 1011
Central D-channel handling	CMC = 1010	CMC = PCM-code for a 2-bit subtime slot
6-bit Signaling (e.g. analog IOM)	CMC = 1010	CMC = 1011
8-bit Signaling (e.g. SLD)	CMC = 1010	CMC = 1011

Upstream:

Application	Even CM Address	Odd CM Address
Decentral D-channel handling	CMC = 1000	CMC = 0000
Central D-channel handling	CMC = 1000	CMC = PCM-code for a 2-bit subtime slot
6-bit Signaling (e.g. analog IOM)	CMC = 1010	CMC = 1010
8-bit Signaling (e.g. SLD)	CMC = 1011	CMC = 1011

c) µP-access Applications

MACR:

0	1	1	1	1	0	0	1

Setting CMC = 1001, initializes the corresponding CFI time slot to be accessed by the µP. Concurrently, the datum in MADR is written (as 8-bit CFI-idle code) to the CM-data field. The content of the CM-data field is directly exchanged with the corresponding time slot.

Note that once the CM-code field has been initialized, the CM-data field can be written and read as described in **subsection 3**.

5. **Control-reading the upstream or downstream CM-code.**

MACR:

1	1	1	1	0	0	0	0

The CM-code can then be read out of the 4 LSBs of the MADR-register.

4.2.3.2 Memory Access Address Register (MAAR)

Access in demultiplexed µP-interface mode: read/write address: 1_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read/write address: 02_H

Reset value: xx_H

bit 7 bit 0

U/$\overline{D}$	MA6	MA5	MA4	MA3	MA2	MA1	MA0

The Memory Access Address Register MAAR specifies the address of the memory access. This address encodes a CFI time slot for control memory (CM) and a PCM time slot for data memory (DM) accesses. Bit 7 of MAAR (U/$\overline{D}$-bit) selects between upstream and downstream memory blocks. Bits MA6..0 encode the CFI- or PCM-port and time slot number as in the following tables:

Table 3

Time Slot Encoding for Data Memory Accesses

Data Memory Address		
PCM-mode 0	bit U/$\overline{D}$ bits MA6..MA3, MA0 bits MA2..MA1	direction selection time slot selection have to be ’0’ (refer to **figure 7**)
PCM-mode 1	bit U/$\overline{D}$ bits MA6..MA3, MA1, MA0 bit MA2	direction selection time slot selection has to be ’0’ (refer to **figure 7**)
PCM-mode 2	bit U/$\overline{D}$ bits MA6..MA0	direction selection time slot selection

Table 4
Time Slot Encoding for Control Memory Accesses

Control Memory Address		
CFI-mode 0	bit U/$\overline{D}$ bits MA6..MA3, MA0 bits MA2..MA1	direction selection time slot selection have to be ’0’ (refer to **figure 7**)
CFI-mode 1	bit U/$\overline{D}$ bits MA6..MA3, MA2, MA0 bit MA1	direction selection time slot selection has to be ’0’ (refer to **figure 7**)
CFI-mode 2	bit U/$\overline{D}$ bits MA6..MA0	direction selection time slot selection
CFI-mode 3	bit U/$\overline{D}$ bits MA6..MA4, MA0 bits MA3..MA1	direction selection time slot selection have to be 000 or 100 as only I/O0 and I/O4 are supported

4.2.3.3 Memory Access Data Register (MADR)

Access in demultiplexed µP-interface mode: read/write address: 2_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read/write address: 04_H

Reset value: xx_H

bit 7							bit 0
MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0

The Memory Access Data Register MADR contains the data to be transferred from or to a memory location. The meaning and the structure of this data depends on the kind of memory being accessed.

4.2.4 Synchronous Transfer Registers

4.2.4.1 Synchronous Transfer Data Register (STDA)

Access in demultiplexed µP-interface mode: read/write address: 3_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read/write address: 06_H

Reset value: xx_H

bit 7							bit 0
MTDA7	MTDA6	MTDA5	MTDA4	MTDA3	MTDA2	MTDA1	MTDA0

The STDA-register buffers the data transferred over the synchronous transfer channel A.

MTDA7 to MTDA0 hold the bits 7 to 0 of the respective time slot. MTDA7 (MSB) is the bit transmitted/received first, MTDA0 (LSB) the bit transmitted/received last over the serial interface.

4.2.4.2 Synchronous Transfer Data Register B (STDB)

Access in demultiplexed µP-interface mode: read/write address: 4_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read/write address: 08_H

Reset value: xx_H

bit 7							bit 0
MTDB7	MTDB6	MTDB5	MTDB4	MTDB3	MTDB2	MTDB1	MTDB0

The STDB-register buffers the data transferred over the synchronous transfer channel B.

MTDB7 to MTDB0 hold the bits 7 to 0 of the respective time slot. MTDB7 (MSB) is the bit transmitted/received first, MTDB0 (LSB) the bit transmitted/received last over the serial interface.

4.2.4.3 Synchronous Transfer Receive Address Register A (SARA)

Access in demultiplexed µP-interface mode: read/write address: 5_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read/write address: $0A_H$

Reset value: xx_H

bit 7 bit 0

ISRA	MTRA6	MTRA5	MTRA4	MTRA3	MTRA2	MTRA1	MTRA0

The SARA-register specifies for synchronous transfer channel A from which input interface and time slot the serial data is extracted. This data can then be read from the STDA-register.

ISRA Interface Select Receive for channel A.

0… selects the PCM-interface as the input interface for synchronous channel A.

1… selects the CFI-interface as the input interface for synchronous channel A.

MTRA6..0 µP-Transfer Receive Address for channel A; selects the port and time slot number at the interface selected by ISRA according to **tables 3** and **4**: MTRA6..0 = MA6..0.

4.2.4.4 Synchronous Transfer Receive Address Register B (SARB)

Access in demultiplexed µP-interface mode: read/write address: 6_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read/write address: $0C_H$

Reset value: xx_H

bit 7 bit 0

ISRB	MTRB6	MTRB5	MTRB4	MTRB3	MTRB2	MTRB1	MTRB0

The SARB-register specifies for synchronous transfer channel B from which input interface and time slot the serial data is extracted. This data can then be read from the STDB register.

ISRB Interface Select Receive for channel B.
0… selects the PCM-interface as the input interface for synchronous channel B.
1… selects the CFI-interface as the input interface for synchronous channel B.

MTRB6..0 µP-Transfer Receive Address for channel B; selects the port and time slot number at the interface selected by ISRB according to **tables 3** and **4**: MTRB6..0 = MA6..0.

4.2.4.5 Synchronous Transfer Transmit Address Register A (SAXA)

Access in demultiplexed µP-interface mode: read/write address: 7_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read/write address: $0E_H$

Reset value: xx_H

bit 7 bit 0

ISXA	MTXA6	MTXA5	MTXA4	MTXA3	MTXA2	MTXA1	MTXA0

The SAXA-register specifies for synchronous transfer channel A to which output interface and time slot the serial data contained in the STDA-register is sent.

ISXA Interface Select Transmit for channel A.
0… selects the PCM-interface as the output interface for synchronous channel A.
1… selects the CFI-interface as the output interface for synchronous channel A.

MTXA6..0 µP-Transfer Transmit Address for channel A; selects the port and time slot number at the interface selected by ISXA according to **tables 3** and **4**: MTXA6..0 = MA6..0.

4.2.4.6 Synchronous Transfer Transmit Address Register B (SAXB)

Access in demultiplexed µP-interface mode: read/write address: 8_H OMDR:RBS = 0
Access in multiplexed µP-interface mode: read/write address: 10_H
Reset value: xx_H

bit 7							bit 0
ISXB	MTXB6	MTXB5	MTXB4	MTXB3	MTXB2	MTXB1	MTXB0

The SAXB-register specifies for synchronous transfer channel B to which output interface and time slot the serial data contained in the STDB-register is sent.

ISXB Interface Select Transmit for channel B.
0… selects the PCM-interface as the output interface for synchronous channel B.
1… selects the CFI-interface as the output interface for synchronous channel B.

MTXB6..0 µP-Transfer Transmit Address for channel B; selects the port and time slot number at the interface selected by ISXB according to **tables 3** and **4**: MTXB6..0 = MA6..0.

4.2.4.7 Synchronous Transfer Control Register (STCR)

Access in demultiplexed µP-interface mode: read/write address: 09_H OMDR:RBS = 0
Access in multiplexed µP-interface mode: read/write address: 12_H
Reset value: $00xxxxxx_B$

bit 7							bit 0
TBE	TAE	CTB2	CTB1	CTB0	CTA2	CTA1	CTA0

The STCR-register bits are used to enable or disable the synchronous transfer utility and to determine the sub time slot bandwidth and position if a PCM-interface time slot is involved.

TAE, TBE Transfer Channel A (B) Enable.
1… enables the µP transfer of the corresponding channel.
0… disables the µP transfer of the corresponding channel.

CTA2..0 Channel Type A (B); these bits determine the bandwidth of the channel and
CTB2..0 the position of the relevant bits in the time slot according to the table below.

Note: If a CFI time slot is selected as receive or transmit time slot of the synchronous transfer, the 64-kbit/s bandwidth must be selected (CT#2..CT#0 = 001).

CT#2	CT#1	CT#0	Bandwidth	Transferred Bits
0	0	0	not allowed	–
0	0	1	64 kbit/s	bits 7..0
0	1	0	32 kbit/s	bits 3..0
0	1	1	32 kbit/s	bits 7..4
1	0	0	16 kbit/s	bits 1..0
1	0	1	16 kbit/s	bits 3..2
1	1	0	16 kbit/s	bits 5..4
1	1	1	16 kbit/s	bits 7..6

4.2.5 Monitor/Feature Control Registers

4.2.5.1 MF-Channel Active Indication Register (MFAIR)

Access in demultiplexed µP-interface mode: read address: A_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read address: 14_H

Reset value: 00xx $xxxx_B$

bit 7 bit 0

0	SO	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0

This register is only used in IOM-2 applications (active handshake protocol) in order to identify active monitor channels when the "Search for active monitor channels" command (CMDR:MFSO) has been executed.

SO MF Channel Search On.
0…the search is completed.
1…the MICO is still busy looking for an active channel.

SAD5..0 Subscriber Address 5..0; after an ISTA:MAC-interrupt these bits point to the time slot where an active channel has been found. The coding is identical to MFSAR:SAD5..SAD0.

4.2.5.2 MF-Channel Subscriber Address Register (MFSAR)

Access in demultiplexed µP-interface mode: write address: A_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: write address: 14_H

Reset value: xx_H

bit 7							bit 0
MFTC1	MFTC0	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0

The exchange of monitor data normally takes place with only one subscriber circuit at a time. This register serves to point the MF-handler to that particular CFI time slot.

MFTC1..0 MF Channel Transfer Control 1..0; these bits, in addition to CMDR:MFT1,0 and OMDR:MFPS control the MF-channel transfer as indicated in **table 5**.

SAD5..0 Subscriber address 5..0; these bits define the addressed subscriber. The CFI time slot encoding is similar to the one used for Control Memory accesses using the MAAR-register (**tables 3** and **4**):

CFI time slot encoding of MFSAR derived from MAAR:

MAAR:	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
		↓	↓	↓	↓	↓	↓	
MFSAR:	MFTC1	MFTC0	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0

MAAR:MA7 selects between upstream and downstream CM-blocks. This information is not required since the transfer direction is defined by CMDR (transmit or receive).

MAAR:MA0 selects between even and odd time slots. This information is also not required since MF-channels are always located on even time slots.

4.2.5.3 Monitor/Feature Control Channel FIFO (MFFIFO)

Access in demultiplexed µP-interface mode: read/write address: B_H OMDR:RBS = 0
Access in multiplexed µP-interface mode: read/write address: 16_H
Reset value: xx_H

bit 7							bit 0
MFD7	MFD6	MFD5	MFD4	MFD3	MFD2	MFD1	MFD0

The 16-byte bi-directional MFFIFO provides intermediate storage for data bytes to be transmitted or received over the monitor or feature control channel.

MFD7..0 MF Data bits 7..0; MFD7 (MSB) is the first bit to be sent over the serial CFI, MFD0 (LSB) the last.

Note: The byte n+1 of an n-byte transmit message in monitor channel is not defined.

4.2.6 Status/Control Registers

4.2.6.1 Signaling FIFO (CIFIFO)

Access in demultiplexed µP-interface mode: read address: C_H OMDR:RBS = 0
Access in multiplexed µP-interface mode: read address: 18_H
Reset value: $0xxxxxxx_B$

bit 7							bit 0
SBV	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0

The 9 byte deep CIFIFO stores the addresses of CFI time slots in which a C/I- and/or a SIG-value change has taken place. This address information can then be used to read the actual C/I- or SIG-value from the control memory.

SBV Signaling Byte Valid.

0… the SAD6..0 bits are invalid.

1… the SAD6..0 bits indicate a valid subscriber address. The polarity of SBV is chosen such that the whole 8 bits of the CIFIFO can be copied to the MAAR register in order to read the upstream C/I- or SIG-value from the control memory.

SAD6..0 Subscriber Address bits 6..0; The CM-address which corresponds to the CFI time slot where a C/I- or SIG-value change has taken place is encoded in these bits. For C/I-channels SAD6..0 point to an even CM-address (C/

I-value), for SIG-channels SAD6..0 point to an odd CM-address (stable SIG-value).

4.2.6.2 Timer Register (TIMR)

Access in demultiplexed µP-interface mode: write address: C_H
OMDR:RBS = 0
Access in multiplexed µP-interface mode: write address: 18_H
Reset value: 00_H

bit 7 bit 0

SSR	TVAL6	TVAL5	TVAL4	TVAL3	TVAL2	TVAL2	TVAL0

The MICO timer can be used for 3 different purposes: timer interrupt generation (ISTA:TIG), FSC multiframe generation (CMD2:FC2..0 = 111) and last look period generation.

SSR Signaling Sampling Rate.
0… the last look period is defined by TVAL6..0.
1… the last look period is fixed to 125 µs.

TVAL6..0 Timer Value bits 6..0; the timer period, equal to (1+TVAL6..0) × 250 µs, is programmed here. It can thus be adjusted within the range of 250 µs up to 32 ms.

The timer is started as soon as CMDR:ST is set to 1 and stopped by writing the TIMR-register or by selecting OMDR:OMS0 = 0.

4.2.6.3 Status Register (STAR)

Access in demultiplexed µP-interface mode: read address: D_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: read address: $1A_H$

Reset value: 05_H

bit 7							bit 0
MAC	TAC	PSS	MFTO	MFAB	MFAE	MFRW	MFFE

The status register STAR displays the current state of certain events within the MICO. The STAR register bits do not generate interrupts and are not modified by reading STAR.

MAC Memory Access

0… no memory access is in operation.

1… a memory access is in operation. Hence, the memory access registers may not be used.

Note: MAC is also set and reset during synchronous transfers.

TAC Timer Active

0… the timer is stopped.

1… the timer is running.

PSS PCM-Synchronization Status.

1… the PCM-interface is synchronized.

0… the PCM-interface is not synchronized. There is a mismatch between the PBNR-value and the applied clock and framing signals (PDC/PFS) or OMDR:OMS0 = 0.

MFTO MF-Channel Transfer in Operation.

0… no MF-channel transfer is in operation.

1… an MF-channel transfer is in operation.

MFAB MF-Channel Transfer Aborted.

0… the remote receiver did not abort a handshake message transfer.

1… the remote receiver aborted a handshake message transfer.

MFAE MFFIFO-Access Enable.

0… the MFFIFO may not be accessed.

1… the MFFIFO may be either read or written to.

MFRW MFFIFO Read/Write.

0… the MFFIFO is ready to be written to.

1… the MFFIFO may be read.

MFFE MFFIFO Empty

0… the MFFIFO is not empty.

1… the MFFIFO is empty.

4.2.6.4 Command Register (CMDR)

Access in demultiplexed µP-interface mode: write address: D_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: write address: $1A_H$

Reset value: 00_H

bit 7							bit 0
0	ST	TIG	CFR	MFT1	MFT0	MFSO	MFFR

Writing a logical 1 to a CMDR-register bit starts the respective operation.

ST Start Timer.

0… no action. If the timer shall be stopped, the TIMR-register must simply be written with a random value.

1… starts the timer to run cyclically from 0 to the value programmed in TIMR:TVAL6..0.

TIG Timer Interrupt Generation.

0… setting the TIG-bit to logical 0 together with the CMDR:ST-bit set to logical 1 disables the interrupt generation.

1… setting the TIG-bit to logical 1 together with CMDR:ST-bit set to logical 1 causes the MICO to generate a periodic interrupt (ISTA:TIN) each time the timer expires.

CFR CIFIFO Reset.

0… no action.

1… resets the signaling FIFO within 2 RCL-periods, i.e. all entries and the ISTA:SFI-bit are cleared.

MFT1..0 MF-channel Transfer Control Bits 1,0; these bits start the monitor transfer enabling the contents of the MFFIFO to be exchanged with the subscriber circuits as specified in MFSAR. The function of some commands depends furthermore on the selected protocol (OMDR:MFPS). **Table 5** summarizes all available MF-commands.

MFSO MF-channel Search On.

0… no action.

1… the MICO starts to search for active MF-channels. Active channels are characterized by an active MX-bit (logical 0) sent by the remote transmitter. If such a channel is found, the corresponding address is stored in MFAIR and an ISTA:MAC-interrupt is generated. The search is stopped when an active MF-channel has been found or when OMDR:OMS0 is set to 0.

MFFR MFFIFO Reset.

0… no action

1… resets the MFFIFO and all operations associated with the MF-handler (except for the search function) within 2 RCL-periods. The MFFIFO is set into the state "MFFIFO empty", write access enabled and any monitor data transfer currently in process will be aborted.

Table 5

Summary of MF-Channel Commands

Transfer Mode	CMDR: MFT1,MFT0	MFSAR	Protocol Selection	Application
Inactive	00	xxxxxxxx	HS, no HS	idle state
Transmit	01	00 SAD5..0	HS, no HS	IOM-2, IOM-1, SLD
Transmit broadcast	01	01xxxxxx	HS, no HS	IOM-2, IOM-1, SLD
Test operation	01	10------	HS, no HS	IOM-2, IOM-1, SLD
Transmit continuous	11	00 SAD5..0	HS	IOM-2
Transmit + receive same time slot				
Any # of bytes	10	00 SAD5..0	HS	IOM-2
1 byte expected	10	00 SAD5..0	no HS	IOM-1
2 bytes expected	10	01 SAD5..0	no HS	(IOM-1)
8 bytes expected	10	10 SAD5..0	no HS	(IOM-1)
16 bytes expected	10	11 SAD5..0	no HS	(IOM-1)
Transmit + receive same line				
1 byte expected	11	00 SAD5..0	no HS	SLD
2 bytes expected	11	01 SAD5..0	no HS	SLD
8 bytes expected	11	10 SAD5..0	no HS	SLD
16 bytes expected	11	11 SAD5..0	no HS	SLD

HS: handshake facility enabled (OMDR:MFPS = 1)

no HS: handshake facility disable (OMDR:MFPS = 0)

4.2.6.5 Interrupt Status Register (ISTA)

Access in demultiplexed μP-interface mode: read address: E_H OMDR:RBS = 0

Access in multiplexed μP-interface mode: read address: $1C_H$

Reset value: 00_H

bit 7 bit 0

TIN	SFI	MFFI	MAC	PFI	0	SIN	SOV

The ISTA-register should be read after an interrupt in order to determine the interrupt source.

TIN Timer interrupt; a timer interrupt previously requested with CMDR:ST,TIG = 1 has occurred. The TIN-bit is reset by reading ISTA. It should be noted that the interrupt generation is periodic, i.e. unless stopped by writing to TIMR, the ISTA:TIN will be generated each time the timer expires.

SFI Signaling FIFO-Interrupt; this interrupt is generated if there is at least one valid entry in the CIFIFO indicating a change in a C/I- or SIG-channel. Reading ISTA does not clear the SFI-bit. Instead SFI is cleared if the CIFIFO is empty which can be accomplished by reading all valid entries of the CIFIFO or by resetting the CIFIFO by setting CMDR:CFR to 1.

MFFI MFFIFO-Interrupt; the last MF-channel command (issued by CMDR:MFT1,MFT0) has been executed and the MICO is ready to accept the next command. Additional information can be read from STAR:MFTO…MFFE. MFFI is reset by reading ISTA.

MAC Monitor channel Active interrupt; the MICO has found an active monitor channel. A new search can be started by reissuing the CMDR:MFSO-command. MAC is reset by reading ISTA.

PFI PCM-Framing Interrupt; the STAR:PSS-bit has changed its polarity. To determine whether the PCM-interface is synchronized or not, STAR must be read. The PFI-bit is reset by reading ISTA.

SIN Synchronous Transfer Interrupt; The SIN-interrupt is enabled if at least one synchronous transfer channel (A and/or B) is enabled via the STCR:TAE, TBE-bits. The SIN-interrupt is generated when the access window for the μP opens. After the occurrence of the SIN-interrupt the μP can read and/or write the synchronous transfer data registers (STDA, STDB). The SIN-bit is reset by reading ISTA.

SOV Synchronous Transfer Overflow; The SOV-interrupt is generated if the µP fails to access the data registers (STDA, STDB) within the access window. The SOV-bit is reset by reading ISTA.

4.2.6.6 Mask Register MICO (MASK)

Access in demultiplexed µP-interface mode: write address: E_H OMDR:RBS = 0

Access in multiplexed µP-interface mode: write address: $1C_H$

Reset value: 00_H

bit 7 bit 0

TIN	SFI	MFFI	MAC	PFI	1	SIN	SOV

A logical 1 disables the corresponding interrupt as described in the ISTA-register.

A masked interrupt is stored internally and reported in ISTA immediately if the mask is released. However, an SFI-interrupt is also reported in ISTA if masked. In this case no interrupt is generated. When writing register MASK while ISTA indicates a non masked interrupt, $\overline{INT}$ is temporarily set into the inactive state.

4.2.6.7 Operation Mode Register (OMDR)

Access in demultiplexed µP-interface mode: read/write address: F_H
OMDR:RBS = X

Access in multiplexed µP-interface mode: read/write address: $1E_H/3E_H$

Reset value: 00_H

bit 7 bit 0

OMS1	OMS0	PSB	PTL	COS	MFPS	CSB	RBS

OMS1..0 Operational Mode Selection; these bits determine the operation mode of the MICO is working in according to the following table:

OMS1..0	Function
00	The **CM-reset mode** is used to reset all locations of the control memory code and data fields with a single command within only 256 RCL-cycles. A typical application is resetting the CM with the command MACR = 70_H which writes the contents of MADR (xx_H) to all data field locations and the code '0000' (unassigned channel) to all code field locations. A CM-reset should be made after each hardware reset. In the CM-reset mode the MICO does not operate normally i.e. the CFI- and PCM-interfaces are not operational.
10	The **CM-initialization mode** allows fast programming of the control memory since each memory access takes a maximum of only 2.5 RCL-cycles compared to the 9.5 RCL-cycles in the normal mode. Accesses are performed on individual addresses specified by MAAR. The initialization of control/signaling channels in IOM- or SLD- applications can for example be carried out in this mode. In the CM- initialization mode the MICO does also not work normally.
11	In the **normal operation mode** the CFI- and PCM-interfaces are operational. Memory accesses performed on single addresses (specified by MAAR) take 9.5 RCL-cycles. An initialization of the complete data memory tristate field takes 1035 RCL-cycles.
01	In **test mode** the MICO sustains normal operation. However memory accesses are no longer performed on a specific address defined by MAAR, but on all locations of the selected memory, the contents of MAAR (including the U/D-bit!) being ignored. A test mode access takes 2057 RCL-cycles.

PSB PCM-Standby.

0…the PCM-interface output pin TxD is set to high impedance and if the $\overline{\text{TSC}}$-pin is actually used as tristate control signal it is set to logical 1 (inactive).

1…the PCM-output pin transmits the contents of the upstream data memory or may be set to high impedance via the data memory tristate field.

PTL PCM-Test Loop.

0…the PCM-test loop is disabled.

1…the PCM-test loop is enabled, i.e. the physical transmit pin TxD is internally connected to the corresponding physical receive pin RxD, such that data transmitted over TxD are internally looped back to RxD and data externally received over RxD are ignored. The TxD pin still outputs the contents of the upstream data memory according to the setting of the tristate field (only modes 0 and 1; mode 1 with AIS-bit set).

COS CFI-Output driver Selection.

0…the CFI-output drivers are tristate drivers.

1…the CFI-output drivers are open drain drivers.

MFPS Monitor/Feature Control Channel Protocol Selection

0...handshake facility disabled (SLD and IOM-1 applications).

1...handshake facility enabled (IOM-2 applications).

CSB CFI-Standby.

0…the CFI-interface output pins DD, DU, DCL and FSC are set to high impedance.

1…the CFI-output pins are active.

RBS Register Bank Selection. Used in demultiplexed data/address modes only.

0…to access the registers used during device operation.

1…to access the registers used during device initialization

4.2.6.8 Version Number Status Register (VNSR)

Access in demultiplexed µP-interface mode: read address: D_H OMDR:RBS = 1

Access in multiplexed µP-interface mode: read address: $3A_H$

Reset value: 02_H

bit 7							bit 0
IR	0	0	0	VN3	VN2	VN1	VN0

The VN3..0 bits are read only bits.

IR Initialization Request; this bit is set to logical 1 after an inappropriate clocking or after a power failure. It is reset to logical 0 after a control memory reset command: OMDR:OMS1..0 = 00, MACR = $7X_H$.

VN3..0 Version status Number; these bits display the MICO chip version as follows

VN3..0	Chip Versions
0010	V1.1

4.3 Register Changes compared to the EPIC

4.3.1 PMOD

AIS1..0 Have to be programmed to ’00’

AIC1..0 Have to be programmed to ’00’ (no alternate input comparison supported).

4.3.2 PCSR

DRCS Added.

ADSRO Added.

4.3.3 PICM

Values are not valid for operation.

4.3.4 CMD1

CIS1..0 Have to be programmed to ’00’ (in CFI modes 0, 1 and 2 always logical port 0 is selected).

4.3.5 CSCR

SC31..30 Have to be programmed to ’00’ (only port 0 supported).
SC21..20
SC11..10

4.3.6 ISTA

PIM Not valid for operation (PCM Input Mismatch not supported as only one PCM input line is provided).

4.3.7 MASK

PIM Has to be programmed to ’1’ (PIM interrupt masked, refer to **4.3.6**).

4.3.8 VSNR

VN3..0 Fixed to ’0010’ (MICO V1.1).

5 Application Examples

5.1 Access Network

Access Networks are used in order to connect subscribers to the telecom network quickly and at low cost.

One possibility is to use the existing cable TV network to provide telephony services. An existing hybrid fiber-coaxial network (HFCN) that has been upgraded for upstream communication is the basis for such an Access Network. **Figure 15** illustrates the functional model of an optical access network (Fiber In The Loop FITL).

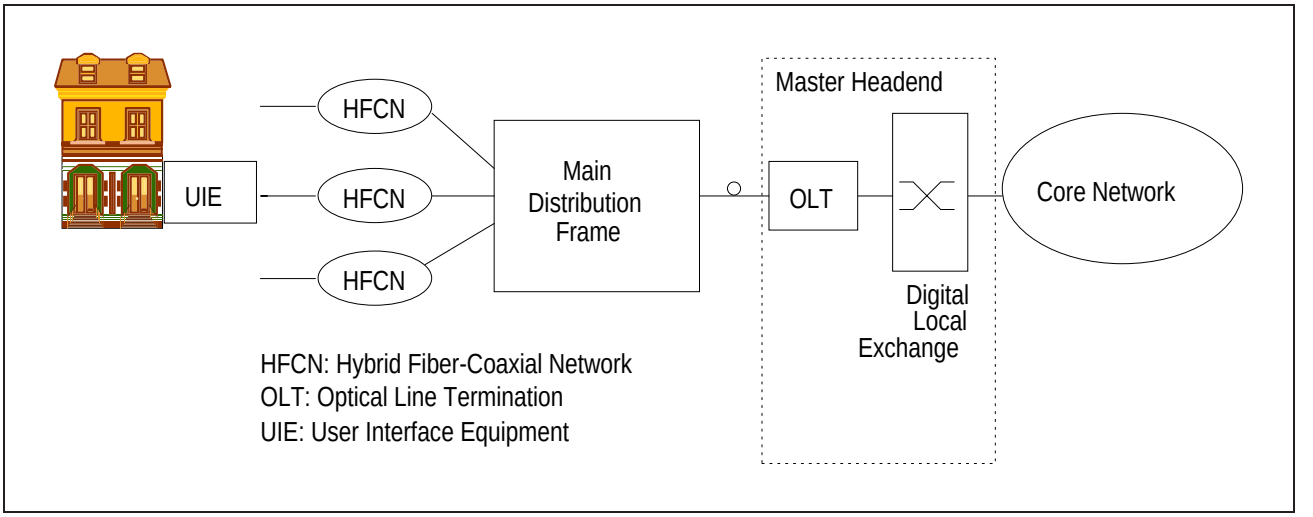


Figure 15 Functional Model of an Optical Access Network

The master headend will serve one or multiple main distribution frames. Via the HFCN the UIE is provided. Depending on the number of supported user ports and how far the fiber is available, the configuration is called Fiber To The Home (FTTH), Fiber To The Building (FTTB) or Fiber To The Curb (FTTC).

The MICO can be used in a configuration where a maximum of 16 POTS or 8 ISDN subscribers are needed, e.g. FTTH or FTTB applications. **Figure 16** shows an example of an user interface equipment (UIE) providing two POTS and one ISDN subscriber.

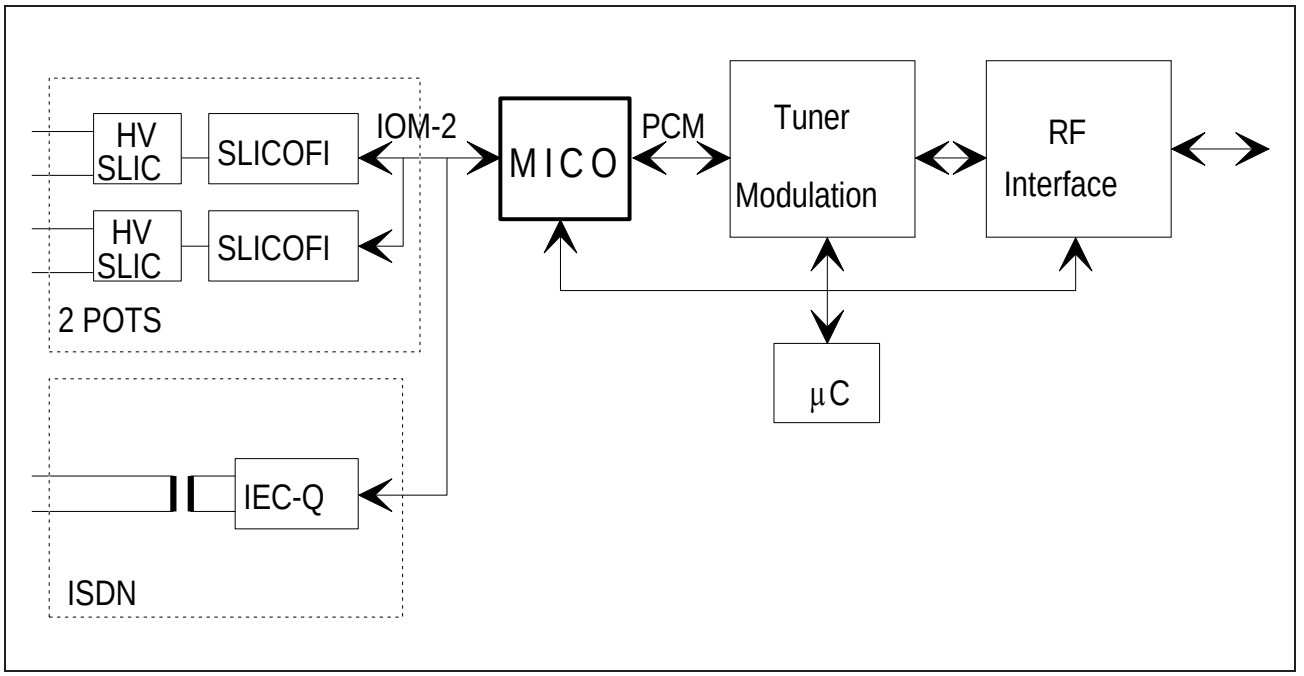


Figure 16 Example using the MICO in an UIE

The MICO will replace the EPIC in applications where only a few subscribers have to be supported. It connects the subscriber circuits to the HF unit providing switching capability. Additionally the subscriber circuits are controlled via the implemented C/I- and Monitor-Handlers.

6 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: PEF	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 125	°C
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Maximum voltage on any pin	V_{max}	6	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

DC Characteristics

PEF: T_A = – 40 to 85 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.2	V_{DD} + 0.4	V	
L-output voltage		V_{OL}		0.45	V	I_{OL} = 7 mA (pins DU, DD) I_{OL} = 2 mA (all other)
H-output voltage		V_{OH}	2.4		V	I_{OH} = – 400 µA
H-output voltage		V_{OH}	3.5		V	I_{OH} = – 200 µA
Power supply current	operational					V_{DD} = 5 V, inputs at 0 V or V_{DD}, no output loads
		I_{CC}		9.5	mA	PDC > 4.096 MHz
		I_{CC}		6.5	mA	PDC ≤ 4.096 MHz
Input leakage current		I_{LI}		1	µA	0 V < V_{IN} < V_{DD} to 0 V
Output leakage current		I_{LO}		1	µA	0 V < V_{OUT} < V_{DD} to 0 V

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V, f_C = 1 MHz, unmeasured pins returned to V_{SS}.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance, f_C = 1 MHz	C_{IN}	5	10	pF
Output capacitance	C_{OUT}	8	15	pF
I/O capacitance	$C_{I/O}$	10	20	pF

AC-Characteristics

Ambient temperature under bias range, V_{DD} = 5 V ± 5 %.

Inputs are driven to 2.4 V for a logical '1' and to 0.4 V for a logical '0'.
Timing measurements are made at 2.0 V for a logical '1' and at 0.8 V for a logical '0'.
The AC-testing input/output wave forms are shown below.

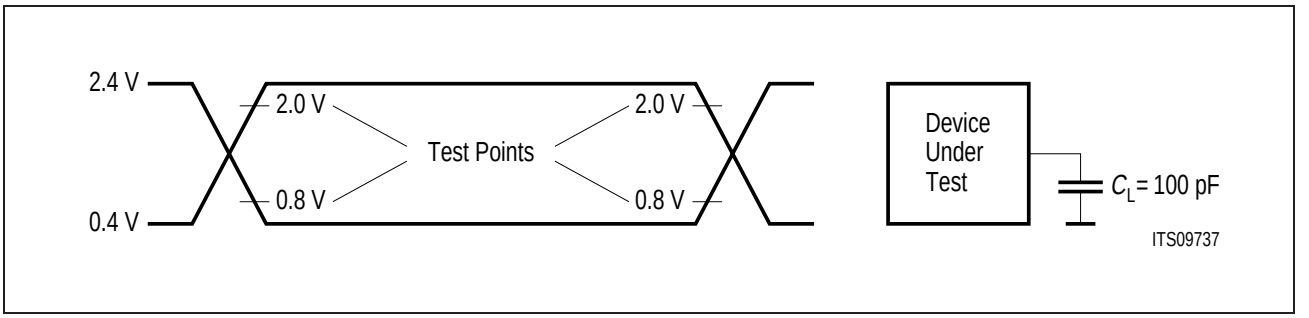


Figure 17 I/O-Wave Form for AC-Test

Bus Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
R or $\overline{W}$ set-up to $\overline{DS}$	t_{DSD}	0		ns
R or $\overline{W}$ hold time from $\overline{DS}$	t_{RWh}		10	ns
$\overline{RD}$-pulse width	t_{RR}	80		ns
$\overline{RD}$-control interval	t_{RI}	40		ns
Data output delay from $\overline{RD}$	t_{RD}		80	ns
Data float delay from $\overline{RD}$	t_{DF}		25	ns
$\overline{WR}$-pulse width	t_{WW}	45		ns
$\overline{WR}$-control interval	t_{WI}	40		ns
Data set-up time to $\overline{WR}$x$\overline{CS}$, $\overline{DS}$x$\overline{CS}$	t_{DW}	0		ns
Data hold time from $\overline{WR}$x$\overline{CS}$, $\overline{DS}$x$\overline{CS}$	t_{WD}	15		ns
ALE-pulse width	t_{AA}	30		ns
Address set-up time to ALE	t_{AL}	10		ns
Address hold time from ALE	t_{LA}	15		ns
ALE set-up time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	8		ns
Address set-up time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	0		ns
Address hold time after reset	t_{AHR}	10		ns

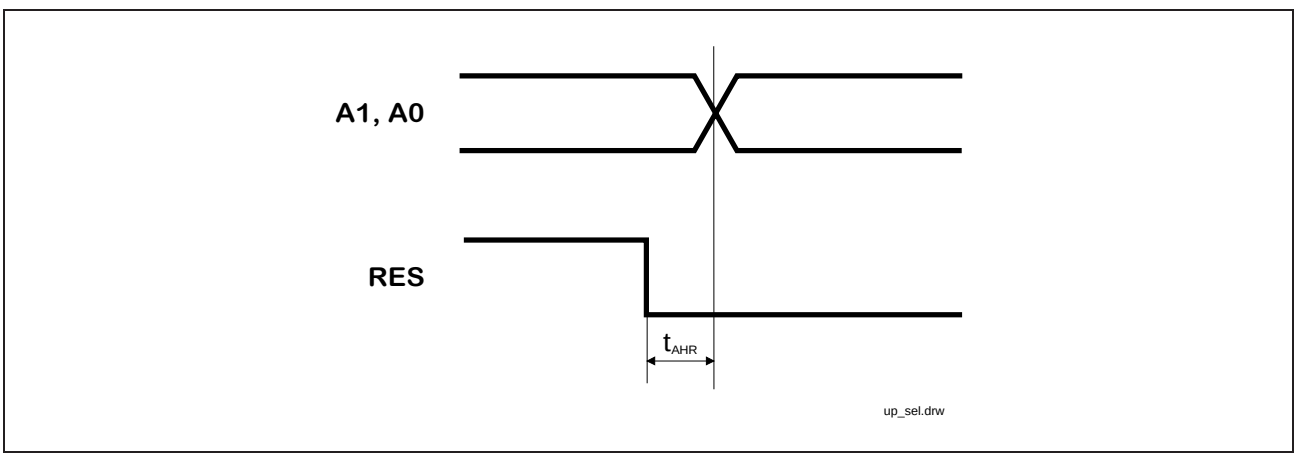


Figure 18 Microprocessor Interface Selection: Address Hold Time after Reset

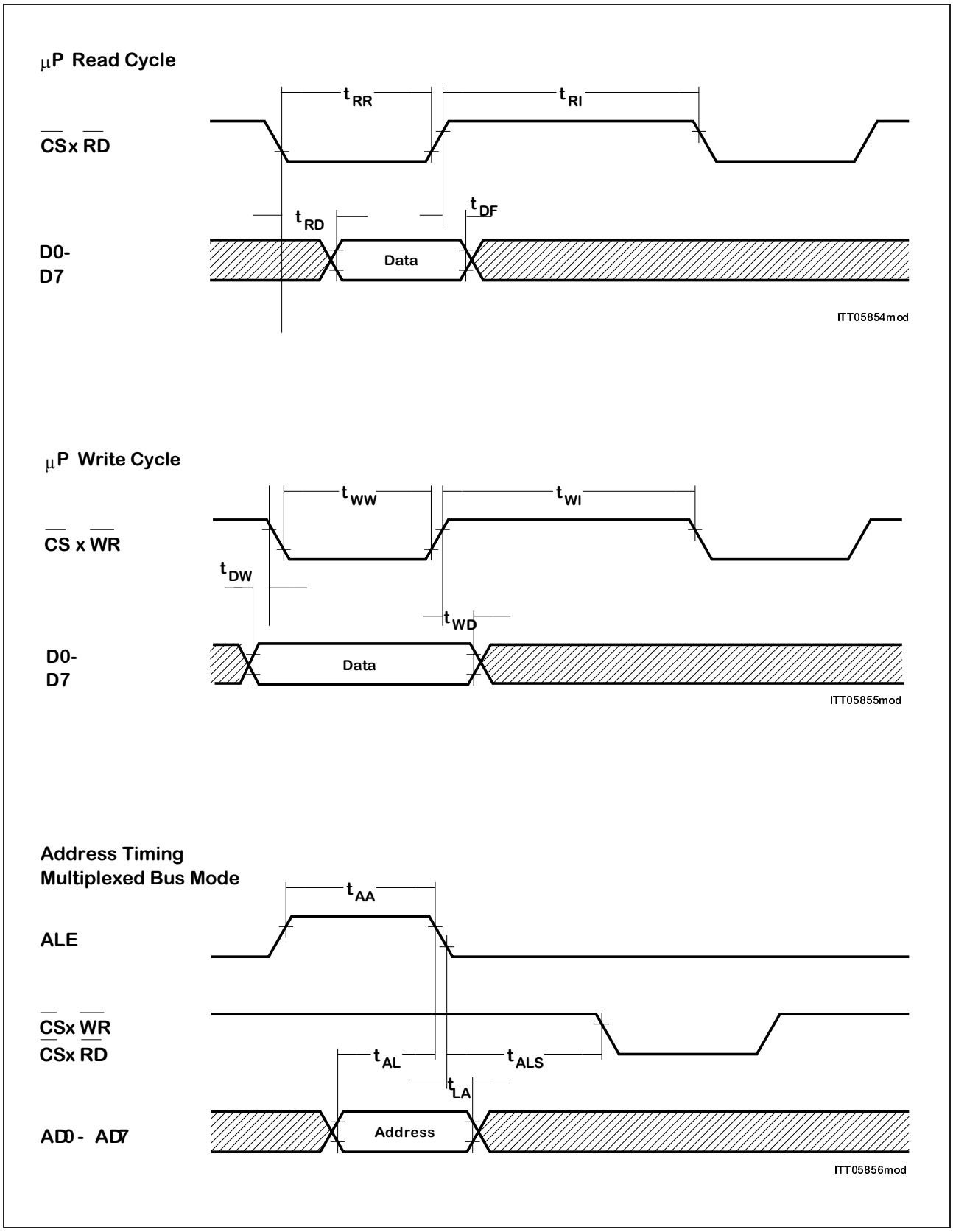


Figure 19 a Siemens/Intel Bus Mode

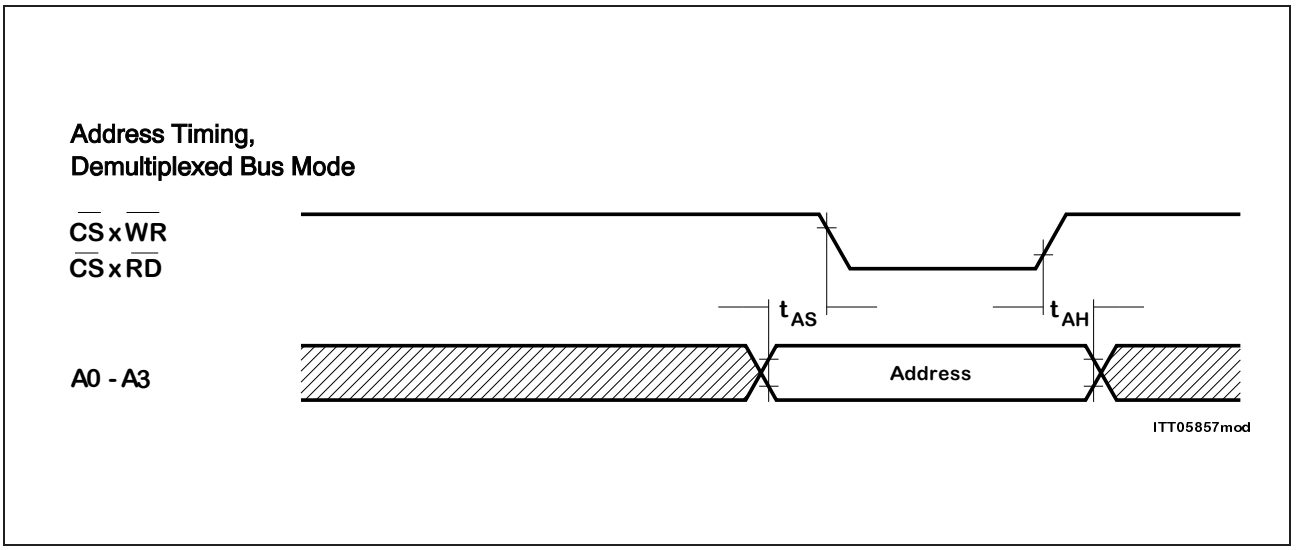


Figure 19 b Siemens/Intel Bus Mode

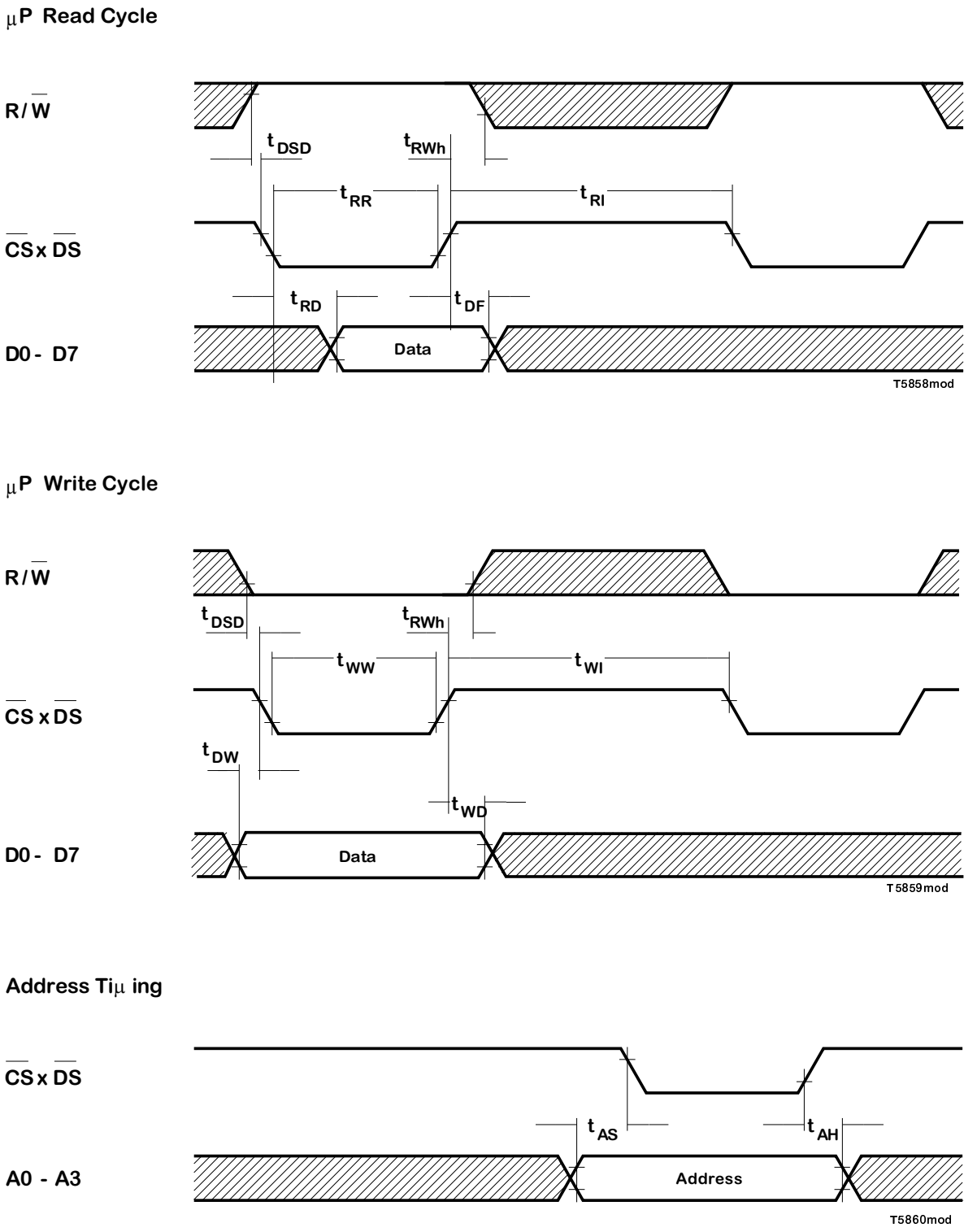


Figure 20 Motorola Bus Mode

PCM and Configurable Interface Timing

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Clock period	t_{CP}	240		ns	clock frequency ≤ 4096 kHz
Clock period low	t_{CPL}	80		ns	
Clock period high	t_{CPH}	100		ns	
Clock period	t_{CP}	120		ns	clock frequency > 4096 kHz
Clock period low	t_{CPL}	50		ns	
Clock period high	t_{CPH}	50		ns	
Frame set-up time to clock	t_{FS}	25		ns	
Frame hold time from clock	t_{FH}	50		ns	
Data clock delay	t_{DCD}		125	ns	
Serial data input set-up time	t_S	7		ns	PCM-input data frequency > 4096 kbit/s
Serial data hold time	t_H	35		ns	
Serial data input set-up time	t_S	15		ns	PCM-input data frequency ≤ 4096 kbit/s
Serial data hold time	t_H	55		ns	
Serial data input set-up time	t_S	20		ns	CFI-input data frequency > 4096 kbit/s
Serial data hold time	t_H	50		ns	
Serial data input set-up time	t_S	0		ns	CFI-input data frequency ≤ 4096 kbit/s
Serial data hold time	t_H	75		ns	
PCM-serial data output delay	t_D		55	ns	
Tristate control delay	t_T		60	ns	
CFI-serial data output delay	t_{CDF}		65	ns	falling clock edge
CFI-serial data output delay	t_{CDR}	–	90	ns	rising clock edge

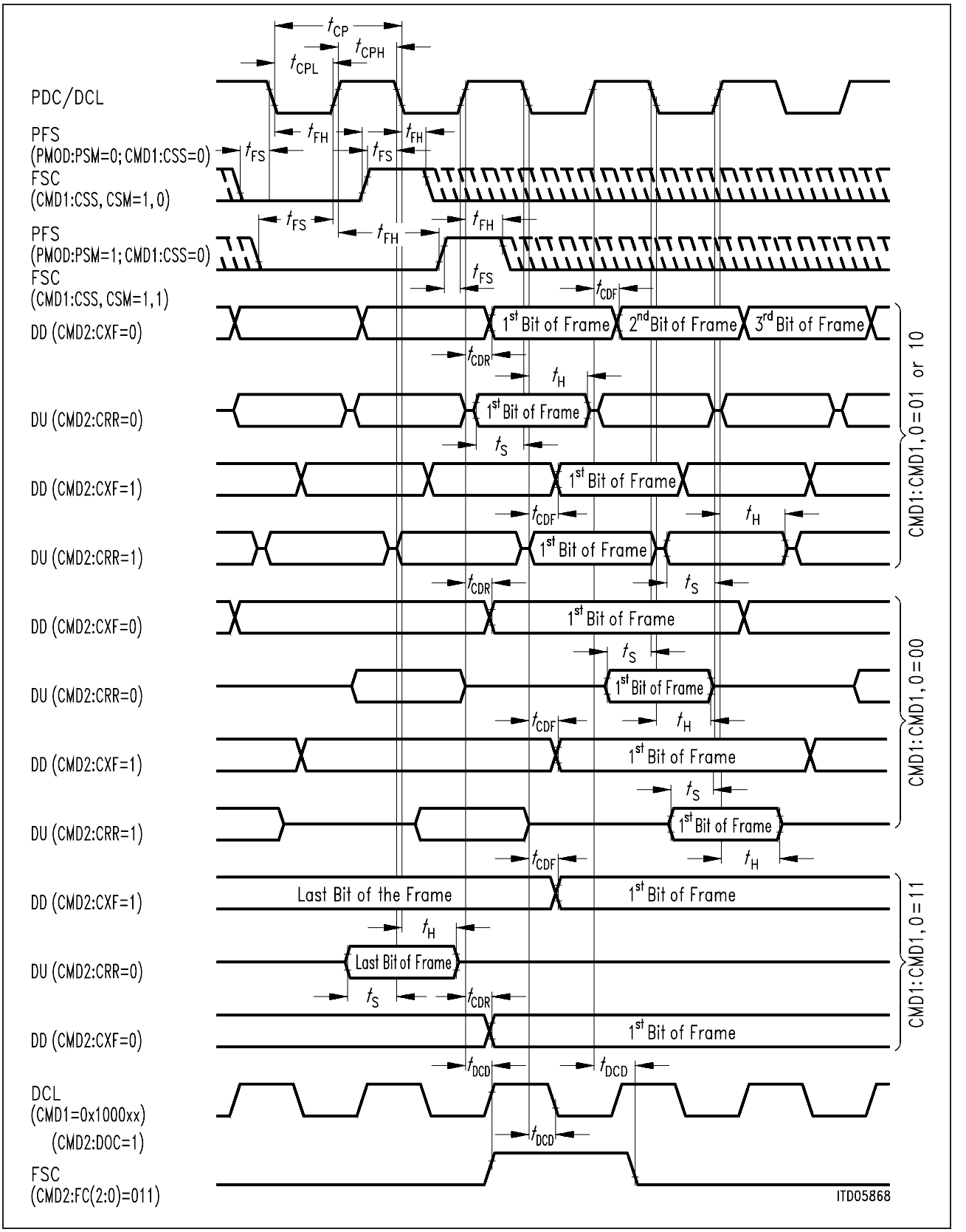


Figure 21 Configurable Interface Timing, CMD:CSP1,0 = 10 (prescalor divisor = 1)

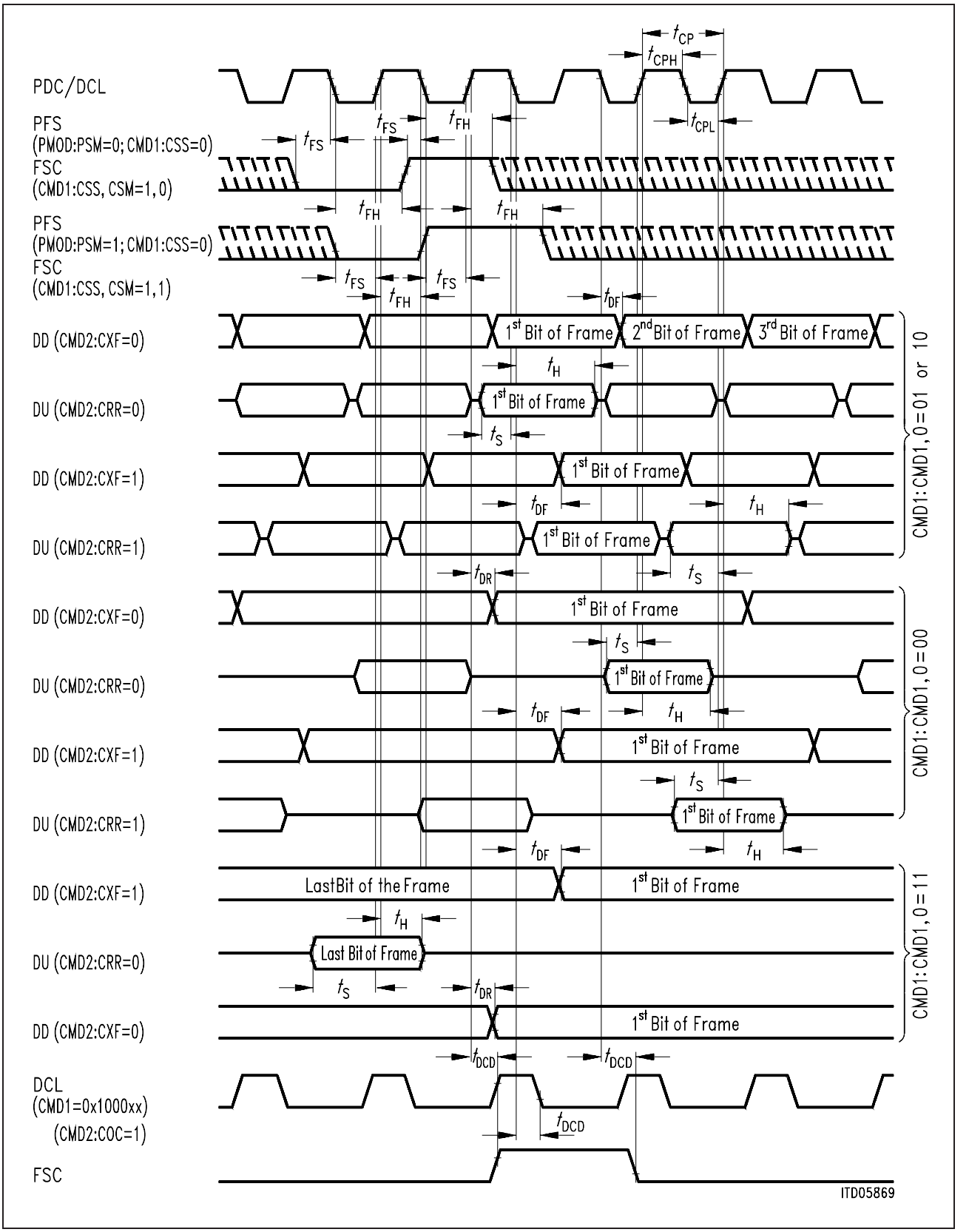


Figure 22 Configurable Interface Timing, CMD:CSP1,0 = 01 (prescalor divisor = 1,5)

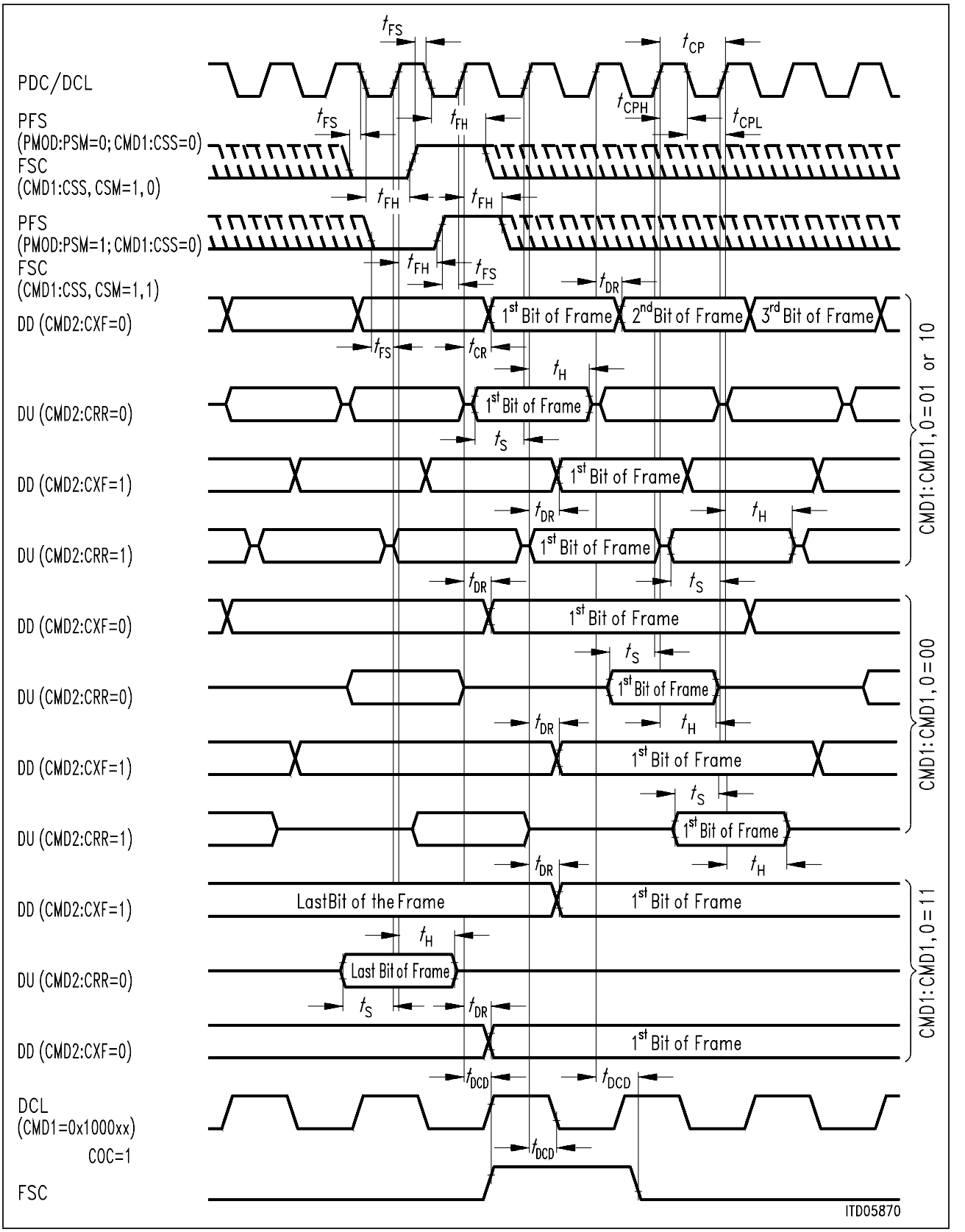


Figure 23 Configurable Interface Timing, CMD:CSP1,0 = 00 (prescalor divisor = 2)

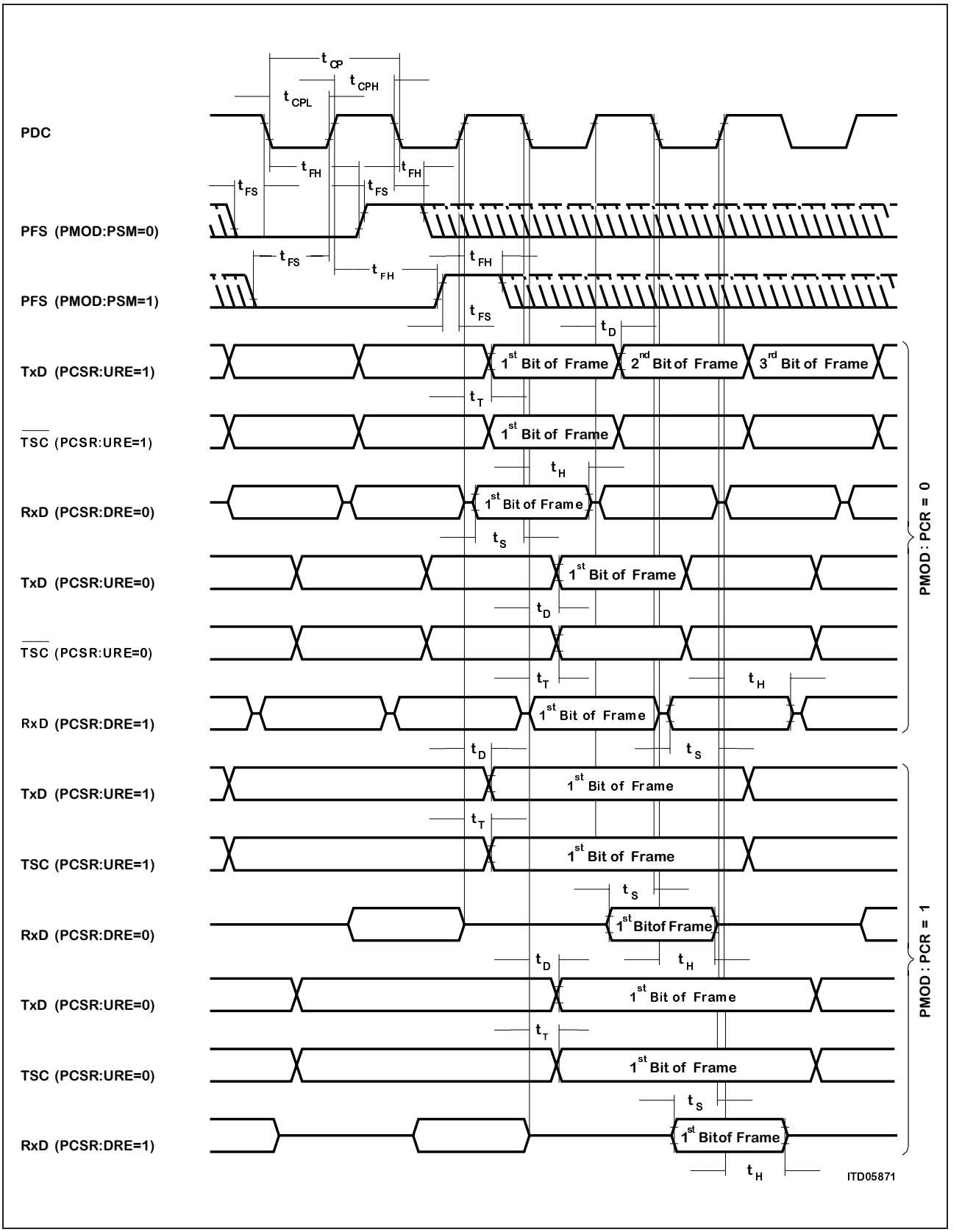
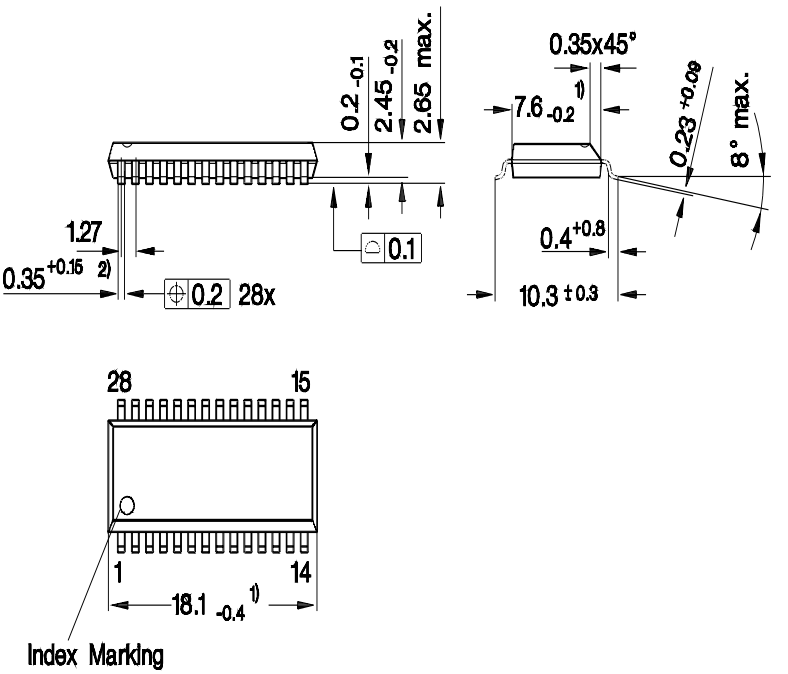


Figure 24 PCM-Interface Timing

7 Package Outlines

P-DSO-28
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm