DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR
μ PA2450C

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA2450C is a switching device, which can be driven directly by a 2.5 V power source.

The μ PA2450C features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

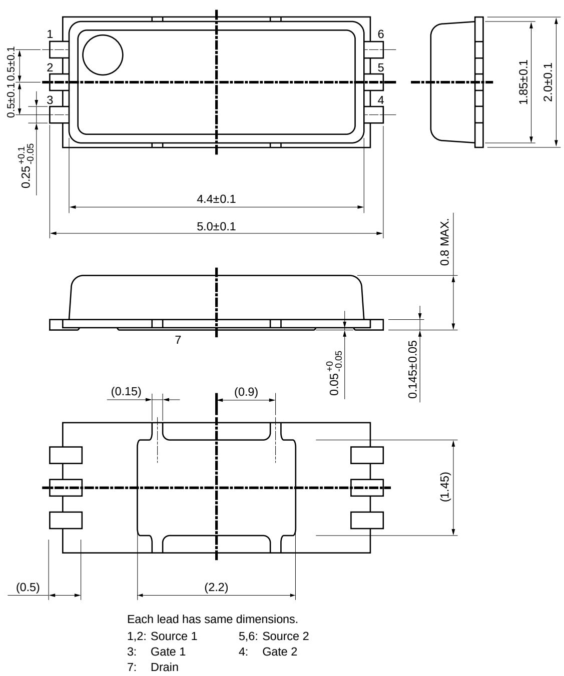
- 2.5 V drive available
- Low on-state resistance
  $R_{DS(on)1}$ = 17.5 mΩ MAX. (V_{GS} = 4.5 V, I_D = 4.0 A)
  $R_{DS(on)2}$ = 18.5 mΩ MAX. (V_{GS} = 4.0 V, I_D = 4.0 A)
  $R_{DS(on)3}$ = 22.0 mΩ MAX. (V_{GS} = 3.1 V, I_D = 4.0 A)
  $R_{DS(on)4}$ = 27.5 mΩ MAX. (V_{GS} = 2.5 V, I_D = 4.0 A)
- Built-in G-S protection diode against ESD

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

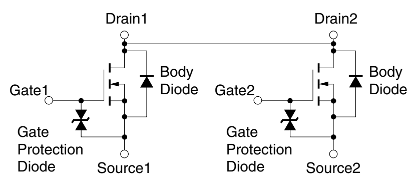
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	20.0	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±12.0	V
Drain Current (DC) Note1	$I_{D(DC)}$	±8.6	A
Drain Current (pulse) Note2	$I_{D(pulse)}$	±70.0	A
Total Power Dissipation (2 units) Note1	P_{T1}	2.5	W
Total Power Dissipation (2 units) Note3	P_{T2}	0.7	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. Mounted on ceramic board of 50 cm^2 x 1.1 mmt
2. PW ≤ 10 μs, Duty Cycle ≤ 1%
3. Mounted on FR-4 board of 50 cm^2 x 1.1 mmt

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2450CTL-E1-A Note	Sn-Bi	Reel 3000 p/reel	6PIN HWSON (4521)
μ PA2450CTL-E2-A Note			

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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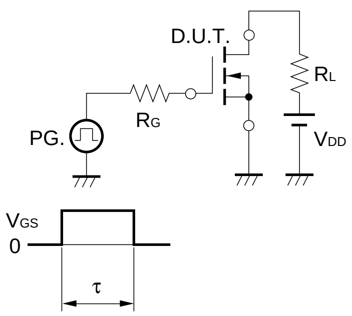
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

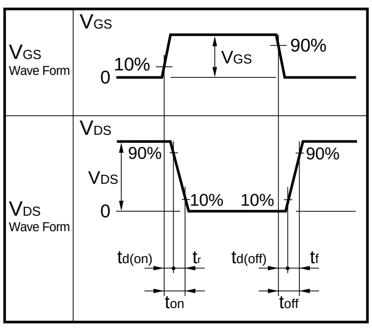
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20.0 V, V_{GS} = 0 V			1.0	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±12.0 V, V_{DS} = 0 V			±10.0	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10.0 V, I_D = 1.0 mA	0.50		1.50	V
Forward Transfer Admittance Note	$\mid y_{fs} \mid$	V_{DS} = 10.0 V, I_D = 4.0 A	3.5			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 4.5 V, I_D = 4.0 A	11.0	12.5	17.5	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 4.0 A	11.5	13.0	18.5	mΩ
	$R_{DS(on)3}$	V_{GS} = 3.1 V, I_D = 4.0 A	12.0	14.5	22.0	mΩ
	$R_{DS(on)4}$	V_{GS} = 2.5 V, I_D = 4.0 A	15.3	18.0	27.5	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10.0 V,		564		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		102		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		64		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 10.0 V,		26.5		ns
Rise Time	t_r	I_D = 4.0 A,		81		ns
Turn-off Delay Time	$t_{d(off)}$	V_{GS} = 4.0 V,		136		ns
Fall Time	t_f	R_G = 6 Ω		97		ns
Total Gate Charge	Q_G	V_{DD} = 16.0 V,		6.0		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 4.0 V,		1.3		nC
Gate to Drain Charge	Q_{GD}	I_D = 8.6 A		2.3		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 8.6 A, V_{GS} = 0 V		0.82		V

Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

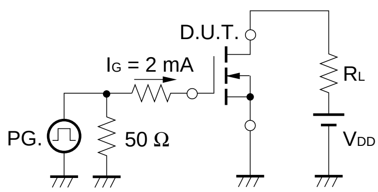
TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

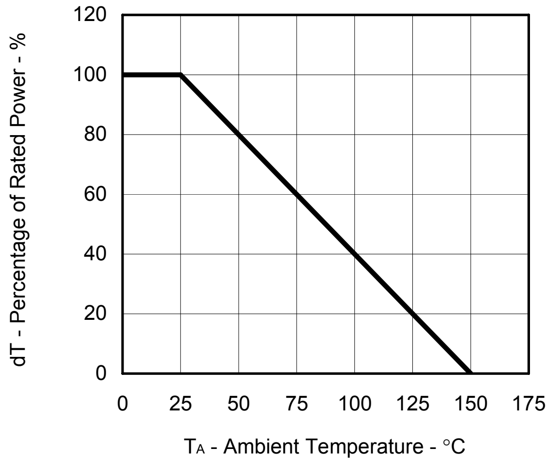


TEST CIRCUIT 2 GATE CHARGE

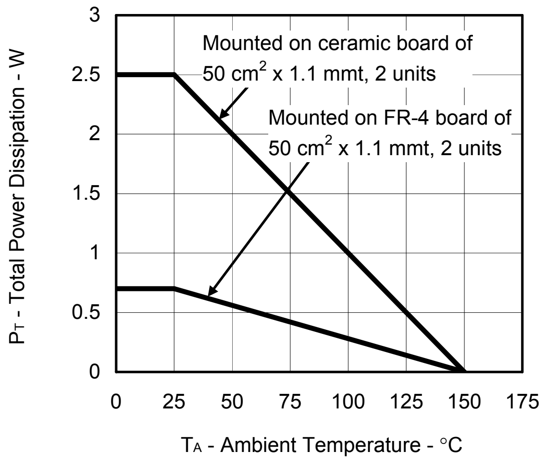


ELECTRICAL CHARACTERISTICS (T_A = 25°C)

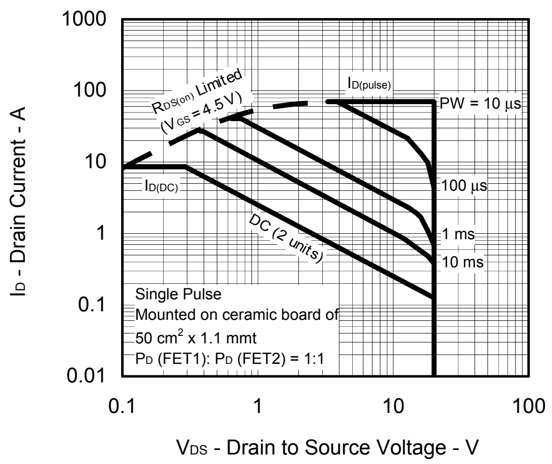
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



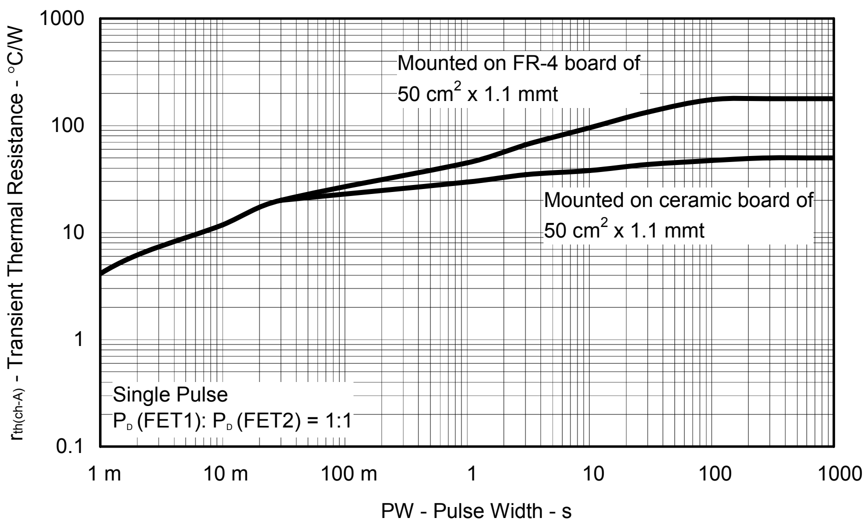
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



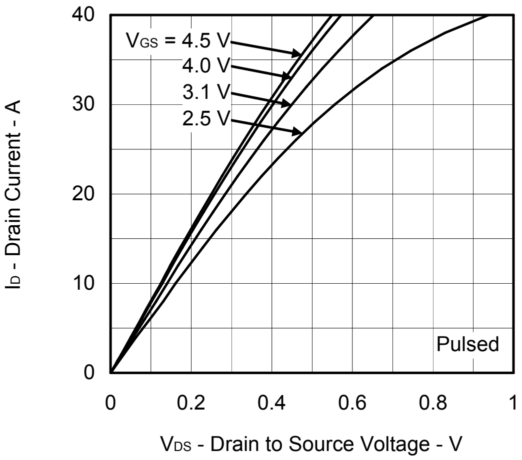
FORWARD BIAS SAFE OPERATING AREA



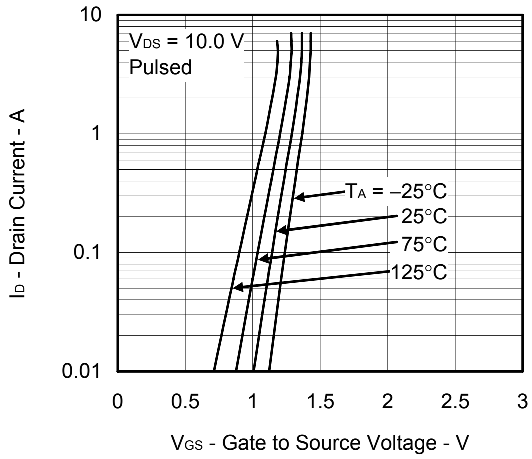
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



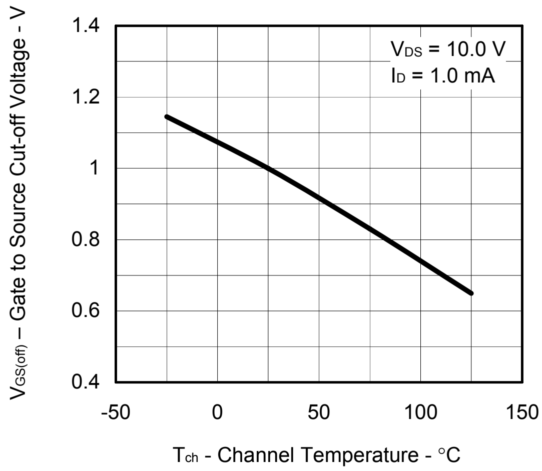
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



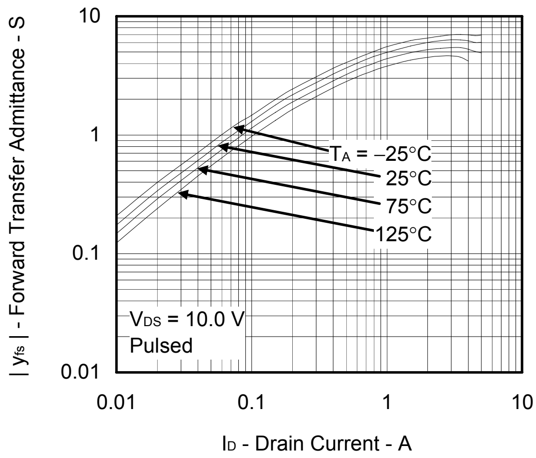
FORWARD TRANSFER CHARACTERISTICS



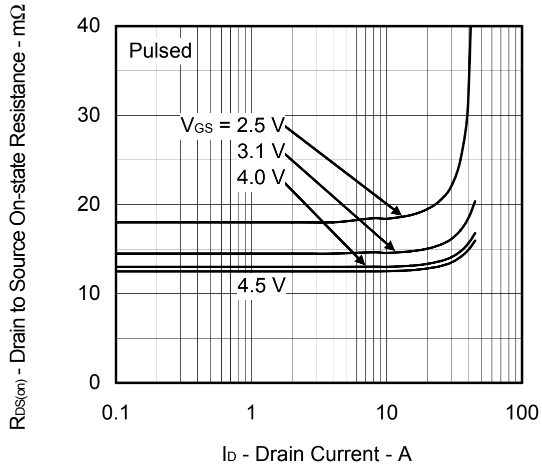
GATE TO SOURE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



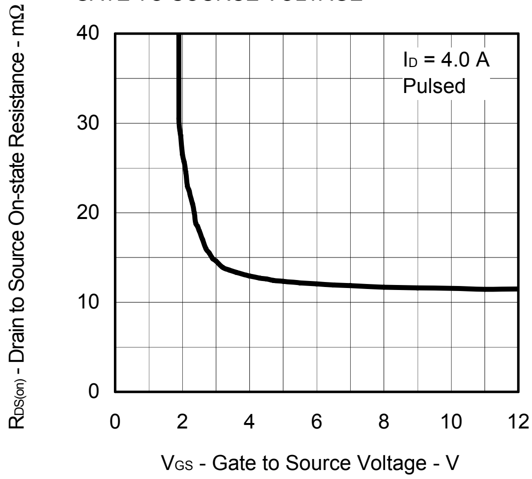
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



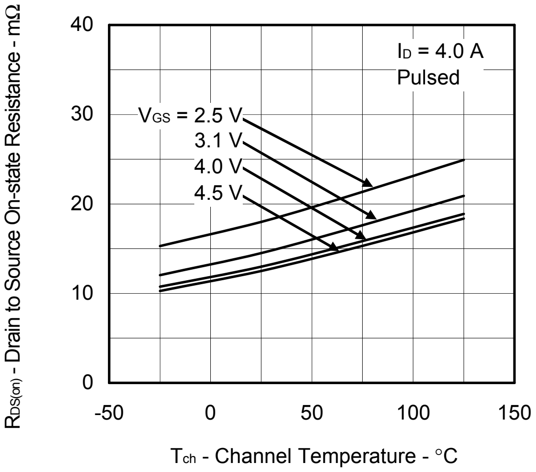
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



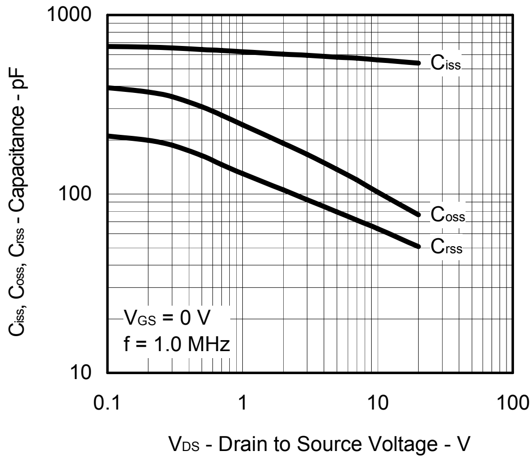
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



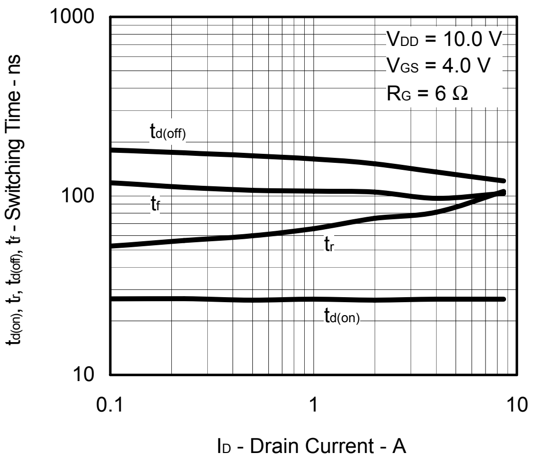
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



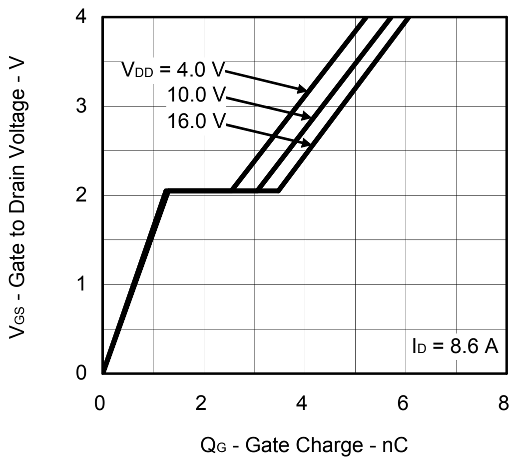
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



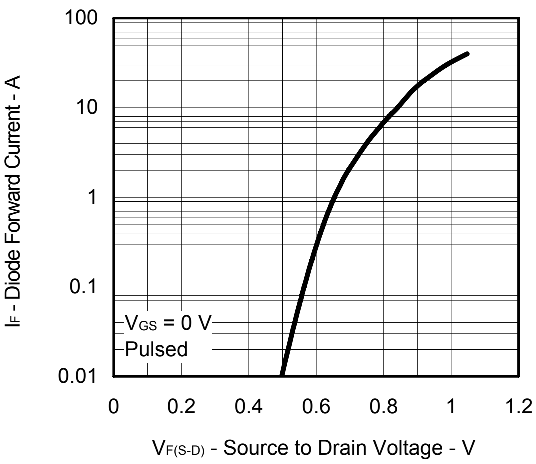
SWITCHING CHARACTERISTICS



DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



<Notes for using this device safely>

When you use this device, in order to prevent a customer's hazard and damage, use it with understanding the following contents. If used exceeding recommended conditions, there is a possibility of causing failure of the device and characteristic degradation.

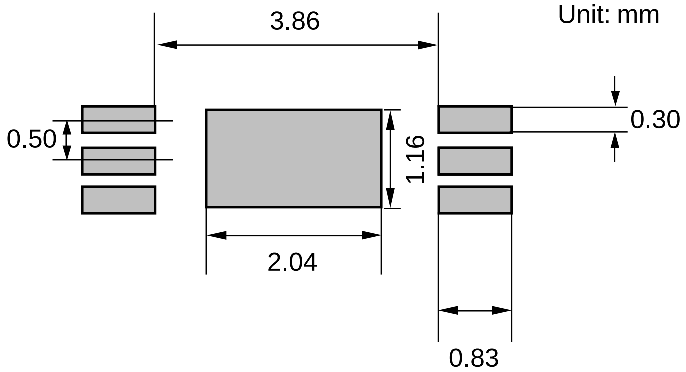
1. When you mount the device on a substrate, carry out within our recommended soldering conditions of infrared reflow. If mounted exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.

2. When you wash the device mounted the substrate, carry out within our recommended conditions. If washed exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.

3. When you use ultrasonic wave to substrate after the device mounting, prevent from touching a resonance generator directly. If it touches, the characteristic of a device may be degraded and it may result in failure.

4. Please refer to **Figure 1** as an example of the land pattern. Optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.

Figure 1. Example of the land pattern



5. This device is very thin device and should be handled with caution for mechanical stress. The rate of distortion applied to the device should become below 2000 $\mu\varepsilon$.[Note1] If the rate of distortion exceeds 2000 $\mu\varepsilon$, the characteristic of a device may be degraded and it may result in failure.

Figure 2. Direction of substrate and stress

The substrate that mounted the device is on a stand with a support width of 24 mm.

The device is turned downward. The stress is applied from a top.

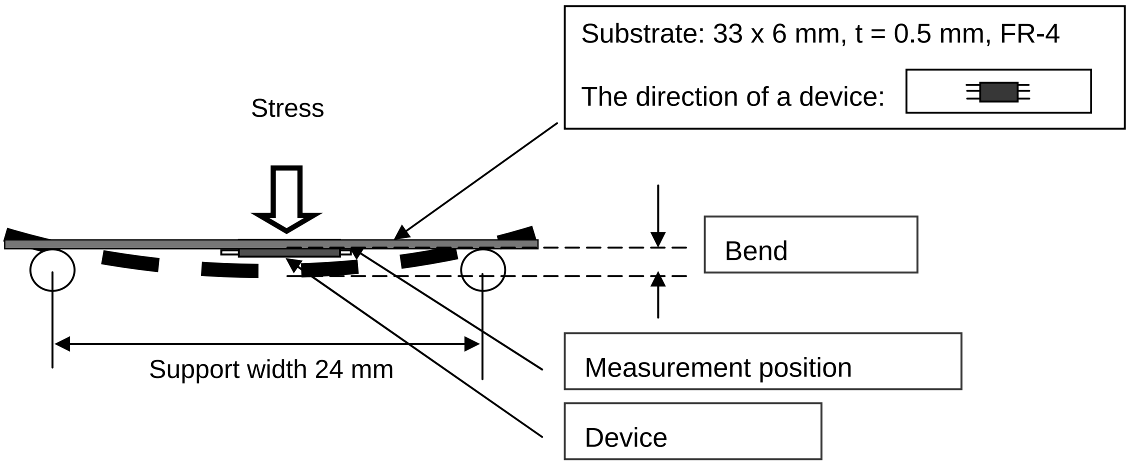
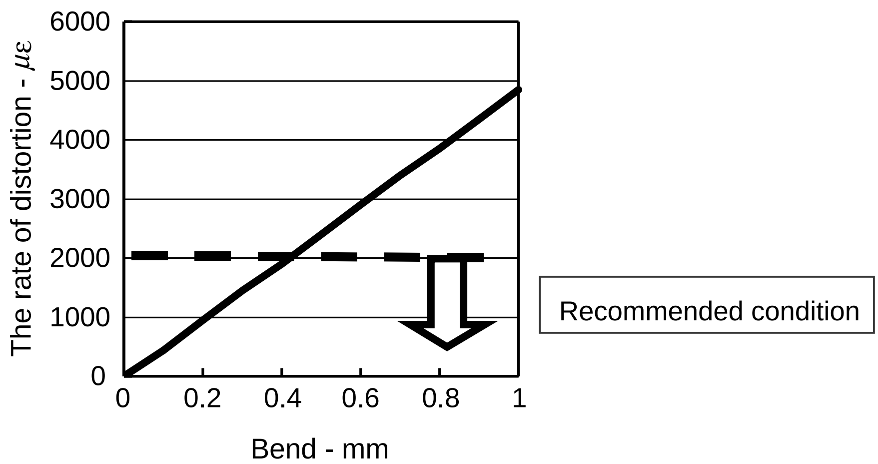


Figure 3. Example of the bend and the rate of distortion[Note2]



Note 1. Definition of rate of distortion(written as ε in this document)

$\varepsilon = (l - l_0)/l_0$

l_0: Distance for two arbitrary points before receiving stress.

l: Distance above-mentioned when receiving stress.

2. The relation of the distortion and the bend changes with several conditions, such as a size of substrate and so on.