

**+5V Powered RS-232
Transmitters/Receivers**

The HIN232-HIN241 family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232E and V.28 specifications, and are particularly suited for those applications where $\pm 12V$ is not available. They require a single +5V power supply (except HIN239) and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The family of devices offer a wide variety of RS-232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300 Ω power-off source impedance. The receivers can handle up to $\pm 30V$, and have a 3k Ω to 7k Ω input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Features

- Meets All RS-232E and V.28 Specifications
- Requires Only Single +5V Power Supply
 - (+5V and +12V - HIN239)
- High Data Rate. 120kbps
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- Low Power Shutdown Function
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
 - $\pm 10V$ Output Swing for 5V Input
 - 300 Ω Power-Off Source Impedance
 - Output Current Limiting
 - TTL/CMOS Compatible
 - 30V/ μs Maximum Slew Rate
- Multiple Receivers
 - $\pm 30V$ Input Voltage Range
 - 3k Ω to 7k Ω Input Impedance
 - 0.5V Hysteresis to Improve Noise Rejection
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Any System Requiring RS-232 Communication Ports
 - Computer - Portable, Mainframe, Laptop
 - Peripheral - Printers and Terminals
 - Instrumentation
 - Modems

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	EXTERNAL COMPONENTS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF LEADS
HIN232	+5V	2	2	4 Capacitors	No/No	16
HIN236	+5V	4	3	4 Capacitors	Yes/Yes	24
HIN237	+5V	5	3	4 Capacitors	No/No	24
HIN238	+5V	4	4	4 Capacitors	No/No	24
HIN239	+5V and +7.5V to 13.2V	3	5	2 Capacitors	No/Yes	24
HIN240	+5V	5	5	4 Capacitors	Yes/Yes	44
HIN241	+5V	4	5	4 Capacitors	Yes/Yes	28

Pin Descriptions

PIN	FUNCTION
V _{CC}	Power Supply Input 5V ±10%.
V+	Internally generated positive supply (+10V nominal), HIN239 requires +7.5V to +13.2V.
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T _{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V _{CC} is connected to each lead.
T _{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R _{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R _{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{\text{EN}}$	Enable input. This is an active low input which enables the receiver outputs. With $\overline{\text{EN}} = 5\text{V}$, the receiver outputs are placed in a high impedance state.
SD	Shutdown Input. With SD = 5V, the charge pump is disabled, the receiver outputs are in a high impedance state and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIN232CB	232CB	0 to 70	16 Ld SOIC	M16.3
HIN232CB-T	232CB	0 to 70	Tape and Reel	
HIN232CBZ (See Note)	232CBZ	0 to 70	16 Ld SOIC (Pb-free)	M16.3
HIN232CBZ-T (See Note)	232CBZ	0 to 70	Tape and Reel (Pb-free)	
HIN232CP	HIN232CP	0 to 70	16 Ld PDIP	E16.3
HIN232CPZ (See Note)	HIN232CPZ	0 to 70	16 Ld PDIP* (Pb-free)	E16.3
HIN232IB	232IB	-40 to 85	16 Ld SOIC	M16.3
HIN232IB-T	232IB	-40 to 85	Tape and Reel	
HIN232IBZ (See Note)	232IBZ	-40 to 85	16 Ld SOIC (Pb-free)	M16.3
HIN232IBZ-T (See Note)	232IBZ	-40 to 85	Tape and Reel (Pb-free)	
HIN232IP	HIN232IP	-40 to 85	16 Ld PDIP	E16.3
HIN232IPZ (See Note)	HIN232IPZ	-40 to 85	16 Ld PDIP* (Pb-free)	E16.3
HIN236CB	236CB	0 to 70	24 Ld SOIC	M24.3
HIN236CBZ (See Note)	236CBZ	0 to 70	24 Ld SOIC (Pb-free)	M24.3
HIN237CB	237CB	0 to 70	24 Ld SOIC	M24.3
HIN237CB-T	237CB	0 to 70	Tape and Reel	
HIN237CBZ (See Note)	237CBZ	0 to 70	24 Ld SOIC (Pb-free)	M24.3
HIN237CBZ-T (See Note)	237CBZ	0 to 70	Tape and Reel (Pb-free)	
HIN238CB	238CB	0 to 70	24 Ld SOIC	M24.3
HIN238CB-T	238CB	0 to 70	Tape and Reel	
HIN238CBZ (See Note)	238CBZ	0 to 70	24 Ld SOIC (Pb-free)	M24.3
HIN238CBZ-T (See Note)	238CBZ	0 to 70	Tape and Reel (Pb-free)	
HIN238CP	HIN238CP	0 to 70	24 Ld PDIP	E24.3
HIN238CPZ (See Note)	HIN238CPZ	0 to 70	24 Ld PDIP* (Pb-free)	E24.3
HIN238IB	238IB	-40 to 85	24 Ld SOIC	M24.3
HIN238IBZ (See Note)	238IBZ	-40 to 85	24 Ld SOIC (Pb-free)	M24.3
HIN239CB	239CB	0 to 70	24 Ld SOIC	M24.3
HIN239CB-T	239CB	0 to 70	Tape and Reel	
HIN239CBZ (See Note)	239CBZ	0 to 70	24 Ld SOIC (Pb-free)	M24.3
HIN239CBZ-T (See Note)	239CBZ	0 to 70	Tape and Reel (Pb-free)	
HIN239CP	HIN239CP	0 to 70	24 Ld PDIP	E24.3

Ordering Information (Continued)

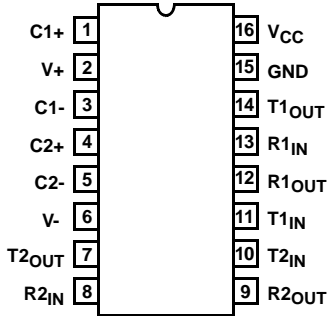
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIN239CPZ (See Note)	HIN239CPZ	0 to 70	24 Ld PDIP* (Pb-free)	E24.3
HIN240CN	HIN240CN	0 to 70	44 Ld MQFP	Q44.10X10
HIN240CNZ (See Note)	HIN240CNZ	0 to 70	44 Ld MQFP (Pb-free)	Q44.10X10
HIN240CNZ-T (See Note)	HIN240CNZ	0 to 70	44 Ld MQFP Tape and Reel (Pb-free)	
HIN241CA	HIN241CA	0 to 70	28 Ld SSOP	M28.209
HIN241CAZ (See Note)	HIN241CAZ	0 to 70	28 Ld SSOP (Pb-free)	M28.209
HIN241CB	241CB	0 to 70	28 Ld SOIC	M28.3
HIN241CB-T	241CB	0 to 70	Tape and Reel	
HIN241CBZ (See Note)	241CBZ	0 to 70	28 Ld SOIC (Pb-free)	M28.3
HIN241CBZ-T (See Note)	241CBZ	0 to 70	Tape and Reel (Pb-free)	
HIN241IB	241IB	-40 to 85	28 Ld SOIC	M28.3
HIN241IBZ (See Note)	241IBZ	-40 to 85	28 Ld SOIC (Pb-free)	M28.3

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

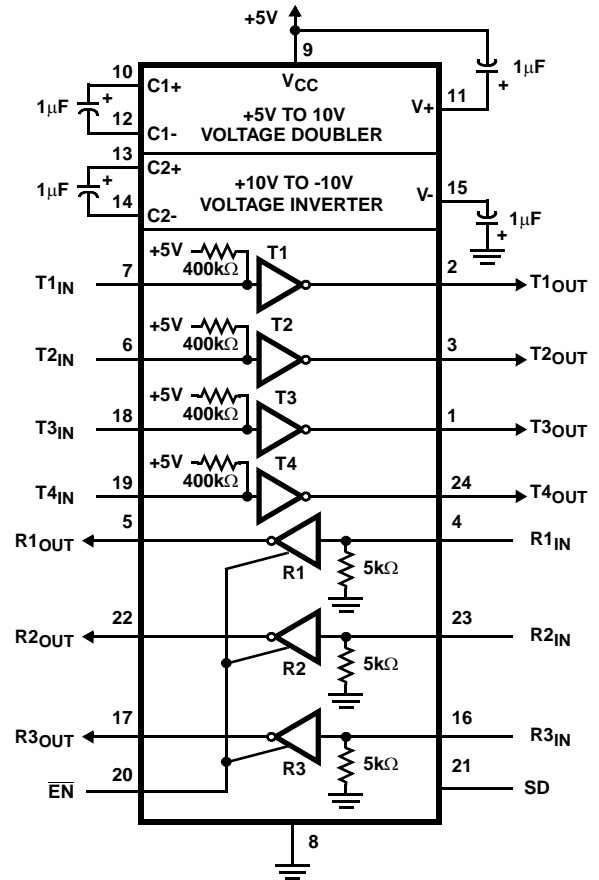
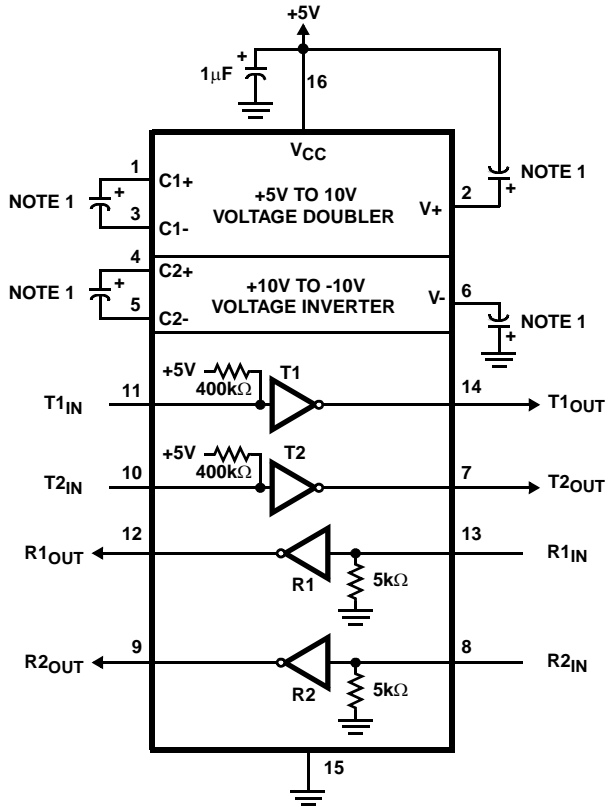
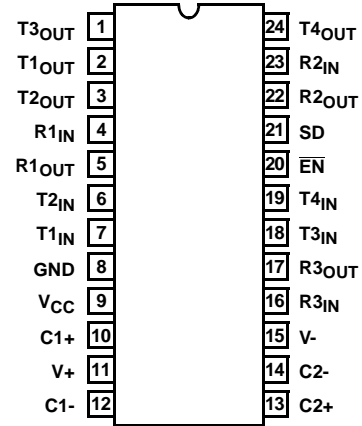
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Pinouts

HIN232 (PDIP, SOIC)
TOP VIEW



HIN236 (SOIC)
TOP VIEW

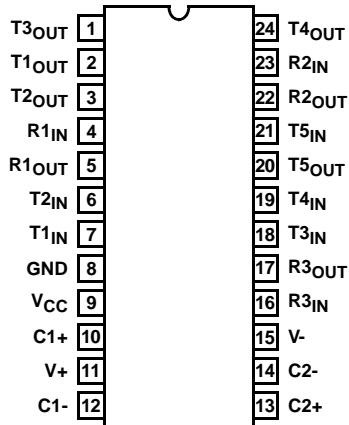


NOTE:

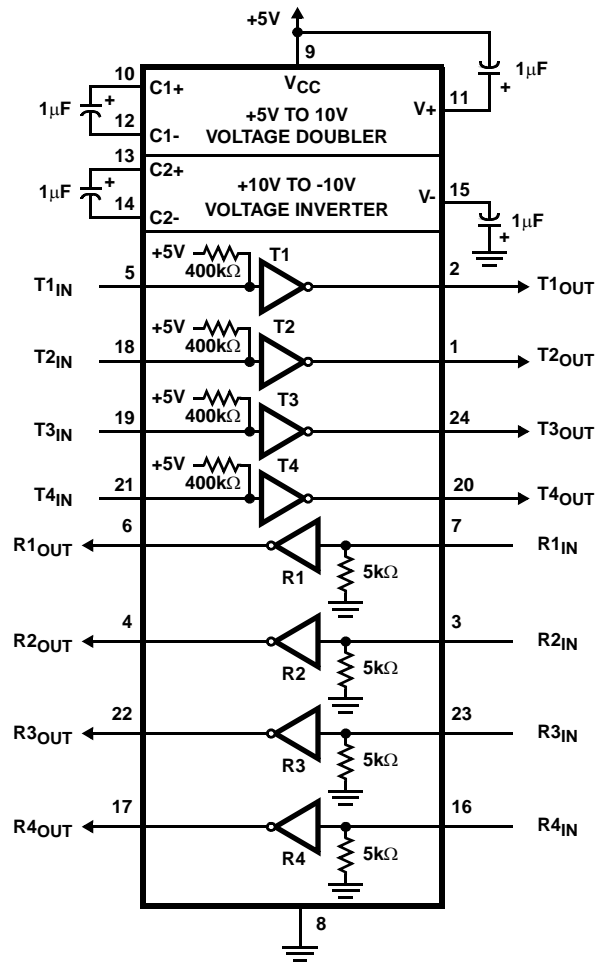
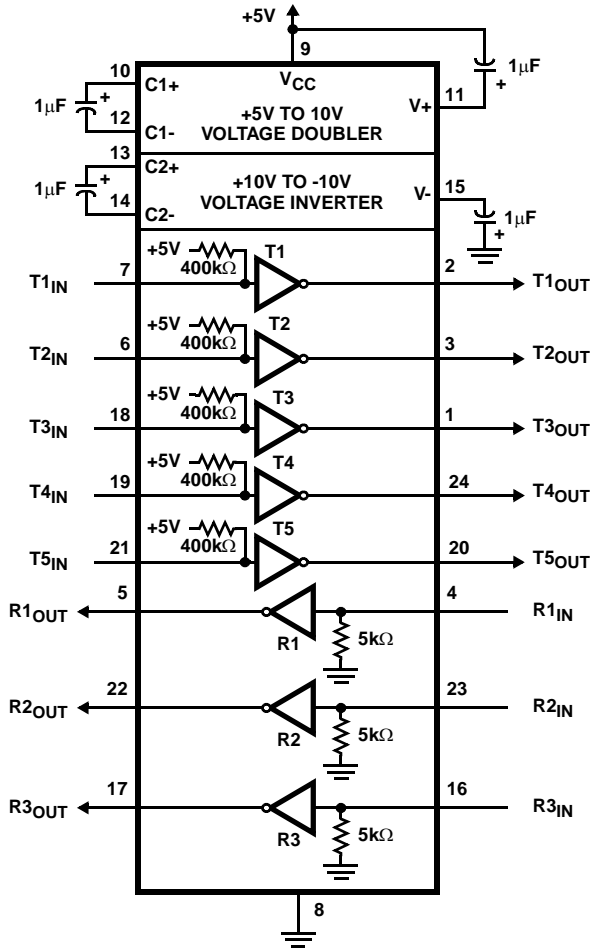
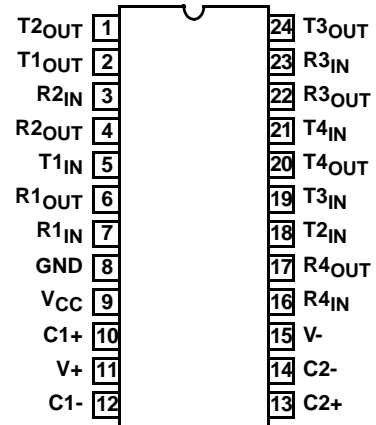
1. Either 0.1µF or 1µF capacitors may be used. The V+ capacitor may be terminated to V_{CC} or to GND.

Pinouts (Continued)

HIN237 (SOIC)
TOP VIEW

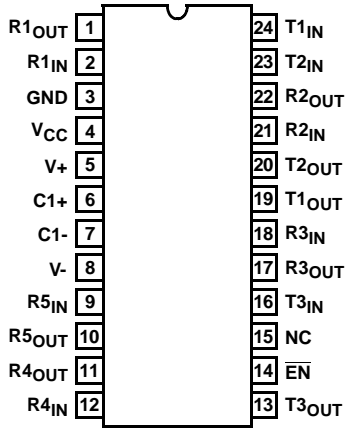


HIN238 (PDIP, SOIC)
TOP VIEW

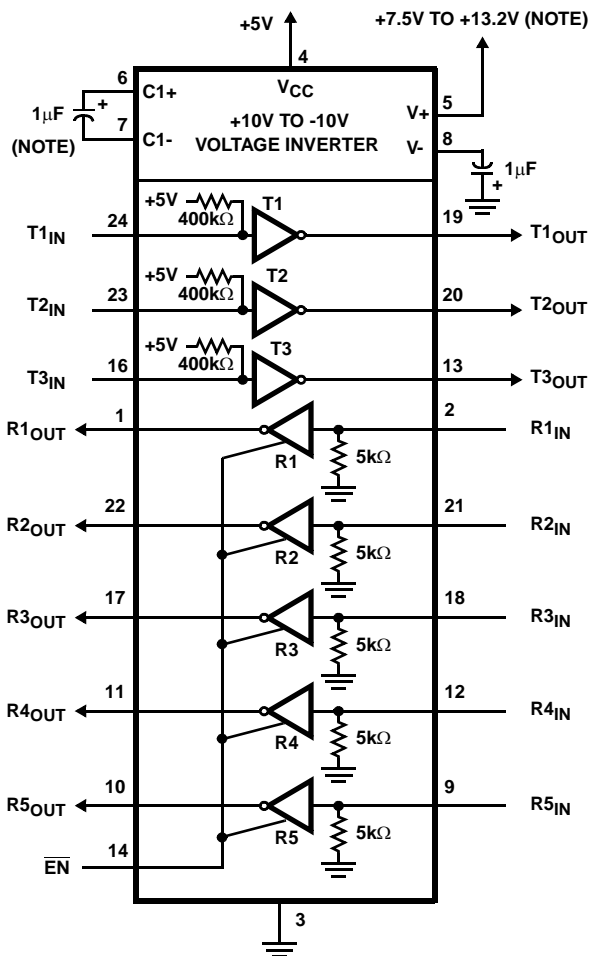
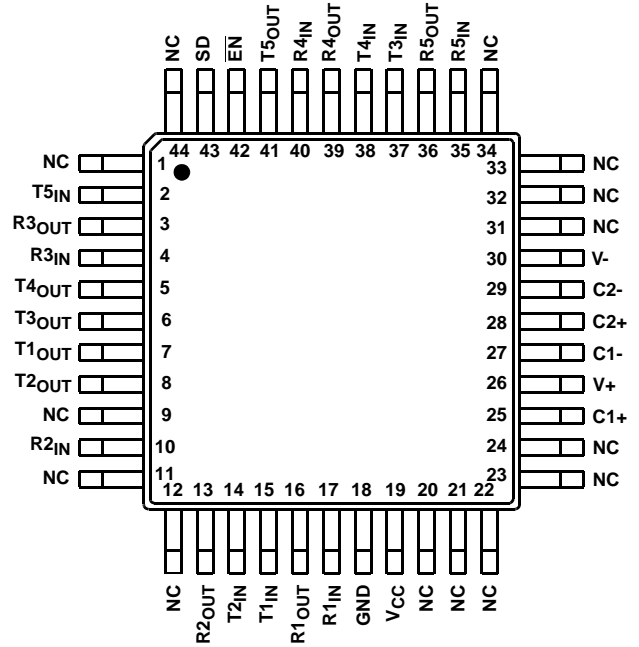


Pinouts (Continued)

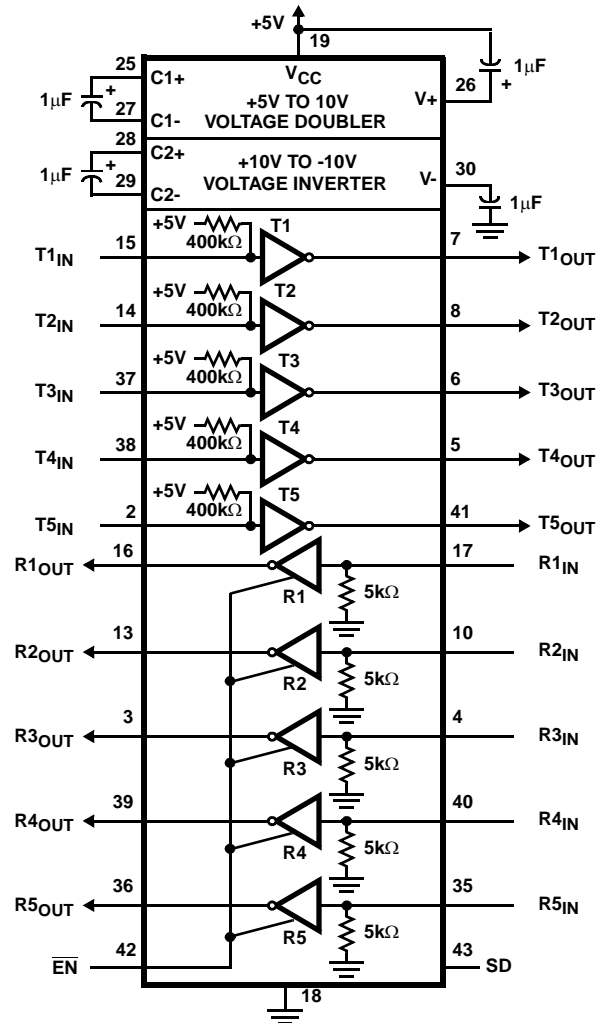
HIN239 (PDIP, SOIC)
TOP VIEW



HIN240 (MQFP)

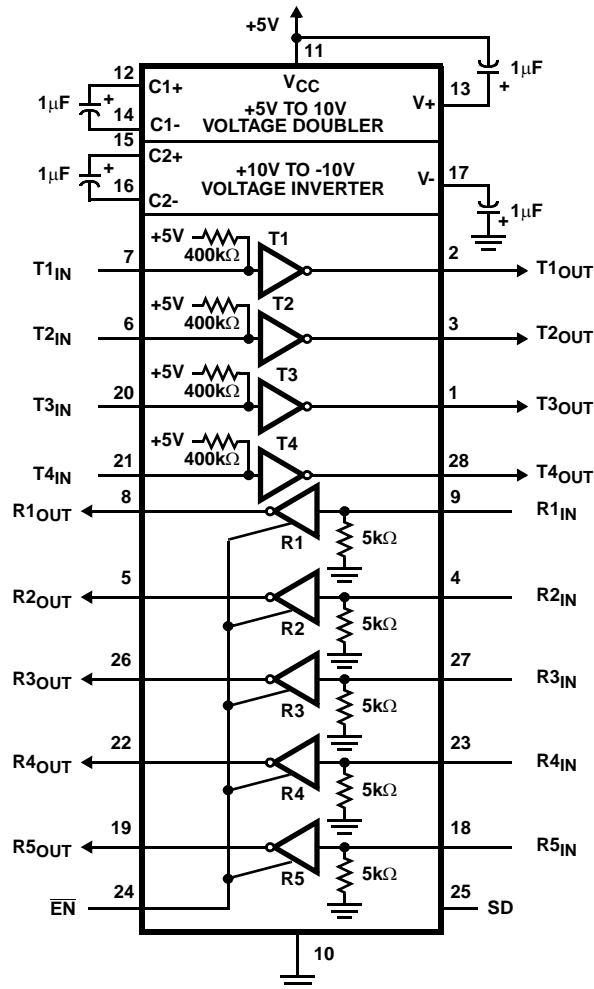
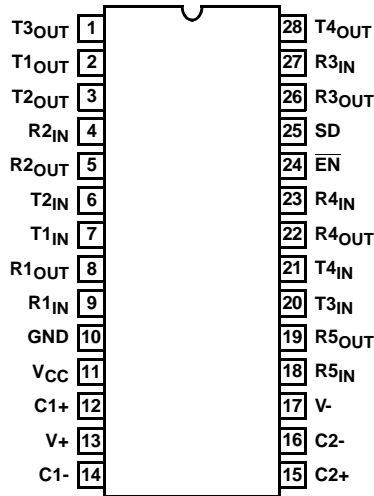


NOTE: For $V_+ > 11V$, use $C_1 \leq 0.1\mu F$.



Pinouts (Continued)

HIN241 (SOIC, SSOP)
TOP VIEW



Absolute Maximum Ratings

V_{CC} to Ground. (GND -0.3V) < V_{CC} < 6V
 V+ to Ground (Note 2) (V_{CC} -0.3V) < V+ < 13.2V
 V- to Ground. -12V < V- < (GND +0.3V)
 V+ to V- 24V
 Input Voltages
 T_{IN} -0.3V < V_{IN} < (V+ +0.3V)
 R_{IN} ±30V
 Output Voltages
 T_{OUT} (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
 R_{OUT} (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
 Short Circuit Duration
 T_{OUT} Continuous
 R_{OUT} Continuous

Operating Conditions

Temperature Range
 HIN2XXCX 0°C to 70°C
 HIN2XXIX -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- Only HIN239. For V+ > 11V, C1 must be ≤0.1μF.
- θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)

16 Ld PDIP Package*	90
24 Ld PDIP Package	70
16 Ld SOIC Package	100
24 Ld SOIC Package	75
28 Ld SOIC Package	70
28 Ld SSOP Package	95
44 Ld MQFP Package	80

Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (SOIC, SSOP, MQFP - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Electrical Specifications Test Conditions: V_{CC} = +5V ±10%, T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
SUPPLY CURRENTS						
Power Supply Current, I _{CC}	No Load, T _A = 25°C	HIN232	-	5	10	mA
		HIN236-HIN238, HIN240-HIN241	-	7	15	mA
		HIN239	-	0.4	1	mA
V+ Power Supply Current, I _{CC} No Load, T _A = 25°C	No Load, T _A = 25°C	HIN239	-	5.0	15	mA
Shutdown Supply Current, I _{CC} (SD)	T _A = 25°C	-	1	10	μA	
LOGIC AND TRANSMITTER INPUTS, RECEIVER OUTPUTS						
Input Logic Low, V _{IL}	T _{IN} , \overline{EN} , Shutdown	-	-	0.8	V	
Input Logic High, V _{IH}	T _{IN}	2.0	-	-	V	
	\overline{EN} , Shutdown	2.4	-	-	V	
Transmitter Input Pullup Current, I _P	T _{IN} = 0V	-	15	200	μA	
TTL/CMOS Receiver Output Voltage Low, V _{OL}	I _{OUT} = 1.6mA	-	0.1	0.4	V	
TTL/CMOS Receiver Output Voltage High, V _{OH}	I _{OUT} = -1.0mA	3.5	4.6	-	V	
RECEIVER INPUTS						
RS-232 Input Voltage Range V _{IN}		-30	-	+30	V	
Receiver Input Impedance R _{IN}	V _{IN} = ±3V	3.0	5.0	7.0	kΩ	
Receiver Input Low Threshold, V _{IN} (H-L)	V _{CC} = 5V, T _A = 25°C	0.8	1.2	-	V	
Receiver Input High Threshold, V _{IN} (L-H)	V _{CC} = 5V, T _A = 25°C	-	1.7	2.4	V	
Receiver Input Hysteresis V _{HYST}		0.2	0.5	1.0	V	

Electrical Specifications Test Conditions: $V_{CC} = +5V \pm 10\%$, $T_A =$ Operating Temperature Range (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS					
Baud Rate (1 Transmitter Switching)	$R_L = 3k\Omega$	120	-	-	kbps
Output Enable Time, t_{EN}	HIN236, HIN239, HIN240, HIN241	-	400	-	ns
Output Disable Time, t_{DIS}	HIN236, HIN239, HIN240, HIN241	-	250	-	ns
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	μs
Instantaneous Slew Rate SR	$C_L = 10pF$, $R_L = 3k\Omega$, $T_A = 25^\circ C$ (Note 4)	-	-	30	$V/\mu s$
Transition Region Slew Rate, SR_T	$R_L = 3k\Omega$, $C_L = 2500pF$ Measured from +3V to -3V or -3V to +3V, 1 Transmitter Switching	-	3	-	$V/\mu s$
TRANSMITTER OUTPUTS					
Output Voltage Swing, T_{OUT}	Transmitter Outputs, $3k\Omega$ to Ground	± 5	± 9	± 10	V
Output Resistance, T_{OUT}	$V_{CC} = V_+ = V_- = 0V$, $V_{OUT} = \pm 2V$	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} shorted to GND	-	± 10	-	mA

NOTE:

- 4. Guaranteed by design.

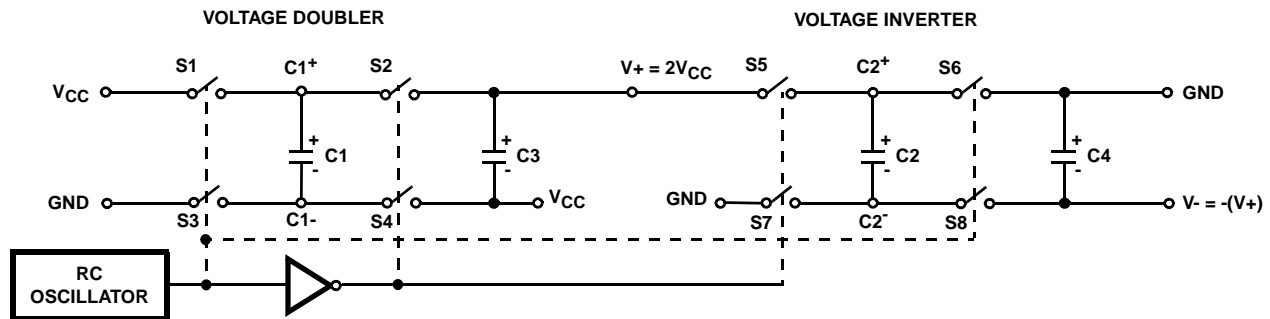


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN232 thru HIN241 family of RS-232 transmitters/receivers are powered by a single +5V power supply (except HIN239), feature low power consumption, and meet all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: The charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC} . During phase two, the voltage on C1 is added to V_{CC} , producing a signal across C3 equal to twice V_{CC} . During phase one, C2 is also charged to $2V_{CC}$, and then during phase two, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up

to 5.5V. The output impedance of the voltage doubler section (V_+) is approximately 200Ω , and the output impedance of the voltage inverter section (V_-) is approximately 450Ω . A typical application uses $1\mu F$ capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V_+ and V_- supplies.

During shutdown mode (HIN236, HIN240 and HIN241), SHUTDOWN control line set to logic "1", the charge pump is turned off, V_+ is pulled down to V_{CC} , V_- is pulled up to GND, and the supply current is reduced to less than $10\mu A$. The transmitter outputs are disabled and the receiver outputs are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC} , or 1.3V for $V_{CC} = 5V$. A logic 1 at the input results in a voltage of between -5V and V^- at the output, and a logic 0 results in a voltage between +5V and $(V^+ - 0.6V)$. Each transmitter input has an internal 400k Ω pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of $\pm 5V$ minimum with the worst case conditions of: all transmitters driving 3k Ω minimum load impedance, $V_{CC} = 4.5V$, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/ μs . The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300 Ω with $\pm 2V$ applied to the outputs and $V_{CC} = 0V$.

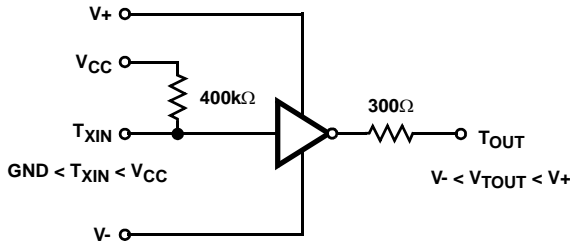


FIGURE 2. TRANSMITTER

Receivers

The receiver inputs accept up to $\pm 30V$ while presenting the required 3k Ω to 7k Ω input impedance even if the power is off ($V_{CC} = 0V$). The receivers have a typical input threshold of 1.3V which is within the $\pm 3V$ limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC} . The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection. The receiver Enable line \overline{EN} , when set to logic "1", (HIN236, 239, 240, and 241) disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode.

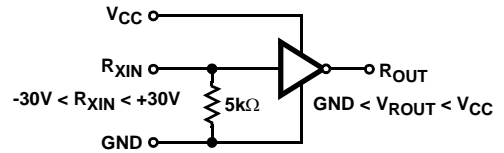
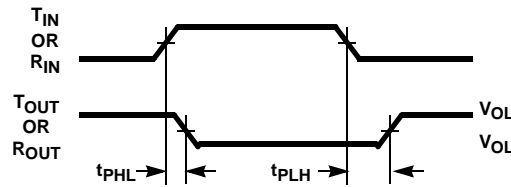


FIGURE 3. RECEIVER



$$\text{Average Propagation Delay} = \frac{t_{PHL} + t_{PLH}}{2}$$

FIGURE 4. PROPAGATION DELAY DEFINITION

Typical Performance Curves

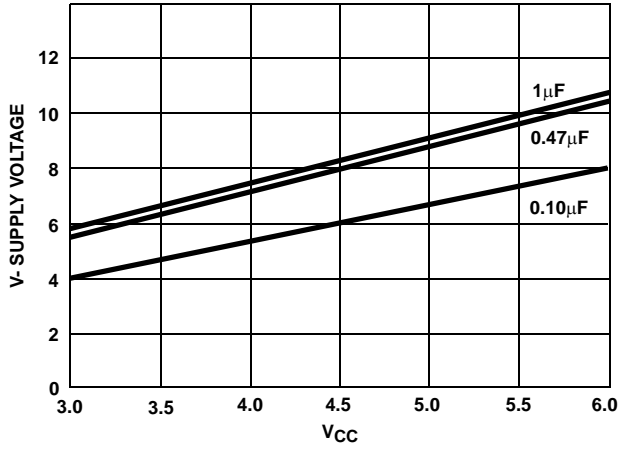


FIGURE 5. V- SUPPLY VOLTAGE vs V_{CC} , VARYING CAPACITORS

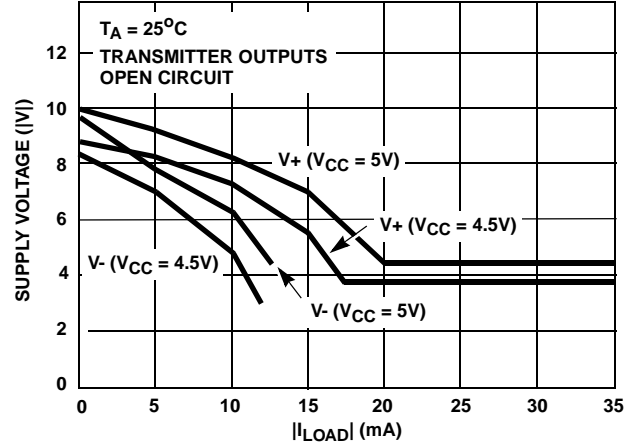


FIGURE 6. V_+ , V_- OUTPUT VOLTAGE vs LOAD (HIN232)

Test Circuits (HIN232)

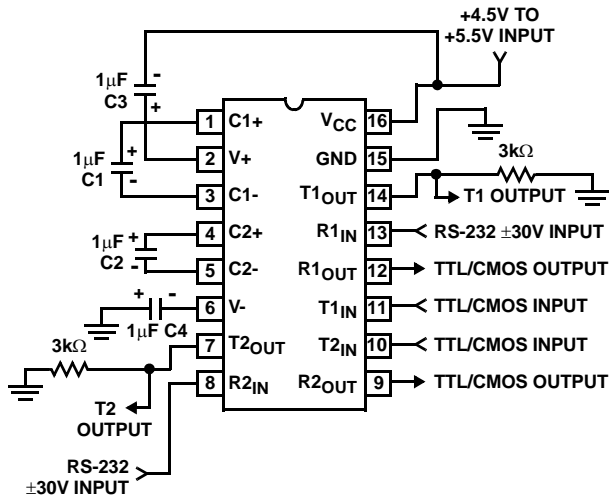


FIGURE 7. GENERAL TEST CIRCUIT

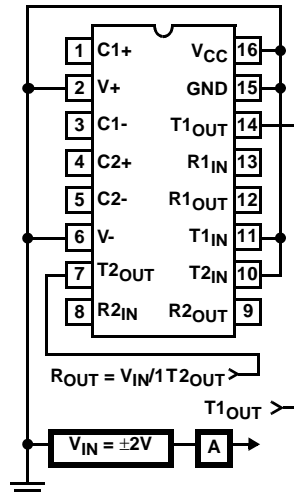


FIGURE 8. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Applications

The HIN2XX may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where $\pm 12V$ power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRs (data signaling rate select) is generated by driving them through a $5k\Omega$ resistor connected to $V+$.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors ($C1$ and $C2$) but can share common reservoir capacitors ($C3$ and $C4$). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

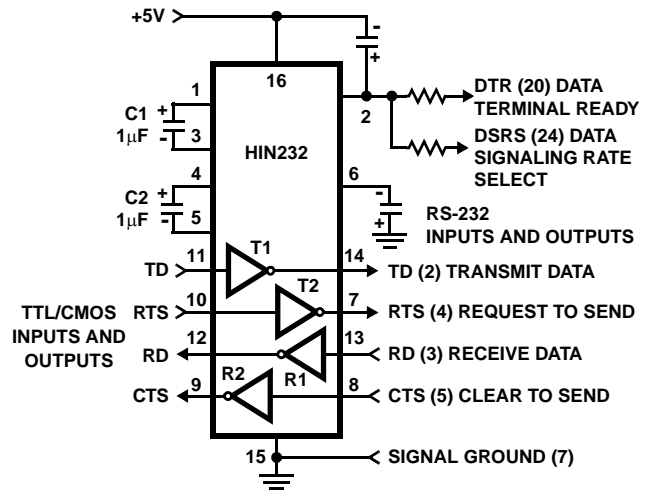


FIGURE 9. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

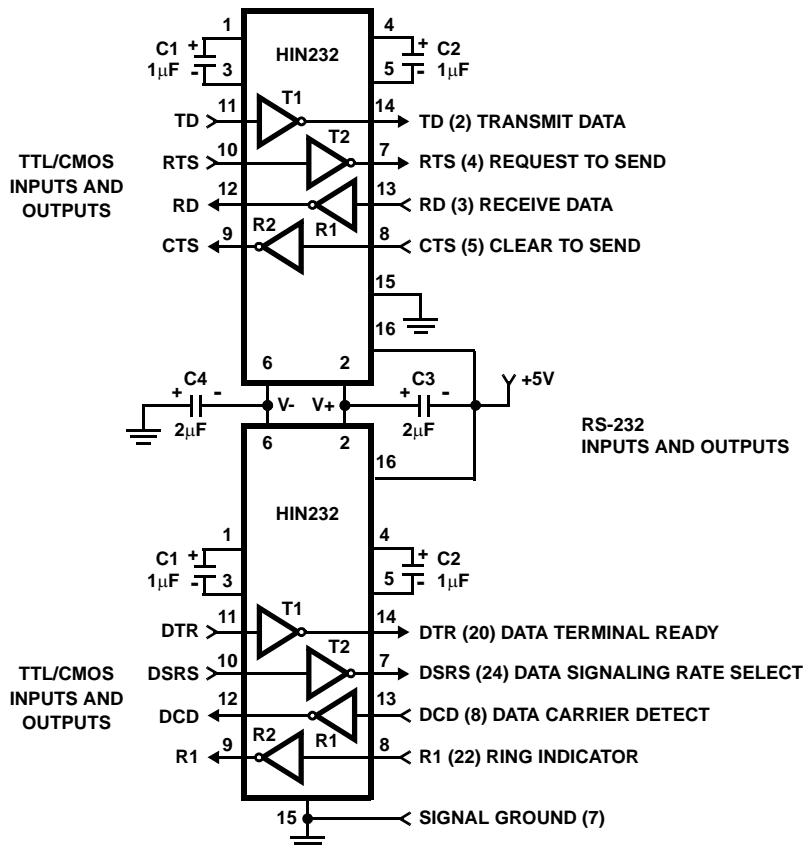


FIGURE 10. COMBINING TWO HIN232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

Die Characteristics

DIE DIMENSIONS

160 mils x 140 mils

METALLIZATION

Type: Al
Thickness: 10kÅ ±1kÅ

SUBSTRATE POTENTIAL

V+

PASSIVATION

Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

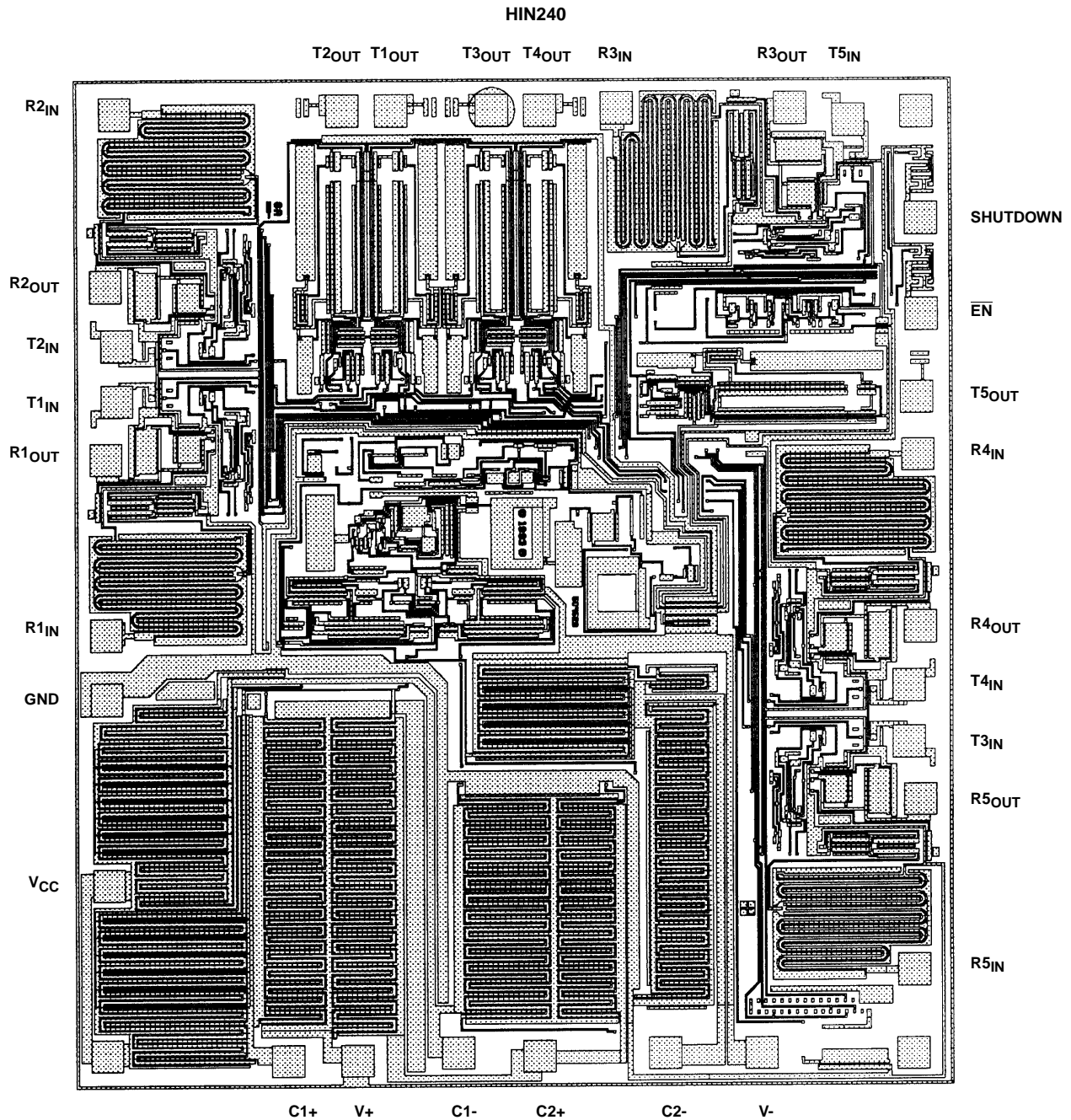
TRANSISTOR COUNT

238

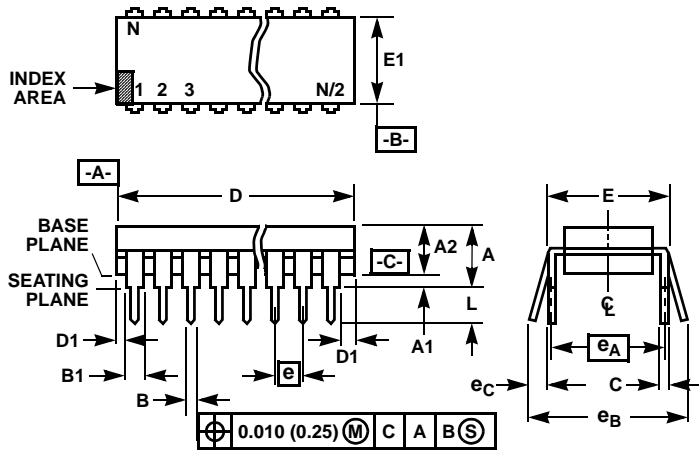
PROCESS

CMOS Metal Gate

Metallization Mask Layout



Dual-In-Line Plastic Packages (PDIP)



NOTES:

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e_A are measured with the leads constrained to be perpendicular to datum $-C-$.
- e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

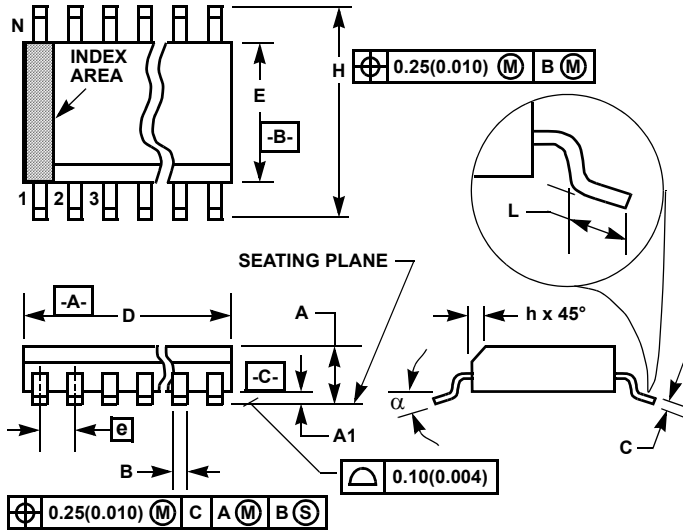
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

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Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

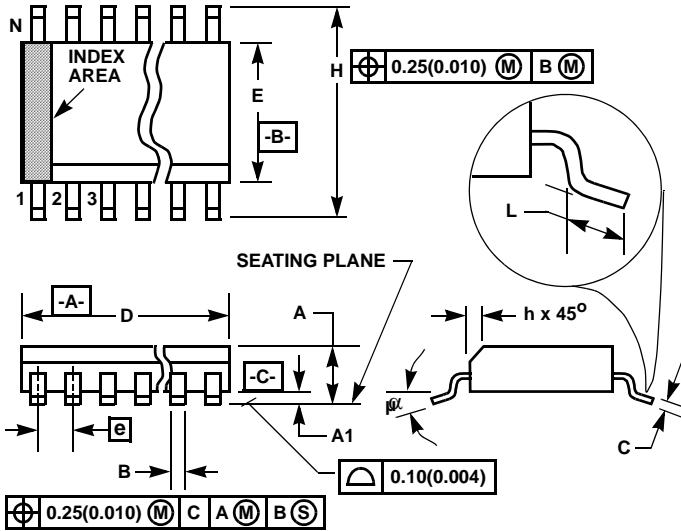
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
alpha	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

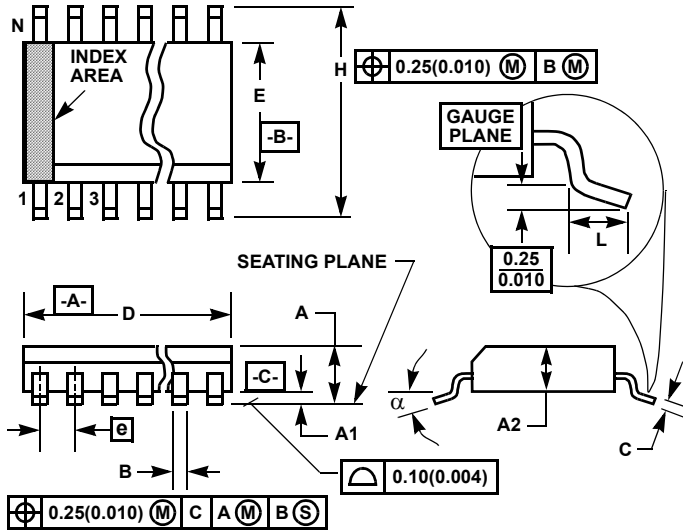
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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Shrink Small Outline Plastic Packages (SSOP)



M28.209 (JEDEC MO-150-AH ISSUE B)
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

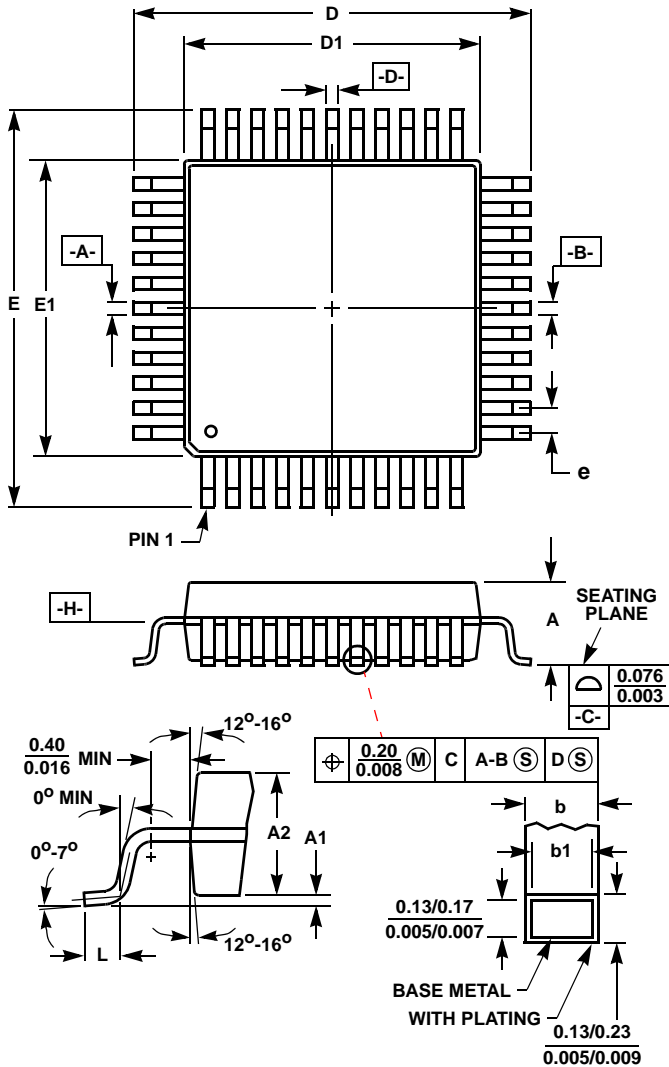
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 2 6/05

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Metric Plastic Quad Flatpack Packages (MQFP)



**Q44.10x10 (JEDEC MS-022AB ISSUE B)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

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NOTES:

- Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
- All dimensions and tolerances per ANSI Y14.5M-1982.
- Dimensions D and E to be determined at seating plane **-C-**.
- Dimensions D1 and E1 to be determined at datum plane **-H-**.
- Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
- Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
- "N" is the number of terminal positions.

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