Data Sheet
March 1992

AT&T Microelectronics

ATT20C476A CMOS RAMDAC

Features

- 110/100/80/66/50 MHz operation
- Low power dissipation = 0.5 W typical
- On-chip output comparators for monitor detection
- Internal V_{REF} accuracy better than ±3%
- External V_{REF} option
- Antisparkle circuitry
- 6-bit DACs
- 256 x 18 palette
- Epitaxial layer over substrate for reduced noise feedthrough
- Latch-up immunity >250 mA
- Industry-compatible footprint
- Monolithic 0.9 µm CMOS

Applications

- Desktop PC VGA and *PS/2** graphics
- Screen resolutions (noninterlaced)
  — 1280 x 1024, 60 Hz
  — 1024 x 1024, 76 Hz

* *PS/2* is a registered trademark of International Business Machines Corporation.

Description

The ATT20C476A RAMDAC is designed to increase speed and reduce power in the digital-to-analog conversion of frame buffer images.

On-chip output comparators detect connection to a monitor. An internal voltage reference with better than ±3% accuracy helps to ensure your product meets PC graphics requirements, and eliminates the need for external references. The part contains antisparkle circuitry.

The ATT20C476A has a 256 x 18 look-up table (LUT) displaying 256 colors out of 262K possible.

The ATT20C476A is designed in AT&T's 0.9 µm CMOS process, adding performance and speed (110 MHz) to industry-standard capabilities. CMOS design and unique RAM cell structure contribute to one of the lowest power dissipations in the industry.

The part is offered in the industry-standard 44-pin PLCC package and compatible footprint. This part is meant to work with an external voltage reference only (internal or external).

Table of Contents

Contents Page

Description (continued)

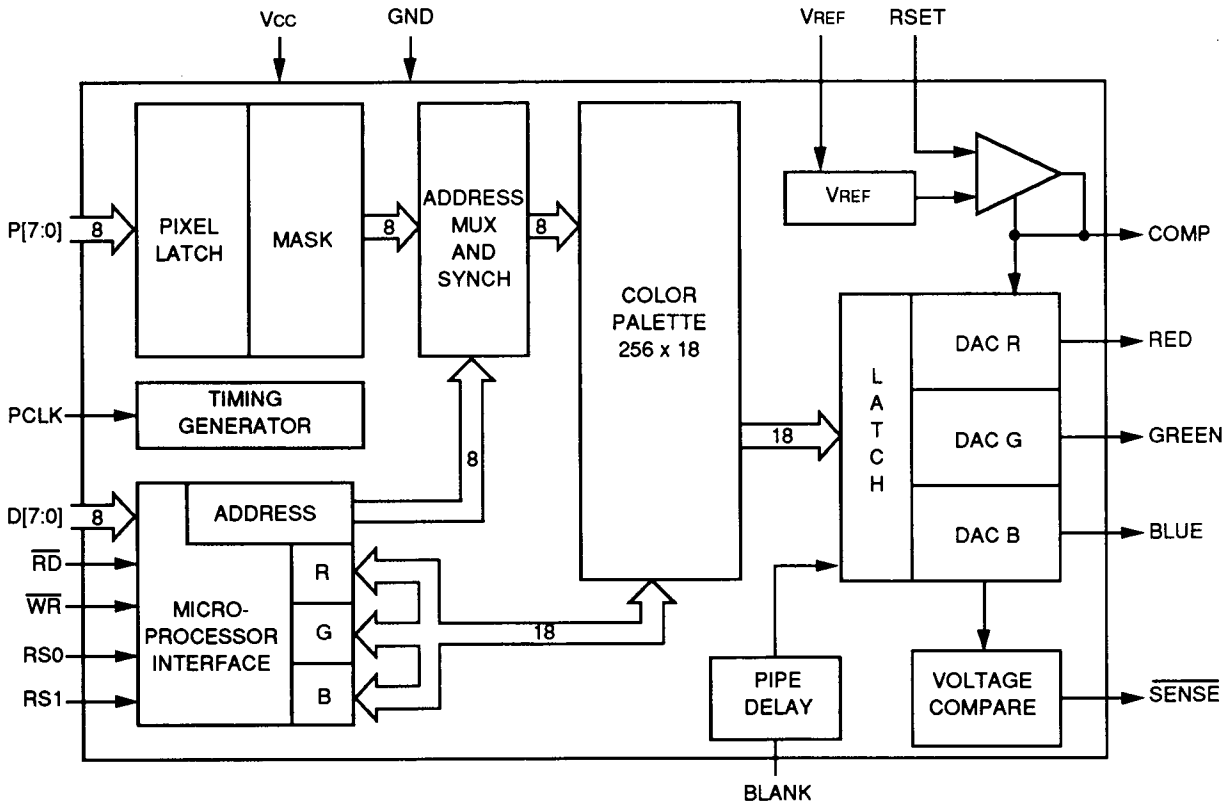


Figure 1. Block Diagram

Pin Information

Top View.

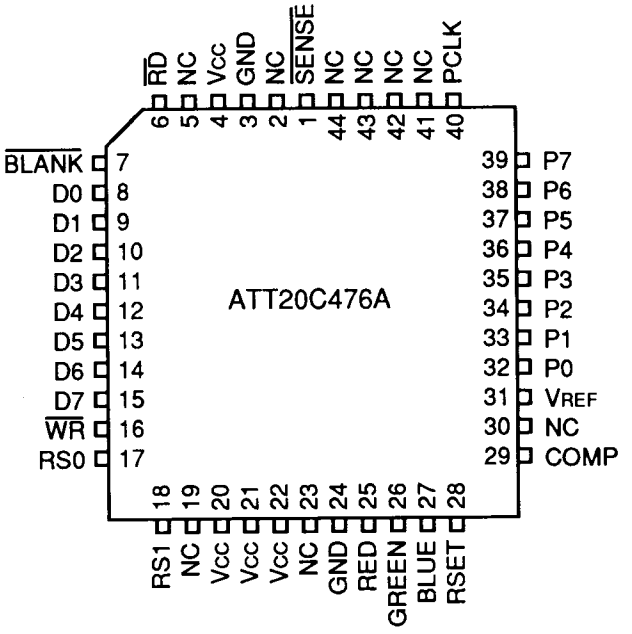


Figure 2. ATT20C476A Pin Diagram

Table 1. Pin Descriptions

ATT20C476A Pin #	Symbol	Type	Name/Function
1	$\overline{\text{SENSE}}$	O	**$\overline{\text{SENSE}}$ (Active-Low).** TTL compatible. Monitor detection signal. $\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level of 340 mV.
2, 5, 19, 23, 30, 41—44	N/C	—	**No Connect.** No internal connection to the chip.
3, 24	GND	—	**Ground.**
4, 20—22	Vcc	—	**Vcc.**
6	$\overline{\text{RD}}$	I	**Read (Active-Low).** TTL compatible. When $\overline{\text{RD}}$ is low, the data transfer from the selected internal register to the data bus takes place. The rising edge of the $\overline{\text{RD}}$ signal indicates the end of a read cycle.
7	$\overline{\text{BLANK}}$	I	**$\overline{\text{BLANK}}$ (Active-Low).** TTL compatible. $\overline{\text{BLANK}}$ is latched on the rising edge of PCLK. When $\overline{\text{BLANK}}$ is low, a 1.44 mA current source on the analog outputs will be turned off. The DACs ignore digital input from memory. The RAMDAC and overlay memory can be updated during blanking.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

ATT20C476A Pin #	Symbol	Type	Name/Function
8—15	D[7:0]	I/O	**Data Bus.** TTL compatible. Data is transferred between the data bus and the internal registers under control of the RD / WR signal. In an MPU write operation, D[7:0] is latched on the rising edge of WR . To read data D[7:0] from the device, RD must be in an active-low state. The rising edge of the RD signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. For 6-bit operation, color data is contained in the lower six bits of the data bus. D0 is the LSB and D5 is the MSB. When the MPU writes color data, D6 and D7 are ignored. During MPU read cycles, D6 and D7 are a logic 0.
16	$\overline{WR}$	I	**Write (Active-Low).** TTL compatible. $\overline{WR}$ controls the data transfer from the data bus to the selected internal register. D[7:0] data is latched at the rising edge of WR , and RS[1:0] are latched at the falling edge of WR .
17—18	RS[1:0]	I	**Register Select.** TTL compatible. These inputs are sampled on the falling edge of the RD or WR to determine which one of the internal registers is to be accessed.
25 26 27	RED GREEN BLUE	O	**Color Signals**. These pins are analog outputs. These high-impedance current sources are capable of driving a double-terminated 75 Ω coaxial cable.
28	RSET	I	**Reference Resistor.** An external resistor is connected between the RSET pin and GND to control the magnitude of the full-scale current. Refer to DAC Gain section under Functional Description.
29	COMP	I	**Compensation Pin.** Bypass this pin with a 0.1 µF capacitor.
31	V_{REF}	I	**Voltage Reference.** If an external voltage reference is used, supply this input with 1.235 V.
32—39	P[7:0]	I	**Pixel Address.** TTL compatible. This pin is latched on the rising edge of PCLK. These inputs are masked by the pixel mask register and then used to specify one of the 256 addresses of the color RAM. Unused inputs should be connected to GND.
40	PCLK	I	**Pixel Clock.** TTL compatible. The duty cycle of the clock should be between 30% and 70%. The rising edge of the pixel clock latches the pixel address and BLANK inputs. The pixel clock controls the four-stage video pipelined operation.

Functional Description

MPU Interface

The ATT20C476A supports a standard MPU interface, allowing the MPU direct access to the RAMDAC RAM (see Figure 1).

As outlined in Table 2, the RS[1:0] select inputs indicate whether the MPU is accessing the address register, RAMDAC RAM, or read mask register. To eliminate the requirement for external address multiplexers, the 8-bit address register is used to address the RAMDAC RAM. ADDR0 corresponds to D0 and is the least significant bit.

Table 2. Control Input Truth Table

RS1	RS0	Addressed by MPU
0	0	Address register (RAM write mode)
1	1	Address register (RAM read mode)
0	1	RAMDAC RAM
1	0	Pixel read mask register

Writing the RAMDAC

The MPU writes the address register (RAM write mode) with the address of the RAMDAC RAM location to be modified. Using RS[1:0] to select the RAMDAC RAM, the MPU completes three continuous write cycles (6 bits each of red, green, and blue). Following the blue write cycle, the color information is concatenated into an 18-bit word and written to the location specified by the address register. The address register advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous R, G, and B write cycles until the entire block has been written.

Reading the RAMDAC

The MPU loads the address register (RAM read mode) with the address of the RAMDAC RAM location to be read. The contents of the RAMDAC RAM at the specified address are copied into the RGB registers, and the address register advances to the next RAM location.

Using RS[1:0] to select the RAMDAC RAM, the MPU completes three continuous read cycles (6 bits each of red, green, and blue). After the blue read cycle, the contents of the RAMDAC RAM at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous R, G, and B read cycles until the entire block has been read.

Additional Information

Following a blue read or write cycle to RAM location $FF, the address register resets to $00.

Operation of the MPU interface occurs asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC RAM/overlay registers and the R, G, B color subregister. The transfers occur between MPU accesses. As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See the ac timing characteristics under $\overline{RD}$ / $\overline{WR}$ high time for further information. To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between look-up table RAMs and the R, G, B registers occurs.

To monitor the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 4. They are reset to 0 when the MPU writes to the address register, and are not reset to 0 when the MPU reads the address register. The MPU does not have access to these bits.

The other 8 bits of the address register (ADDR[7:0]), incremented following a blue read or write cycle, are accessible to the MPU and are used to address RAMDAC RAM locations as outlined in Table 3.

The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM.

Table 3. Address Register (ADDR) Operation

RS1	RS0	ADDR[7:0]	Addressed by MPU
0	1	$00—$FF	RAMDAC RAM

Functional Description (continued)

Table 4. Modulo Counter Operation

Value	Addressed by MPU
00	Red value
01	Green value
10	Blue value

Pixel Pins

The contents of the pixel read mask register, which can be accessed by the MPU at any time, are bit-wise logically ANDed with the P[7:0] inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 18 bits of color information to the three D/A converters.

To maintain synchronization with color data, the rising edge of the clock latches the BLANK input. BLANK adds appropriately weighted currents to the analog outputs to produce the BLANK pedestal currents as shown in Figures 3 and 4 and Tables 6 and 7.

The analog outputs of the ATT20C476A are capable of directly driving 37.5 Ω loads (R, G, B), such as a doubly terminated 75 Ω coaxial cable.

$\overline{\text{SENSE}}$ Output

$\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, and blue outputs have exceeded the internal voltage reference level (340 mV). This output is used to determine the presence of a CRT monitor, and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 340 mV reference has a ±40 mV tolerance.

DAC Gain

The device gain from the voltage reference to the DAC output current is shown below. To set the full-scale white current on the DACs while using an internal or external voltage reference, use the formula below. V_{REF} is the voltage reference in volts, and K is the gain constant shown in Table 6. RSET is the resistor connected between the RSET pin and ground.

I_{OUT} (mA) = [V_{REF} (V) * 1,000 * K] / RSET (Ω)

In this case, a voltage reference of 1.235 V with RSET = 147 Ω and a K factor of 2.27, results in I_{OUT} = 19.07 mA. A DAC without any blanking pedestal results in a K factor of 2.1 and I_{OUT} = 17.64 mA.

As shown in Table 5, the recommended RSET for RS-343A compatibility (doubly terminated 75 Ω) applications is 147 Ω. The recommended RSET for *PS/2* applications (50 Ω) is 182 Ω.

Table 5. I_{OUT} Current

Output Waveform Level	RS-343A	*PS/2*	K Factor
Black to White	17.6 mA	14.25 mA	2.1
Black to BLANK	1.4 mA	—	0.1667
Recommended RSET	147 Ω	182 Ω	—

Functional Description (continued)

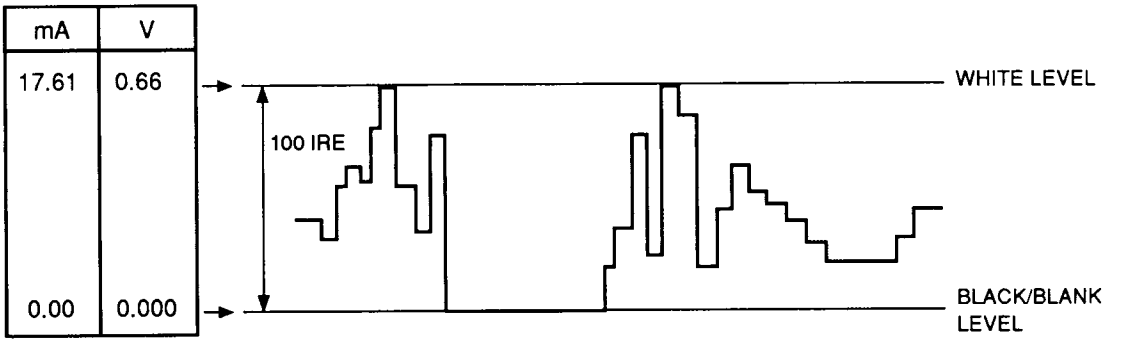


Figure 3. Composite Video Output Waveforms

Table 6. Video Output Truth Table

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	IOUT (mA)
$FF	1	WHITE	17.61
data	1	DATA	data
$00	1	BLACK	0
$XX	0	$\overline{\text{BLANK}}$	0

Note: 75 Ω doubly terminated load. V_{REF} = 1.235 V or I_{REF} = 8.39 mA, RSET = 147 Ω.

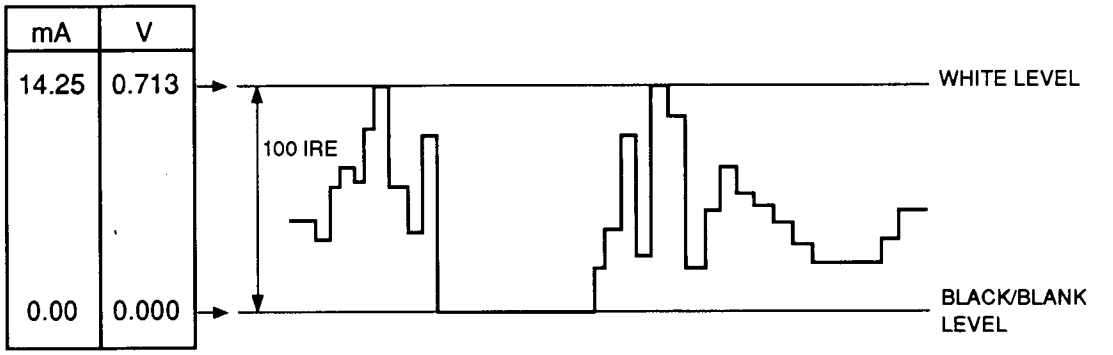


Figure 4. *PS/2* Composite Video Output Waveforms

Table 7. *PS/2* Video Output Truth Table

DAC Input Data	$\overline{\text{BLANK}}$	Output Level	IOUT (mA)
$FF	1	WHITE	14.25
data	1	DATA	data
$00	1	BLACK	0
$XX	0	$\overline{\text{BLANK}}$	0

Note: 50 Ω load. V_{REF} = 1.235 V or I_{REF} = –6.79 mA, RSET = 182 Ω.

Application Information

Board Layout

Careful configuration and placement of supply planes, components, and signal traces ensure a low-noise board. This helps ensure proper functionality and low signal emissions in restricted frequency bands as mandated by regulatory agencies.

A 4-layer PC board with separate power and ground planes will likely result in a board with quieter signals and supplies as well as less spectral content in emitted frequency bands. The board should have signal layers 1 and 4 (outside layers) and supply layers 2 and 3 (inside layers). Use a solid ground plane for frequencies up to 100 MHz.

The ATT20C476A should be placed close to the video output connector and between the video output connector and the edge card connector. This will keep the high-speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

Power Distribution

Separate the power plane into digital and analog areas. Place all digital components over the digital plane and all analog components over the analog plane. The analog components will include the RAMDAC, reference circuitry, comparators, all mixed signal chips (such as a clock synthesizer), and any passive support components for analog circuits.

The analog and digital power plane should be connected with at least one ferrite bead across the separation as illustrated in Figures 5 and 6 This bead provides resistance to high-frequency currents. Select a ferrite bead with an impedance curve suitable for your design. The ferrite should have a resistance at a higher frequency than the maximum signal frequency on the board, but lower than the second harmonic (2x) of that frequency. The following beads provide resistances of approximately 75 Ω at 100 MHz: Ferroxcube VK20019-4B, Fair-Rite 2743001111, or Philips 431202036690.

Decoupling Capacitors

All decoupling capacitors should be located within 0.25 in. of the device to be decoupled. Chip capacitors are recommended, but radial and axial leads will work. Keep lead lengths as short as possible to reduce inductance and EMI. For leaded capacitors, use devices with a self-resonance above the pixel clock frequency.

For the ATT20C476A RAMDAC, decouple the two groups of Vcc pins to ground with 0.1 µF capacitors. For higher frequency pixel clocks (>80 MHz), use a 0.001 µF capacitor in parallel with the 0.1 µF capacitor to shunt the higher frequency noise to ground. Power supply noise should be <200 mV for a good design. Supply noise >400 mV should be avoided. About 10% of any noise below 1 MHz will be coupled onto the DAC outputs. As illustrated in Figures 5 and 6, the COMP pin should also be decoupled with a 0.1 µF capacitor. For designs showing ghosting or smearing, add a parallel COMP capacitance of 2.2 µF.

Digital Signals

The digital inputs should not travel over the analog power plane if possible. The RAMDAC should be located over the analog plane close to the digital/analog supply separation. The RAMDAC may also be placed over the supply separation, so the digital pixel inputs are over the digital supply plane. The digital inputs, especially the P[7:0] high-speed inputs, should be isolated from the analog outputs. Placing the digital inputs over the digital supply reduces coupling into the analog supply plane. High-speed signals (both analog and digital) should not be routed under the RAMDAC.

Avoid high slew rate edges, as they can contribute to undershoot, overshoot, ringing, EMI, and noise feedthrough. Wherever possible, use slower edge rate (3 ns—5 ns) logic such as 74LS or 74ALS devices. If this is not possible, edges can be slowed down using series termination (75 Ω to 150 Ω). Edge noise will result if the digital signal propagates from an impedance mismatch while the signal rises. The reflection noise is particularly troublesome in the TTL threshold region. For a 2 ns edge, the trace length must be less than 4 in.

Application Information (continued)

Digital Signals (continued)

The clock signal trace should be as short as possible and should not run parallel to any high-speed signals. To ensure a quality clock signal without high-frequency noise components, decouple the supply pins on the clock driver. If necessary, transmission line techniques should be used on the clock by providing controlled impedance striplines and parallel termination.

Analog Signals

The load resistor should be as close as possible to the DAC outputs. The resistor should equal the destination termination, which is usually a 75 Ω monitor. Unused analog outputs should be connected to ground. The DAC output traces should be as short as possible to minimize any impedance mismatch in the trace or video connector. Series ferrite beads can be added to the analog video signal to reduce high-frequency signals coupled onto the DAC outputs or reflected from the monitor.

To reduce the interaction of the analog video return current with board components, a separate video ground return trace can be added to the ground plane or signal layer. This trace connects directly to the ground of the edge card connector.

DAC Outputs

The ATT20C476A analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching ac coupled monitors.

The diode protection circuit shown in Figures 5 and 6 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA205X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

Application Information (continued)

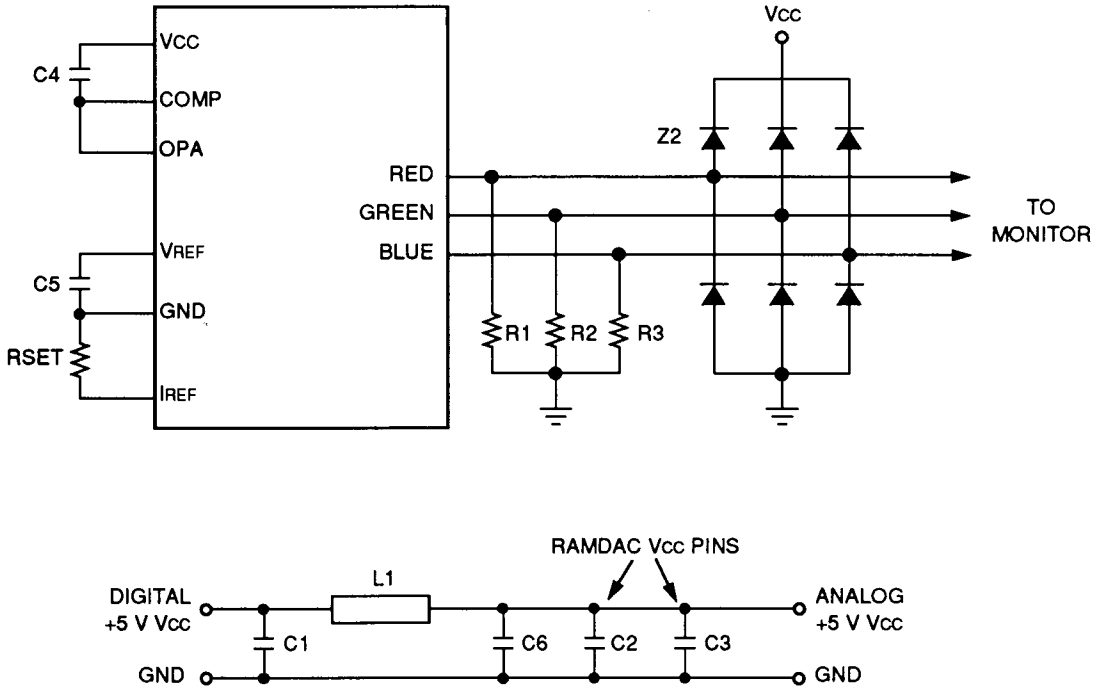


Figure 5. Typical Connection Diagram for Internal Voltage Reference

Table 8. Internal Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1—R3	75 Ω, 1% metal film resistor	Dale CMF-55C
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
D1—D6	Fast-switching diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C476A.

Application Information (continued)

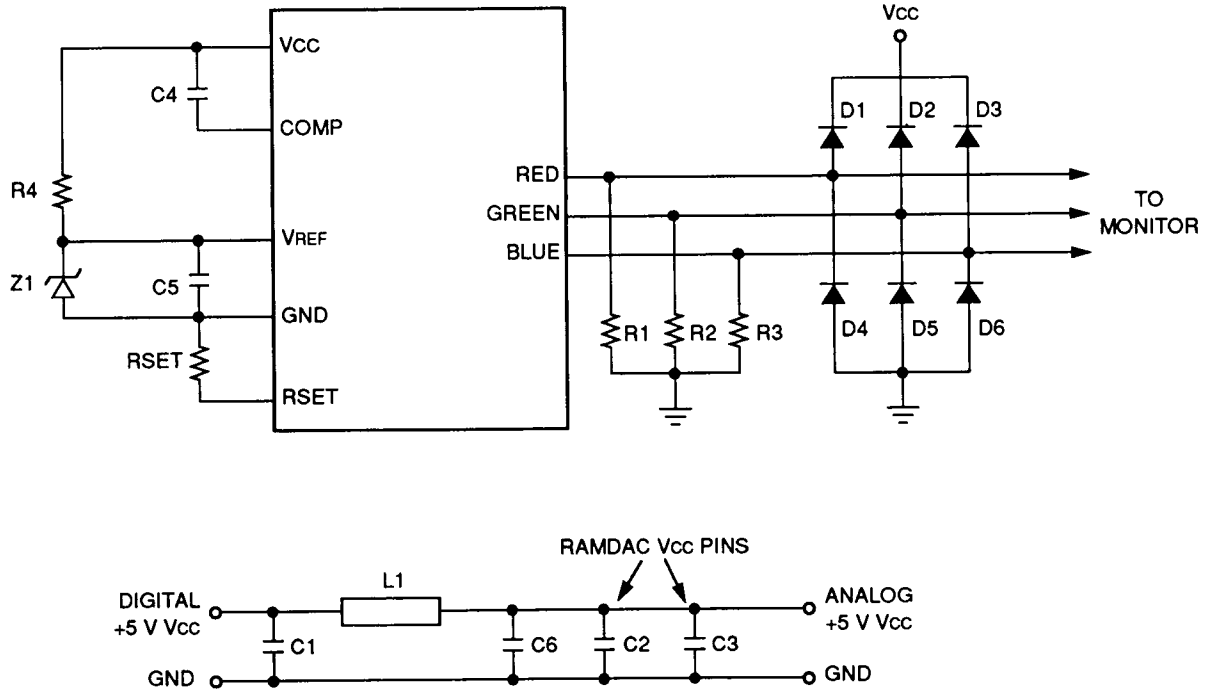


Figure 6. Typical Connection Diagram for External Voltage Reference

Table 9. External Voltage Reference Parts List

Location	Description	Vendor Part Number
C1—C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω, 1% metal film resistor	Dale CMF-55C
R4	1 kΩ, 5% resistor	—
RSET	147 Ω, 1% metal film resistor	Dale CMF-55C
Z1	1.2 voltage reference	National Semiconductor LM385BZ-1.2
D1—D6	Fast-switching diode	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the ATT20C476A.

Application Information (continued)

Multiple RAMDACs

Each device should have its own power plane and ferrite bead, when using multiple ATT20C476A devices. Use the internal voltage references rather than a single external reference to achieve less color channel crosstalk and RAMDAC interaction.

Each ATT20C476A device must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
Vcc (measured to GND)	—	—	—	7.0	V
Voltage on any Digital Pin	—	GND – 0.5	—	Vcc + 0.5	V
Analog Output Short Circuit: Duration to any Power Supply or Common	ISC	—	indefinite	—	—
Ambient Operating Temperature	T_A	–55	—	125	°C
Storage Temperature	Tstg	–65	—	150	°C
Junction Temperature	T_J	—	—	150	°C
Vapor Phase Soldering (60 s)	TVSOL	—	—	220	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply:					
66/80	Vcc	4.5	5.0	5.5	V
100/110	Vcc	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	0	—	70	°C
Output Load	R_L	—	37.5	—	Ω
Voltage Reference Configuration: Reference Voltage	VREF	1.2	1.235	1.27	V

Electrical Characteristics

Table 10. dc Characteristics

The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235.
The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC):					
ATT20C476A	—	6	6	6	Bits
Accuracy (each DAC):					
Integral Linearity Error:	IL	—	—	±1/4	LSB
Differential Linearity Error:	DL	—	—	±1/4	LSB
Gain Error	—	—	—	±5	%
Monotonicity	—	—	guaranteed	—	Scale
Coding	—	—	—	—	Binary
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND – 0.5	—	0.8	V
High	V_{IH}	2.0	—	V_{CC} + 0.5	V
Input Current:					
Low (V_{IN} = 0.4 V)	I_{IL}	—	—	–1	µA
High (V_{IN} = 2.4 V)	I_{IH}	—	—	1	µA
Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}	—	—	7	pF
Digital Outputs:					
Output Voltage:					
Low (I_{OL} = 3.2 mA)	V_{OL}	—	—	0.4	V
High (I_{OH} = –400 µA)	V_{OH}	2.4	—	—	V
3-State Current	I_{OZ}	—	—	50	µA
Capacitance	CD_{OUT}	—	—	7	pF
Analog Outputs:					
Gray Scale Current Range	—	—	—	20	mA
Output Current:					
White Level Relative to Black	—	16.74	17.62	18.50	mA
Black Level Relative to Blank	—	0	0	0	µA
Blank Level	—	0	5	50	µA
LSB Size	—	—	279.68	—	µA
DAC to DAC Matching	—	—	2	5	%
Output Compliance	V_{OC}	–1.0	—	1.5	V
Output Impedance	RA_{OUT}	—	10	—	kΩ
Output Capacitance (f = 1 MHz, I_{OUT} = 0 mA)	CA_{OUT}	—	—	30	pF
Internal Reference Output (±3%)	V_{REF}	1.2	1.235	1.27	V
Power Supply Rejection Ratio	PSRR	—	—	0.5	%/% ΔVcc
(COMP = 0.1 F, f = 1 kHz)	—	—	—	–6	dB

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): Recommended operating conditions using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

Table 11. ac Characteristics

		110 MHz Devices			100 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	110	—	—	100	MHz
RS[1:0] Setup Time	1	10	—	—	10	—	—	ns
RS[1:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	30	—	—	30	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	4	—	—	4	—	—	PCLK
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	2	—	—	2	—	—	ns
Pixel and Control Hold Time	13	2	—	—	2	—	—	ns
Clock Cycle Time	14	9.1	—	—	10	—	—	ns
Clock Pulse Width High Time	15	3	—	—	3	—	—	ns
Clock Pulse Width Low Time	16	3	—	—	3	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	3	—	—	3	—	ns
Analog Output Settling Time*	—	—	10	—	—	10	—	ns
Clock and Data Feedthrough*	—	—	-30	—	—	-30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	-23	—	—	-23	—	dB
Analog Output Skew	18	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	4	4	4	4	4	Clocks
Vcc Supply Current†: Normal Operation	Icc	—	115	175	—	110	175	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, Icc (typ) at Vcc = 5.0 V Icc (max) at Vcc (max).

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): Recommended operating conditions using external voltage reference with RSET = 147 Ω, V_{REF} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF, $\overline{SENSE}$, D[7:0] output load ≤50 pF. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

Table 11. ac Characteristics (continued)

		80 MHz Devices			66 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	80	—	—	66	MHz
RS[1:0] Setup Time	1	10	—	—	10	—	—	ns
RS[1:0] Hold Time	2	10	—	—	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	5	—		ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	40	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	—	—	20	ns
Read Data Hold Time	6	5	—	—	5	—	—	ns
Write Data Setup Time	7	10	—	—	10	—	—	ns
Write Data Hold Time	8	10	—	—	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	4	—	—	4	—	—	PCLK
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	6	—	—	PCLK
Pixel and Control Setup Time	12	3	—	—	3	—	—	ns
Pixel and Control Hold Time	13	3	—	—	3	—	—	ns
Clock Cycle Time	14	12.5	—	—	15.15	—	—	ns
Clock Pulse Width High Time	15	4	—	—	5	—	—	ns
Clock Pulse Width Low Time	16	4	—	—	5	—	—	ns
Analog Output Delay	17	—	—	30	—	—	30	ns
Analog Output Rise/Fall Time	—	—	3	—	—	3	—	ns
Analog Output Settling Time*	—	—	13	—	—	13	—	ns
Clock and Data Feedthrough*	—	—	–30	—	—	–30	—	dB
Glitch Impulse*	—	—	75	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	—	–23	—	dB
Analog Output Skew	18	—	—	2	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	—	1	—	µs
Pipeline Delay	—	4	4	4	4	4	4	Clocks
V_{CC} Supply Current†: Normal Operation	I_{CC}	—	105	160	—	100	160	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, I_{CC} (typ) at V_{CC} = 5.0 V I_{CC} (max) at V_{CC} (max).

Electrical Characteristics (continued)

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operating condition for generating test signals is RSET = 147 Ω, V_{REF} = 1.235 V, SETUP = 7.5 IRE, 8/$\overline{6}$ pin = logic 1. The parameters are applicable over the full voltage and temperature range as shown in the Recommended Operating Conditions table.

Table 11. ac Characteristics (continued)

		50 MHz Devices			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Clock Rate	fmax	—	—	50	MHz
RS[1:0] Setup Time	1	10	—	—	ns
RS[1:0] Hold Time	2	10	—	—	ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5	—	—	ns
$\overline{RD}$ Asserted to Data Valid	4	—	—	40	ns
$\overline{RD}$ Negated to Data Bus 3-Stated	5	—	—	20	ns
Read Data Hold Time	6	5	—	—	ns
Write Data Setup Time	7	10	—	—	ns
Write Data Hold Time	8	10	—	—	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	4	—	—	PCLK
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10, 11	6	—	—	PCLK
Pixel and Control Setup Time	12	3	—	—	ns
Pixel and Control Hold Time	13	3	—	—	ns
Clock Cycle Time	14	20	—	—	ns
Clock Pulse Width High Time	15	6	—	—	ns
Clock Pulse Width Low Time	16	6	—	—	ns
Analog Output Delay	17	—	—	30	ns
Analog Output Rise/Fall Time	—	—	3	—	ns
Analog Output Settling Time*	—	—	20	—	ns
Clock and Data Feedthrough*	—	—	–30	—	dB
Glitch Impulse*	—	—	75	—	pV-s
DAC to DAC Crosstalk	—	—	–23	—	dB
Analog Output Skew	18	—	—	2	ns
$\overline{SENSE}$ Output Delay	—	—	1	—	µs
Pipeline Delay	—	4	4	4	Clocks
V_{CC} Supply Current†: Normal Operation	I_{CC}	—	100	160	mA

* Clock and data feedthrough are functions of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. –3 dB test bandwidth = 2 x clock rate.

† At fmax, I_{CC} (typ) at V_{CC} = 5.0 V I_{CC} (max) at V_{CC} (max).

Timing Characteristics

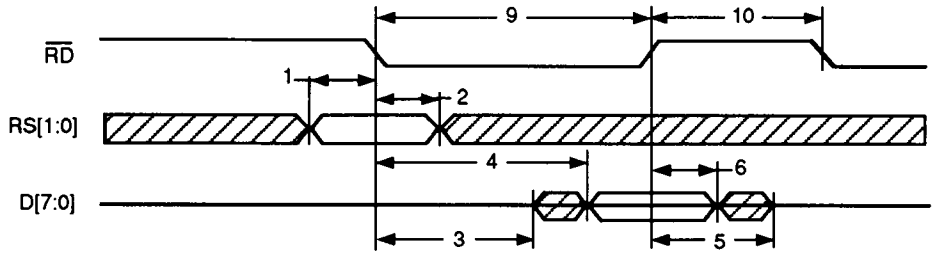


Figure 7. Basic Read-Cycle Timing Diagram

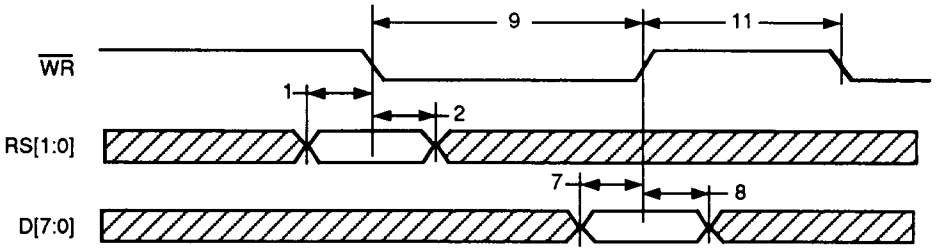


Figure 8. Basic Write-Cycle Timing Diagram

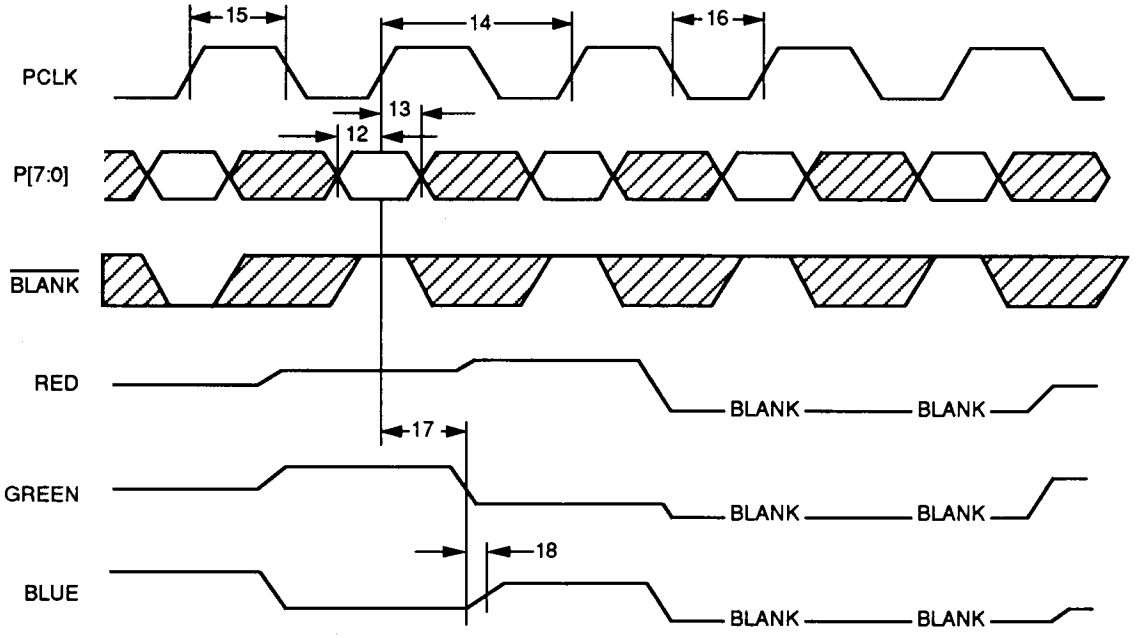


Figure 9. Pixel and Video Control Timing

Timing Characteristics (continued)

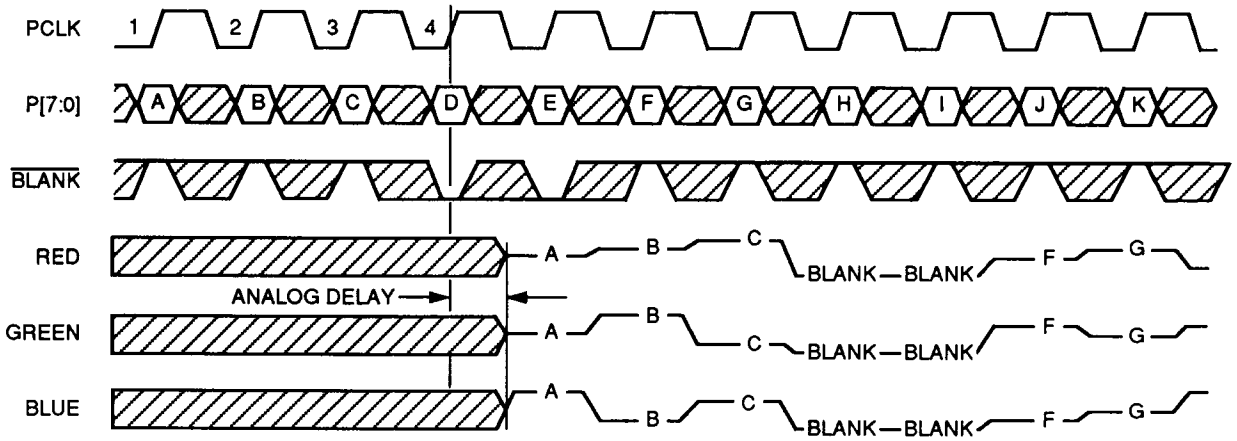


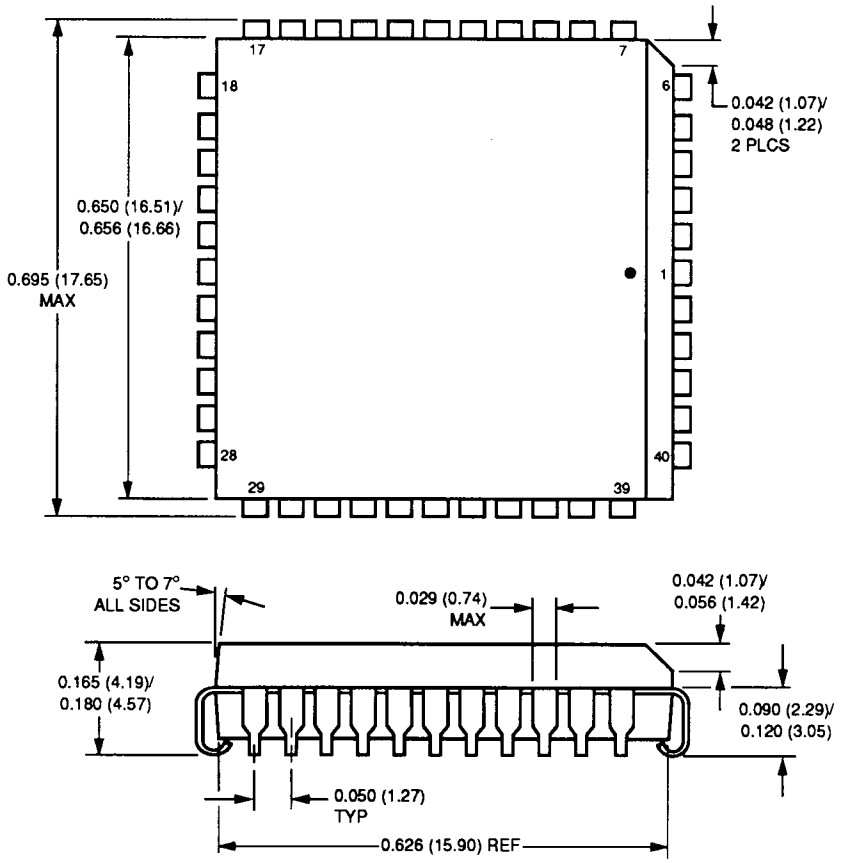
Figure 10. System Timing Diagram: Pixel Pipeline

Outline Diagram

44-Pin PLCC Package

Top View.

Dimensions are in inches and (millimeters).



Ordering Information

Device	Speed	Package Type
ATT20C476A-XXM44*	110/100/80/66/50 MHz	44-Pin PLCC

*XX refers to speed grade:
11 = 110 MHz
10 = 100 MHz
80 = 80 MHz
66 = 66 MHz
50 = 50 MHz

Revision History

Table 12. Updates to ATT20C476A Data Sheet

The following table outlines and identifies the updates to the *ATT20C476A CMOS RAMDAC* Data Sheet.

Date	Description	Pages Revised
August 1991	First release.	—
March 1992	— Added 50 MHz speed grade. — Table references revised on pages 6, 7, and 10 for Tables 2, 3, 4, 5, 6, and 7. — Minor text revisions; not affecting operation or specifications. — Added revision history.	1, 6, 7, 10, and 19

For additional information, contact your AT&T Account Manager or the following:
U.S.A.: AT&T Microelectronics, Dept. AL-520404200, 555 Union Boulevard, Allentown, PA 18103
1-800-372-2447, FAX 215-778-4106 (In CANADA: **1-800-553-2448,** FAX 215-778-4106)
EUROPE: AT&T Microelectronics, AT&T Deutschland GmbH, Bahnhofstr. 27A, D-8043 Unterfoehring, Germany
Tel. (49) 89 95086-0, FAX (49) 89 95086-331
ASIA PACIFIC: AT&T Microelectronics Asia/Pacific, 14 Science Park Drive, #03-02A/04 The Maxwell, Singapore 0511
Tel. (65) 778-8833, FAX (65) 777-7495, Telex RS 42898 ATTM
JAPAN: AT&T Microelectronics, AT&T Japan Ltd., 31-11, Yoyogi 1-chome, Shibuya-ku, Tokyo 151, Japan
Tel. (03) 5371-2700, FAX (03) 5371-3556
SPAIN: AT&T Microelectronica de España, Poligono Industrial de Tres Cantos (Zona Oeste), 28770 Colmenar Viejo, Madrid, Spain
Tel. (34) 1-8071441, FAX (34) 1-8071420

March 1992
DS92-084ASSP (Replaces DS91-067CMOS)

AT&T Microelectronics