



8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W78L51 microcontroller supplies a wider frequency and supply voltage range than most 8-bit microcontrollers on the market. It is compatible with the industry standard 80C51 microcontroller series.

The W78L51 contains four 8-bit bidirectional parallel ports, one extra 4-bit bit-addressable I/O port (Port 4) and two additional external interrupts ($\overline{\text{INT2}}$, $\overline{\text{INT3}}$), two 16-bit timer/counters, one watchdog timer and a serial port. These peripherals are supported by a seven-source, two-level interrupt capability. There are 128 bytes of RAM and an 4K byte mask ROM for application programs.

The W78L51 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

FEATURES

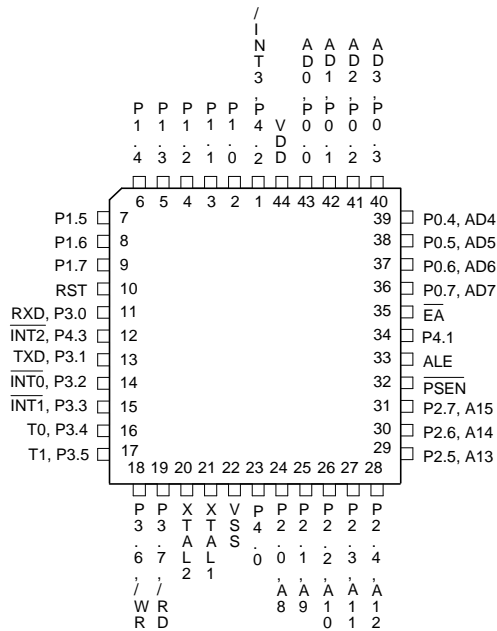
- Fully static design
- Supply voltage of 1.8V to 5.5V
- DC-24 MHz operation
- 128 bytes of on-chip scratchpad RAM
- 4K bytes of on-chip mask ROM
- 64K bytes program memory address space
- 64K bytes data memory address space
- Four 8-bit bidirectional ports
- Two 16-bit timer/counters
- One full duplex serial port
- Seven-source, two-level interrupt capability
- One extra 4-bit bit-addressable I/O port
- Two additional external interrupts $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$
- Watchdog timer
- EMI reduction mode
- Built-in power management
- Code protection
- Packages:
 - DIP 40: W78L51-24
 - PLCC 44: W78L51P-24
 - QFP 44: W78L51F-24

PIN CONFIGURATIONS

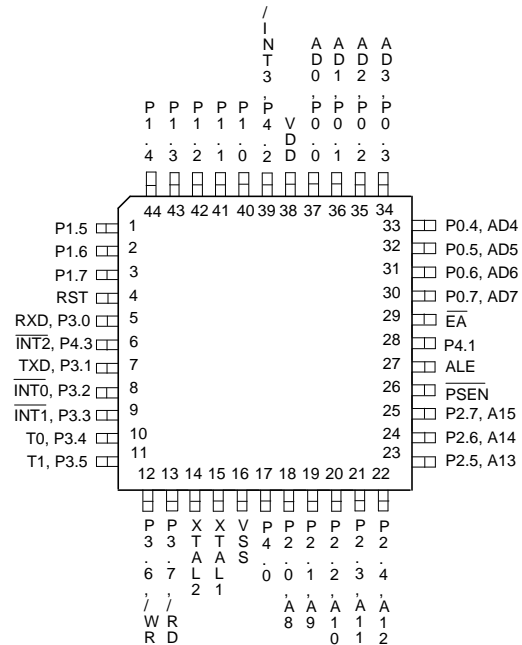
40-Pin DIP (W78L51)

P1.0	1	40	VDD
P1.1	2	39	P0.0, AD0
P1.2	3	38	P0.1, AD1
P1.3	4	37	P0.2, AD2
P1.4	5	36	P0.3, AD3
P1.5	6	35	P0.4, AD4
P1.6	7	34	P0.5, AD5
P1.7	8	33	P0.6, AD6
RST	9	32	P0.7, AD7
RXD, P3.0	10	31	\overline{EA}
TXD, P3.1	11	30	ALE
INT0, P3.2	12	29	PSEN
INT1, P3.3	13	28	P2.7, A15
T0, P3.4	14	27	P2.6, A14
T1, P3.5	15	26	P2.5, A13
WR, P3.6	16	25	P2.4, A12
RD, P3.7	17	24	P2.3, A11
XTAL2	18	23	P2.2, A10
XTAL1	19	22	P2.1, A9
VSS	20	21	P2.0, A8

44-Pin PLCC (W78L51P)



44-Pin QFP (W78L51F)





PIN DESCRIPTION

P0.0- P0.7

Port 0, Bits 0 through 7. Port 0 is a bidirectional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.

P1.0- P1.7

Port 1, Bits 0 through 7. Port 1 is a bidirectional I/O port with internal pull-ups.

P2.0- P2.7

Port 2, Bits 0 through 7. Port 2 is a bidirectional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.

P3.0- P3.7

Port 3, Bits 0 through 7. Port 3 is a bidirectional I/O port with internal pull-ups. All bits have alternate functions, which are described below:

PIN	ALTERNATE FUNCTION
P3.0	RXD Serial Receive Data
P3.1	TXD Serial Transmit Data
P3.2	$\overline{\text{INT0}}$ External Interrupt 0
P3.3	$\overline{\text{INT1}}$ External Interrupt 1
P3.4	T0 Timer 0 Input
P3.5	T1 Timer 1 Input
P3.6	$\overline{\text{WR}}$ Data Write Strobe
P3.7	$\overline{\text{RD}}$ Data Read Strobe

P4.0- P4.3

Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{\text{INT2}}$ / $\overline{\text{INT3}}$).

$\overline{\text{EA}}$

External Address Input, active low. This pin forces the processor to execute out of external ROM. This pin should be kept low for all W78C31 operations.

RST

Reset Input, active high. This pin resets the processor. It must be kept high for at least two machine cycles in order to be recognized by the processor.



ALE

Address Latch Enable Output, active high. ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. A single ALE pulse is skipped during external data memory accesses. ALE goes to a high impedance state during reset with a weak pull-up.

PSEN

Program Store Enable Output, active low. $\overline{\text{PSEN}}$ enables the external ROM onto the Port 0 address/data bus during fetch and MOV_C operations. $\overline{\text{PSEN}}$ goes to a high impedance state during reset with a weak pull-up.

XTAL1

Crystal 1. This is the crystal oscillator input. This pin may be driven by an external clock.

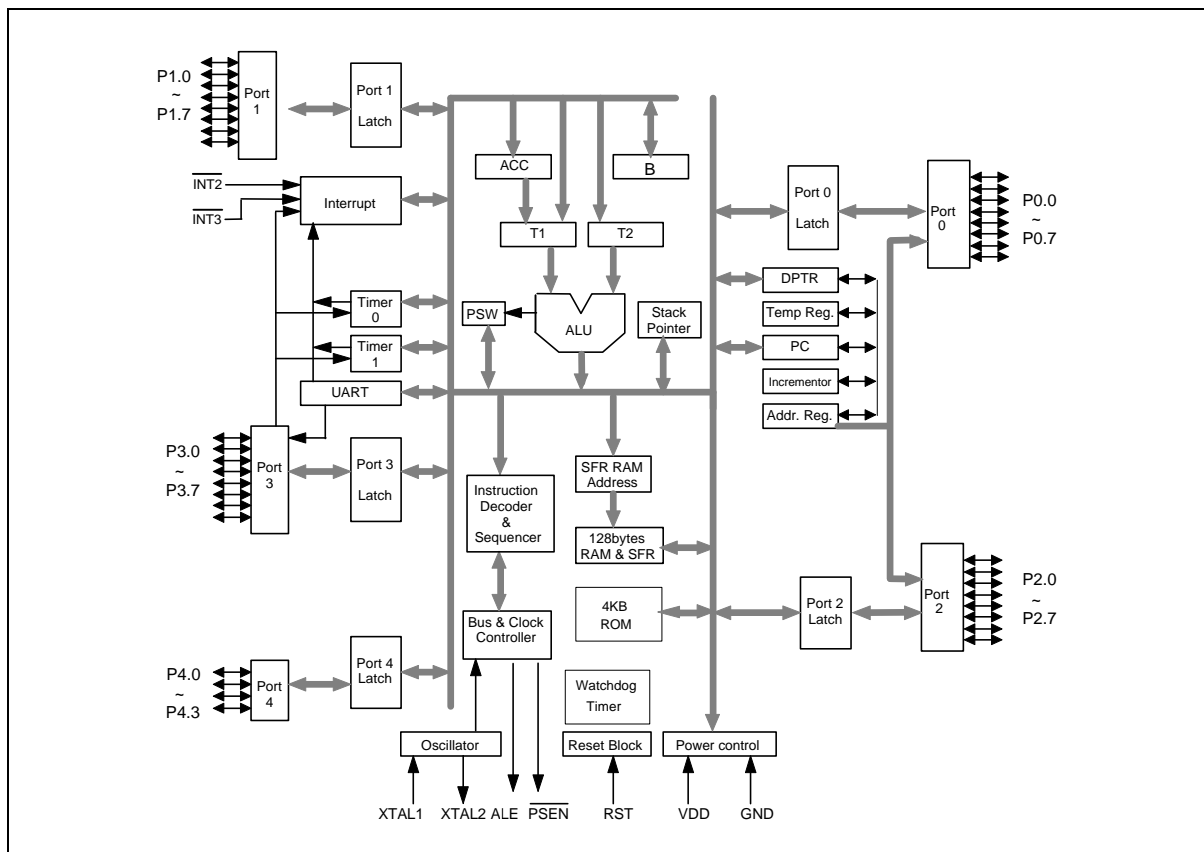
XTAL2

Crystal 2. This is the crystal oscillator output. It is the inversion of XTAL1.

VSS, VDD

Power Supplies. These are the chip ground and positive supplies.

BLOCK DIAGRAM





FUNCTIONAL DESCRIPTION

The W78L51 architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 128 bytes of RAM, two timer/counters, one watchdog timer and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64 K data storage space.

Timers 0, 1

Timers 0, 1 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1. The TCON and TMOD registers provide control functions for timers 0, 1.

Clock

The W78L51 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78L51 relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78L51 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input high level of greater than 3.5 volts when $V_{DD} = 5$ volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks, including the oscillator are stopped. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L51 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.



New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupts $\overline{\text{INT2}}$, $\overline{\text{INT3}}$ have been added to either the PLCC or QFP package. And description follows:

1. $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$

Two additional external interrupts, $\overline{\text{INT2}}$ and $\overline{\text{INT3}}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

***XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2
-----	-----	-----	-----	-----	-----	-----	-----

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Seven-source interrupt informations:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
External Interrupt 2	33H	5	XICON.2	XICON.0
External Interrupt 3	3BH	6 (lowest)	XICON.6	XICON.3



2. PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{\text{INT2}}$ / $\overline{\text{INT3}}$).

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Example: P4      REG  0D8H
          MOV     P4, #0AH    ; Output data "A" through P4.0–P4.3.
          MOV     A, P4       ; Read P4 status to Accumulator.
          SETB    P4.0        ; Set bit P4.0
          CLR     P4.1        ; Clear bit P4.1
```

Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, and a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will be disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0
Mnemonic: WDTC				Address: 8FH				

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2–0 as follows:

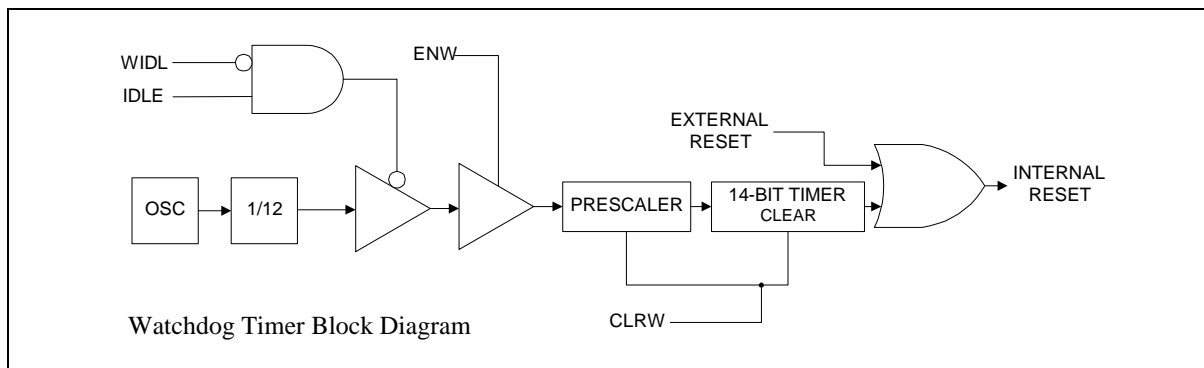
PS2	PS1	PS0	PRESCALER SELECT
0	0	0	2
0	1	0	4
0	0	1	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256



The time-out period is obtained using the following formula:

$$\frac{1}{\text{OSC}} \times 2^{14} \times \text{PRESCALER} \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Typical Watchdog time-out period when OSC = 20 MHz

PS2	PS1	PS0	WATCHDOG TIME-OUT PERIOD
0	0	0	19.66 mS
0	1	0	39.32 mS
0	0	1	78.64 mS
0	1	1	157.28 mS
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

Reduce EMI Emission

Because of the on-chip ROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is not needed. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space.

AUXR - Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	AO

Mnemonic: AUXR

Address: 8Eh

AO: Turn off ALE signal.



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	VCC-VSS	-0.3	+7.0	V
Input Voltage	V _{IN}	V _{SS} -0.3	V _{CC} +0.3	V
Operating Temperature	T _A	0	70	°C
Storage Temperature	T _{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(V_{DD}-V_{SS} = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Operating Voltage	V _{DD}	1.8	5.5	V	
Operating Current	I _{DD}	-	20	mA	No load, V _{DD} = 5.5V, 20 MHz
		-	3	mA	No load, V _{DD} = 2.0V, 16 MHz
Idle Current	I _{IDLE}	-	6	mA	V _{DD} = 5.5V, Fosc = 20 MHz
		-	1.5	mA	V _{DD} = 2.0V, Fosc = 16 MHz
Power Down Current	I _{PWDN}	-	50	μA	V _{DD} = 5.5V, Fosc = 20 MHz
		-	20	μA	V _{DD} = 2.0V, Fosc = 16 MHz
Input Current P1, P2, P3, P4	I _{IN1}	-50	+10	μA	V _{DD} = 5.5V V _{IN} = 0V or V _{DD}
Input Current RST	I _{IN2}	-10	+300	μA	V _{DD} = 5.5V 0 < V _{IN} < V _{DD}
Input Leakage Current P0, $\overline{\text{EA}}$	I _{LK}	-10	+10	μA	V _{DD} = 5.5V 0V < V _{IN} < V _{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I _{TL} [*4]	-500	-	μA	V _{DD} = 5.5V V _{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{\text{EA}}$	V _{IL1}	0	0.8	V	V _{DD} = 4.5V
		0	0.5	V	V _{DD} = 2.0V
Input Low Voltage RST[*1]	V _{IL2}	0	0.8	V	V _{DD} = 4.5V
		0	0.3	V	V _{DD} = 2.0V

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Input Low Voltage XTAL1 [*3]	V _{IL3}	0	0.8	V	V _{DD} = 4.5V
		0	0.6	V	V _{DD} = 2.0V
Input High Voltage P0, P1, P2, P3, P4, \overline{EA}	V _{IH1}	2.0	V _{DD} + 0.2	V	V _{DD} = 5.5V
		1.4	V _{DD} + 0.2	V	V _{DD} = 2.0V
Input High Voltage RST[*1]	V _{IH2}	3.5	V _{DD} + 0.2	V	V _{DD} = 5.5V
		1.7	V _{DD} + 0.2	V	V _{DD} = 2.0V
Input High Voltage XTAL1 [*3]	V _{IH3}	3.5	V _{DD} + 0.2	V	V _{DD} = 5.5V
		1.6	V _{DD} + 0.2	V	V _{DD} = 2.0V
Output Low Voltage P1, P2, P3, P4	V _{OL1}	-	0.45	V	V _{DD} = 4.5V, I _{OL} = +2 mA
		-	0.25	V	V _{DD} = 2.0V, I _{OL} = +1 mA
Output Low Voltage P0, ALE, \overline{PSEN} [*2]	V _{OL2}	-	0.45	V	V _{DD} = 4.5V, I _{OL} = +4 mA
		-	0.25	V	V _{DD} = 2.0V, I _{OL} = +2 mA
Sink Current P1, P2, P3, P4	I _{SK1}	4	9	mA	V _{DD} = 4.5V, V _{in} = 0.45V
		1.8	5.4	mA	V _{DD} = 2.0V, V _{in} = 0.45V
Sink Current P0, ALE, \overline{PSEN}	I _{SK2}	8	16	mA	V _{DD} = 4.5V, V _{in} = 0.45V
		4.5	9	mA	V _{DD} = 2.0V, V _{in} = 0.45V
Output High Voltage P1, P2, P3, P4	V _{OH1}	2.4	-	V	V _{DD} = 4.5V, I _{OH} = -100 μ A
		1.4	-	V	V _{DD} = 2.0V, I _{OH} = -8 μ A
Output High Voltage P0, ALE, \overline{PSEN} [*2]	V _{OH2}	2.4	-	V	V _{DD} = 4.5V, I _{OH} = -400 μ A
		1.4	-	V	V _{DD} = 2.0V, I _{OH} = -200 μ A
Source Current P1, P2, P3, P4	I _{SR1}	-100	-250	μ A	V _{DD} = 4.5V, V _{in} = 2.4V
		-10	-30	μ A	V _{DD} = 2.0V, V _{in} = 1.4V
Source Current P0, ALE, \overline{PSEN}	I _{SR2}	-8	-16	mA	V _{DD} = 4.5V, V _{in} = 2.4V
		-1.0	-2.4	mA	V _{DD} = 2.0V, V _{in} = 1.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and \overline{PSEN} are tested in the external access mode.

*3. XTAL1 is a CMOS input.

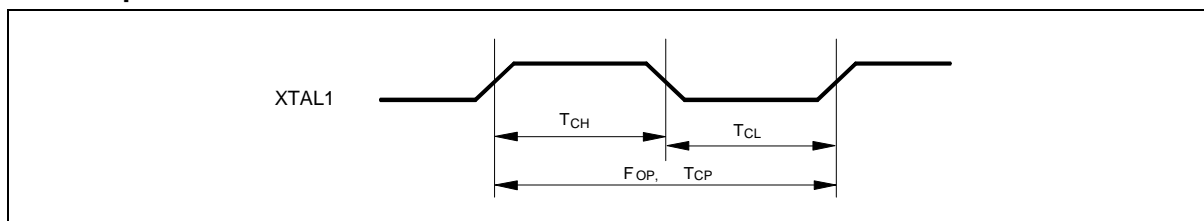
*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.



AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ± 20 nS variation. The numbers below represent the performance expected from a 0.5 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	24	MHz	1
Clock Period	TCP	41.7	-	-	nS	2
Clock High	TCH	20	-	-	nS	3
Clock Low	TCL	20	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP- Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP- Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP- Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP- Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP- Δ	3 TCP	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. " Δ " (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to \overline{RD} Low	TDAR	3 TCP- Δ	-	3 TCP+ Δ	nS	1, 2
\overline{RD} Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from \overline{RD} High	TDDH	0	-	2 TCP	nS	
Data Float from \overline{RD} High	TDDZ	0	-	2 TCP	nS	
\overline{RD} Pulse Width	TDRD	6 TCP- Δ	6 TCP	-	nS	2

Notes:

1. Data memory access time is 8 TCP.
2. " Δ " (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to \overline{WR} Low	TDAW	3 TCP- Δ	-	3 TCP+ Δ	nS
Data Valid to \overline{WR} Low	TDAD	1 TCP- Δ	-	-	nS
Data Hold from \overline{WR} High	TDWD	1 TCP- Δ	-	-	nS
\overline{WR} Pulse Width	TDWR	6 TCP- Δ	6 TCP	-	nS

Note: " Δ " (due to buffer driving delay and wire loading) is 20 nS.

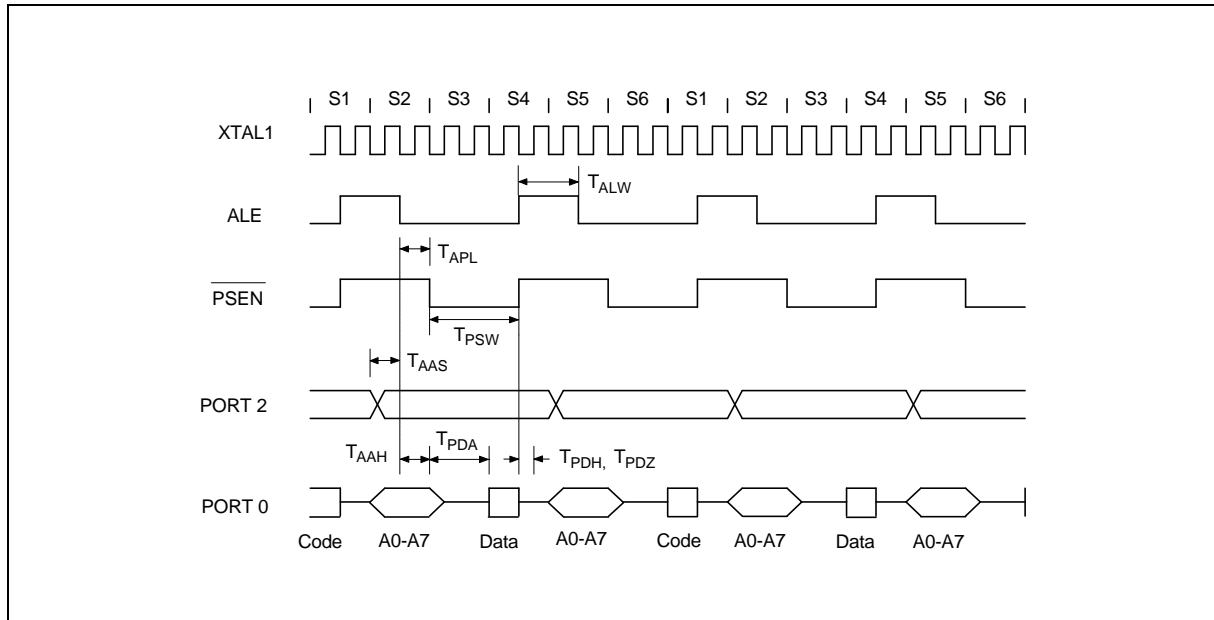
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

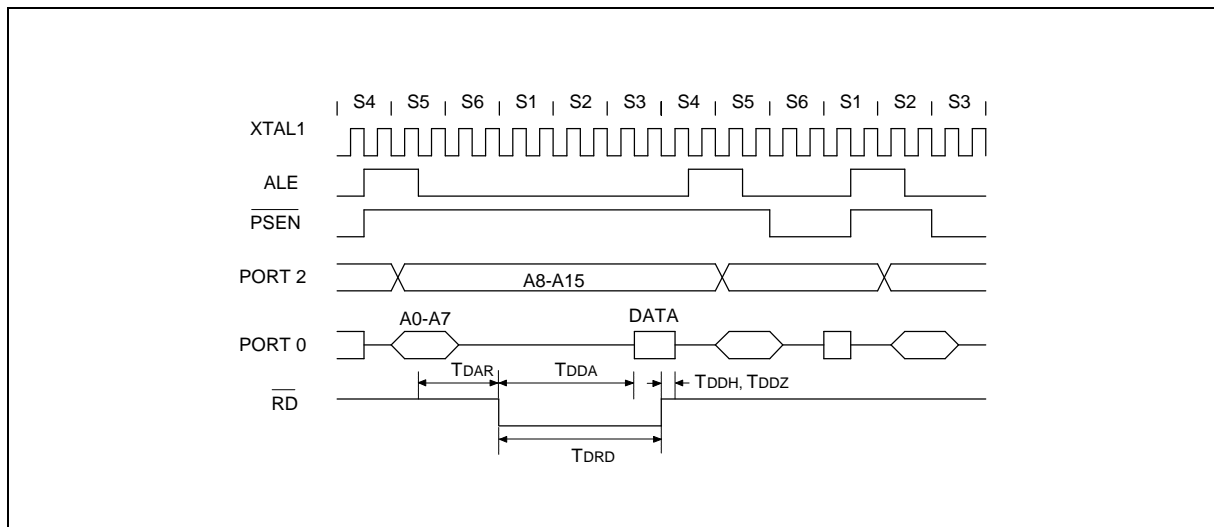
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

TIMING WAVEFORMS

Program Fetch Cycle



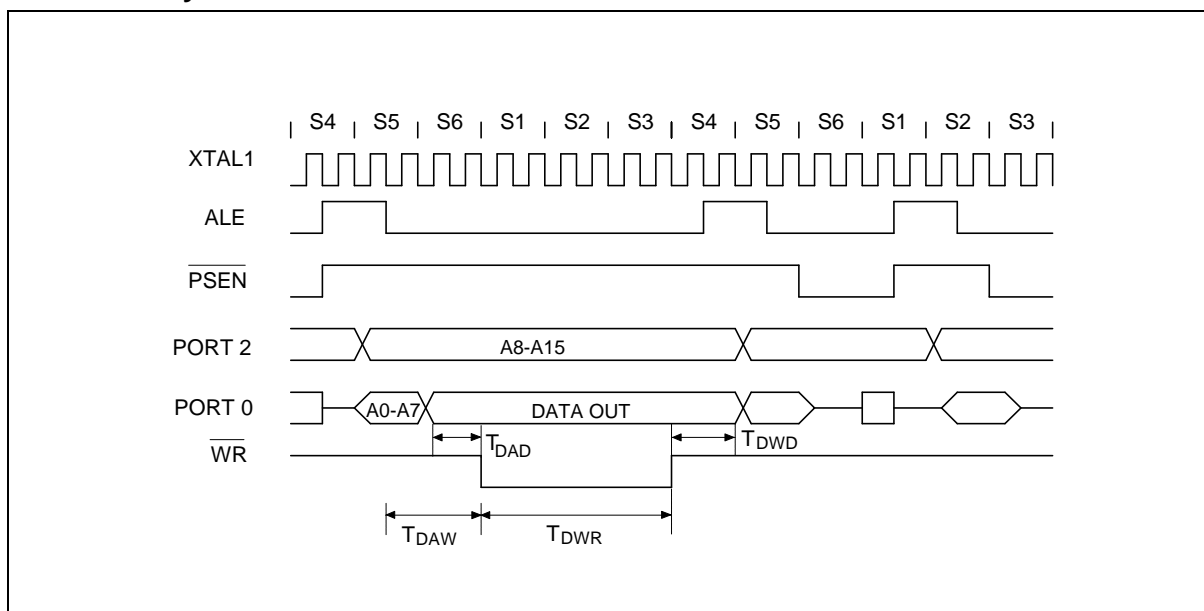
Data Read Cycle



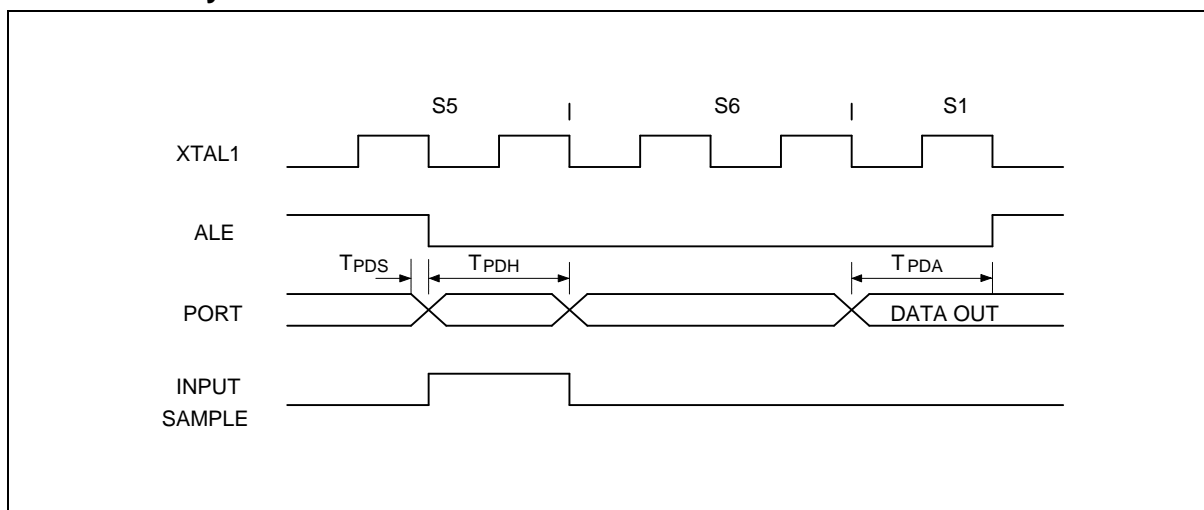


Timing Waveforms, continued

Data Write Cycle



Port Access Cycle



TYPICAL APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

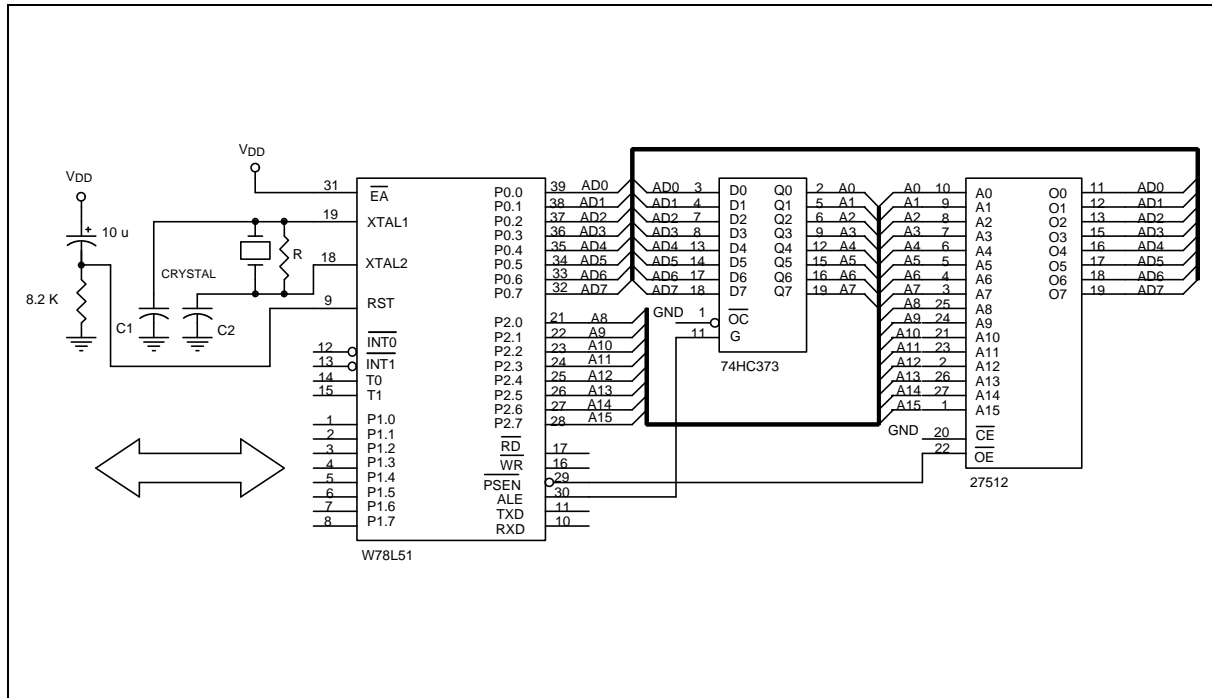


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	—
24 MHz	15P	15P	—

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

Typical Application Circuits, continued

Expanded External Data Memory and Oscillator

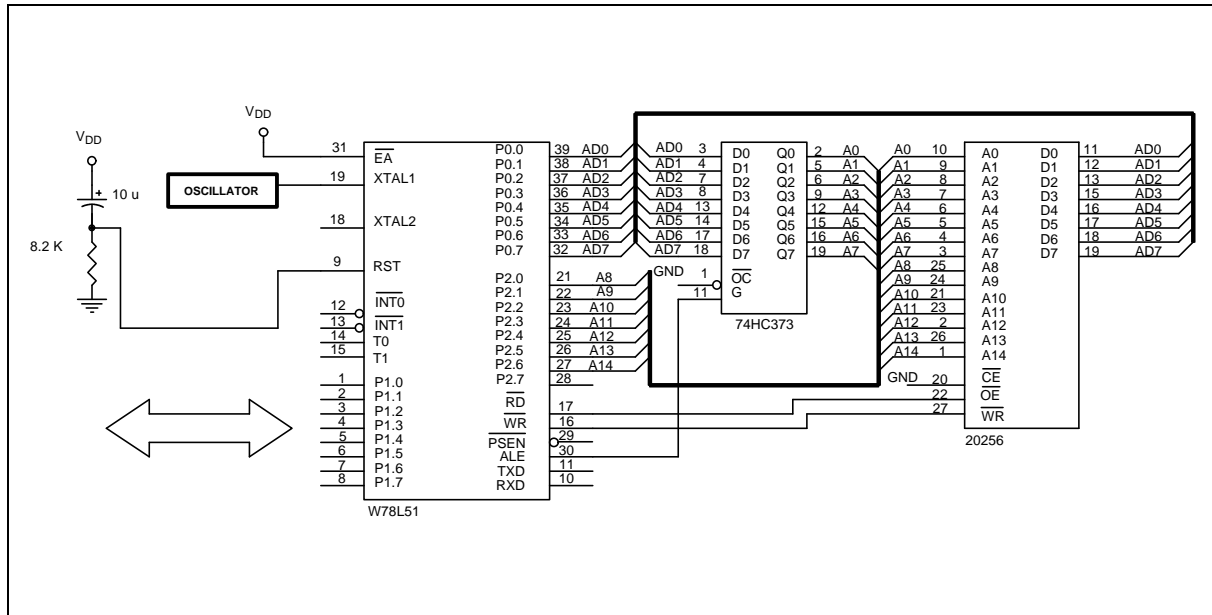
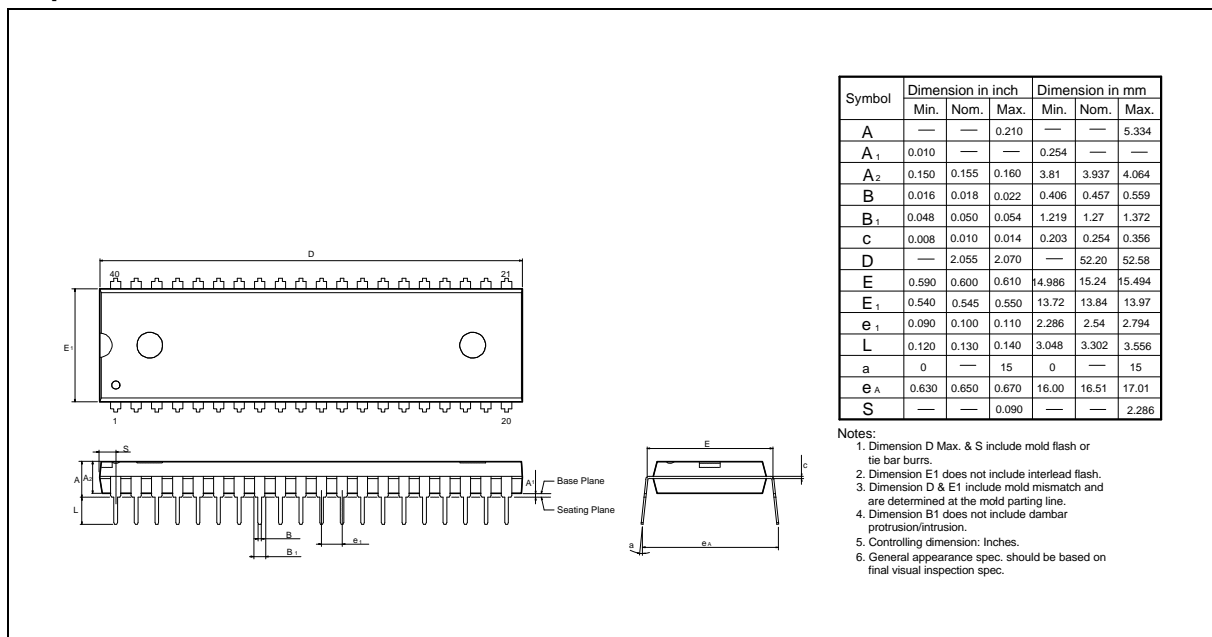


Figure B

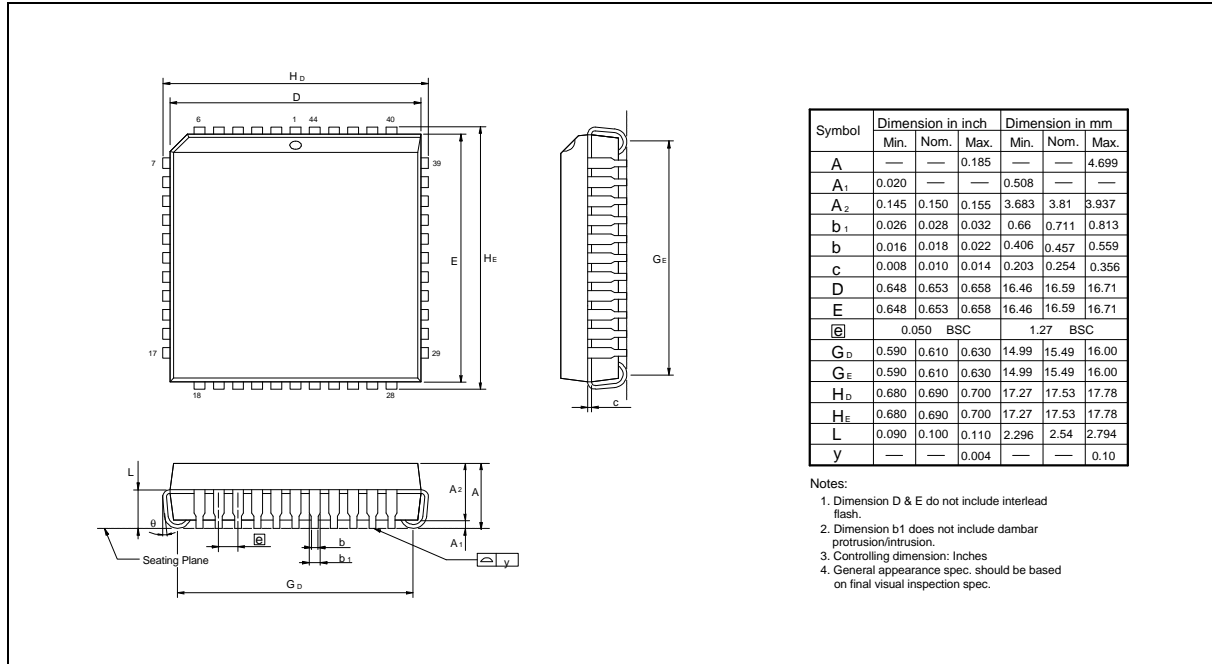
PACKAGE DIMENSIONS

40-pin DIP

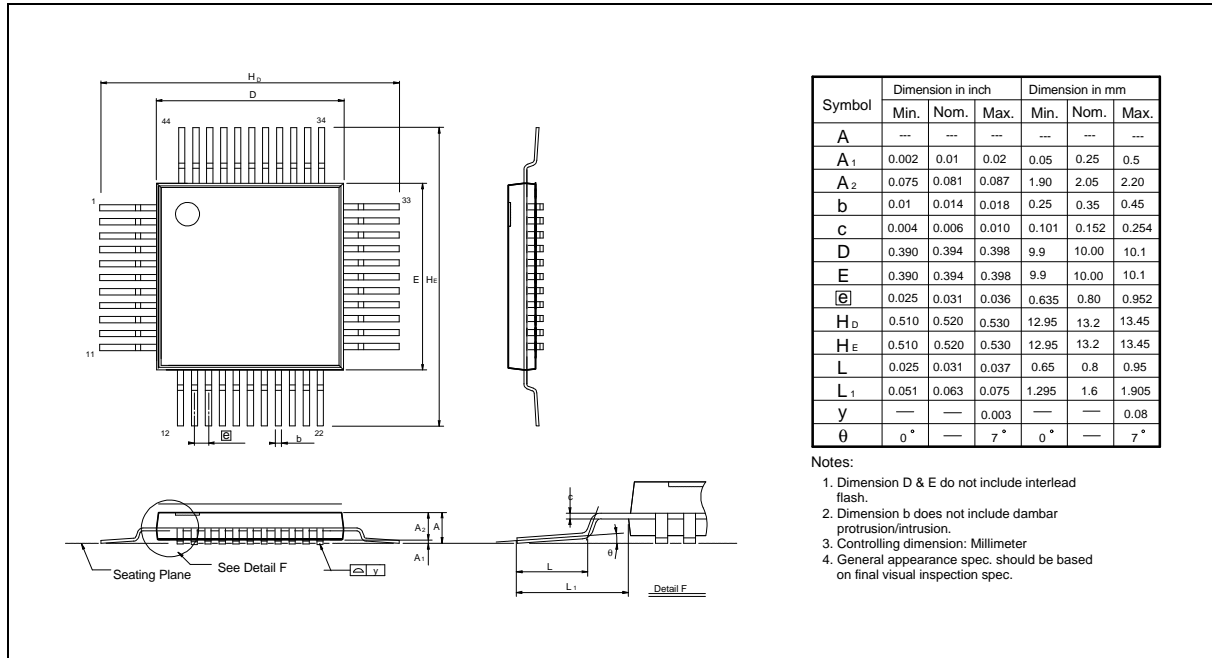


Package Dimensions, continued

44-pin PLCC



44-pin QFP



**Headquarters**

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792766
<http://www.winbond.com.tw/>
Voice & Fax-on-demand: 886-2-27197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd;
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.**Winbond Memory Lab.****Winbond Microelectronics Corp.****Winbond Systems Lab.**

2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798

Note: All data and specifications are subject to change without notice.