32M(2M × 16/4M × 8)
BOOT BLOCK FLASH MEMORY

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1. GENERAL DESCRIPTION

The W28J320B/T Flash memory chip is a high-density, cost-effective, nonvolatile, read/write storage device suited for a wide range of applications. It operates of V_{DD} = 2.7V to 3.6V, with V_{PP} of 2.7V to 3.6V or 11.7V to 12.3V. This low voltage operation capability enbales use in low power applications. The IC features a boot, parameter and main-blocked architecture, as well as low voltage and extended cycling. These features provide a highly flexible device suitable for portable terminals and personal computers. Additionally, the enhanced suspend capabilities provide an ideal solution for both code and data storage applications. For secure code storage applications, such as networking where code is either directly executed out of flash or downloaded to DRAM, the device offers four levels of protection. These are: absolute protection, enabled when $V_{PP} \leq V_{PPLK}$; selective hardware blocking; flexible software blocking; or write protection. These alternatives give designers comprehensive control over their code security needs. The device is manufactured using 0.25 μm process technology. It comes in industry-standard packaging, a 48-lead TSOP, which makes it ideal for small real estate applications.

2. FEATURES

- Low Voltage Operation
  - $V_{DD} = V_{PP}$ = 2.7V to 3.6V Single Voltage
- OTP(One Time Program) Block
  - 3963 word + 4 word Program only array
- User-Configurable × 8 or × 16 Operation
- High-Performance Read Access Time
  - 90 nS (V_{DD} = 2.7V to 3.6V)
- Operating Temperature
  - -40° C to +85° C
- Low Power Management
  - 4 μA (V_{DD} = 3.0V)Typical Standby Current
  - Automatic Power Savings Mode Decreases I_{CCR} in Static Mode
  - 120 μA (V_{DD} = 3.0V, TA =+25° C)Typical Read Current
- Optimized Array Blocking Architecture
  - Two 4k-word (8k-byte) Boot Blocks
  - Six 4k-word (8k-byte) Parameter Blocks
  - Sixty-three 32k-word (64k-byte) Main Blocks
  - Top or Bottom Boot Location
- Extended Cycling Capability
  - Minimum of 100,000 Block Erase Cycles
- Enhanced Automated Suspend Options
  - Word/Byte Write Suspend to Read
  - Block Erase Suspend to Word/Byte Write
  - Block Erase Suspend to Read
- Enhanced Data Protection Features
  - Complete Protection with $V_{PP} \leq V_{PPLK}$
  - Block Erase, Full Chip Erase, Word/Byte Write and Lock-Bit Configuration Lockout during Power Transitions
  - Block Locking with Command and #WP
  - Permanent Locking
- Automated Block Erase, Full Chip Erase, Low Power Management Word/Byte Write and Lock-Bit Configuration
  - Command User Interface (CUI)
  - Status Register (SR)
- SRAM-Compatible Write Interface
- Industry-Standard Packaging
  - 48-Lead TSOP
- Nonvolatile Flash Technology
- CMOS Process (P-type silicon substrate)
- Not designed or rated as radiation hardened

3. PRODUCT OVERVIEW

The W28J320B/T is a high-performance 32M-bit Boot Block Flash memory organized as 2M-word of 16 bits or 4M-byte of 8 bits. The 2M-word/4M-byte of data is arranged in two 4k-word/8k-byte boot blocks, six 4k-word/8k-byte parameter blocks and sixty-three 32k-word/64k-byte main blocks which are individually erasable, lockable and unlockable in-system. The memory map is shown in Figure 3.

The dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, word/byte write and lock-bit configuration operations.

A block erase operation erases one of the device's 32k-word/64k-byte blocks typically within 1.2s (3V V_{DD}, 3V V_{PP}), 4k-word/8k-byte blocks typically within 0.6s (3V V_{DD}, 3V V_{PP}) independent of other blocks. Each block can be independently erased minimum 100,000 times. Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

Writing memory data is performed in word/byte increments of the device's 32k-word blocks typically within 33 μS (3V V_{DD}, 3V V_{PP}), 64k-byte blocks typically within 31 μS (3V V_{DD}, 3V V_{PP}), 4k-word blocks typically within 36 μS (3V V_{DD}, 3V V_{PP}), 8Kbyte blocks typically within 32 μS (3V V_{DD}, 3V V_{PP}). Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits, seventy-one block lock-bits, a permanent lock-bit and #WP pin, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and word/byte write operations, while the permanent lock-bit gates block lock-bit modification and locked block alternation. Lock-bit configuration operations (Set Block Lock-Bit, Set Permanent Lock-Bit and Clear Block Lock-Bits commands) set and cleared lock-bits.

The status register indicates when the WSM's block erase, full chip erase, word/byte write or lock-bit configuration operation is finished.

The RY/#BY output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using RY/#BY minimizes both CPU overhead and system power consumption. When low, RY/#BY indicates that the WSM is performing a block erase, full chip erase, word/byte write or lock-bit configuration. RY/#BY-high Z indicates that the WSM is ready for a new command, block erase is suspended (and word/byte write is inactive), word/byte write is suspended, or the device is in reset mode.

The access time is 90 nS (t_{AVQV}) over the operating temperature range (-40° C to +85° C) and V_{DD} supply voltage range of 2.7V to 3.6V.

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 4 μA (CMOS) at 3.0V V_{DD}.

When #CE and #RESET pins are at V_{DD}, the I_{CC} CMOS standby mode is enabled. When the #RESET pin is at V_{SS}, reset mode is enabled which minimizes power consumption and provides write protection. A reset time (t_{PHQV}) is required from #RESET switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from #RESET-high until writes to the CUI are recognized. With #RESET at V_{SS}, the WSM is reset and the status register is cleared.

Overwriting a "0" to a bit already holding a data "0" may render this bit un-erasable. In order to avoid this potential "stuck bit" failure, when re-programming (changing data from "1" to "0") the following should be followed:

- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which is already holding a data "0". (Note: Since only an erase process can change the data from "0" to "1", programming "1" to a bit holding a data "0" will not change the data).

For example, changing data from "10111101" to "10111100" requires "11111110" programming.

4. BLOCK DIAGRAM

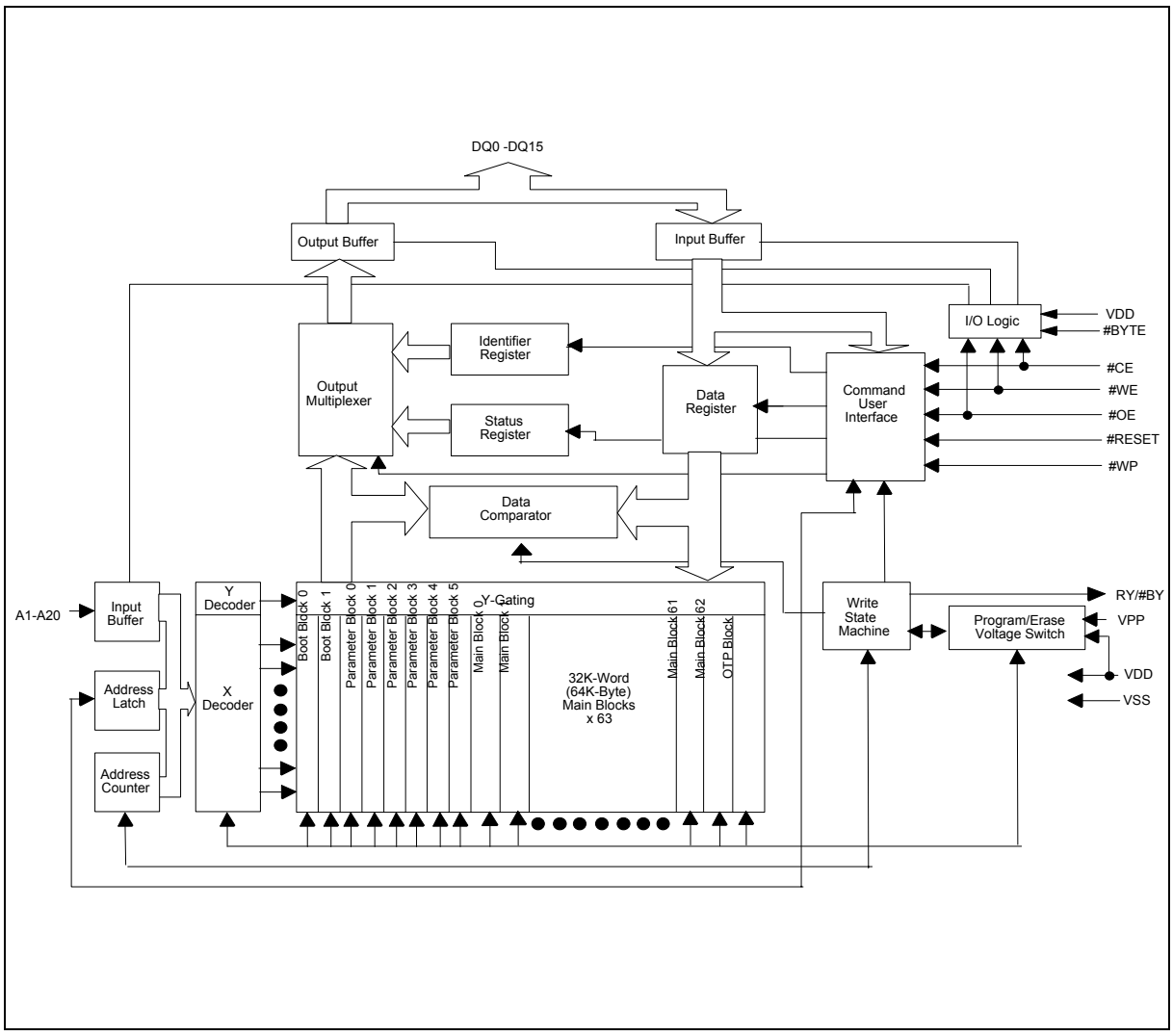


Figure 1. Block Diagram

Block Organization

This product features an asymmetrically-blocked architecture providing system memory integration. Each erase block can be erased independently of the others up to 100,000 times. For the address locations of the blocks, see the memory map in Figure 3.

Boot Blocks: The boot block is intended to replace a dedicated boot PROM in a microprocessor or microcontroller-based system. This boot block 4k words (4,096 words) features hardware controllable write protection to protect the crucial microprocessor boot code from accidental modification. The protection of the boot block is controlled using a combination of the V_{PP}, #RESET, #WP pins and block lock-bit.

Parameter Blocks: The boot block architecture includes parameter blocks to facilitate storage of frequently update small parameters that would normally require an EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. Each boot block component contains six parameter blocks of 4k words (4,096 words) each. The protection of the parameter block is controlled using a combination of the V_{PP}, #RESET and block lock-bit.

Main Blocks: The reminder is divided into main blocks for data or code storage. Each 32M-bit device contains sixty-three 32k words (32,768 words) blocks. The protection of the main block is controlled using a combination of the V_{PP}, #RESET and block lock-bit.

5. PIN CONFIGURATION

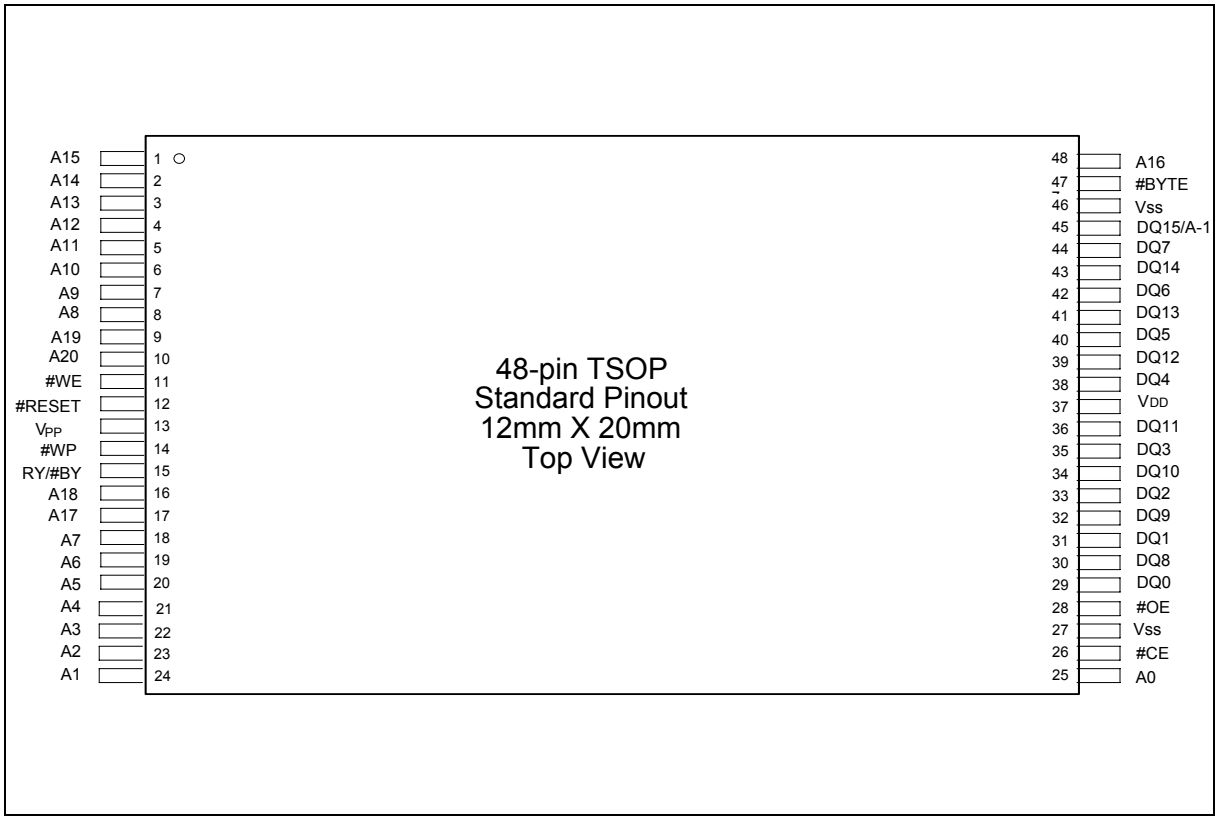


Figure 2. TSOP 48-Lead Pinout

6. PIN DESCRIPTION

SYMBOL	TYPE	NAME AND FUNCTION
A-1 A0 – A20	INPUT	**ADDRESS INPUTS**: Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A-1: Lower address input while #BYTE is V_{IL}. A-1 pin changes DQ15 pin while #BYTE is V_{IH}. A15 – A20: Main Block Address. A12 – A20: Boot and Parameter Block Address.
DQ0 – DQ15	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS**: Inputs data and commands during CUI write cycles; outputs data during memory array, status register and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a pin write cycle. DQ8 – DQ15 pins are not used while byte mode (#BYTE = V_{IL}). Then, DQ15 changes A-1address input.
#CE	INPUT	**CHIP ENABLE**: Activates the device's control logic, input buffers, decoders and sense amplifiers. #CE-high deselects the device and reduces power consumption to standby levels.
#RESET	INPUT	**RESET**: Resets the device internal automation. #RESET-high enables normal operation. When driven low, #RESET inhibits write operations which provides data protection during power transitions. Exit from reset mode sets the device to read array mode. #RESET must be V_{IL} during power-up.
#OE	INPUT	**OUTPUT ENABLE**: Gates the device's outputs during a read cycle.
#WE	INPUT	**WRITE ENABLE**: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the #WE pulse.
#WP	INPUT	**WRITE PROTECT**: When #WP is V_{IL}, boot blocks cannot be written or erased. When #WP is V_{IH}, locked boot blocks can not be written or erased. #WP is not affected parameter and main places device in byte mode (×8). All data is then input or output on blocks.
#BYTE	INPUT	**BYTE ENABLE**: #BYTE V_{IL} places the device in byte mode (×8), All data is then input or output on DQ0 – 7, and DQ8 – 15 float. #BYTE V_{IH} places the device in word mode (×16), and turns off the A-1 input buffer.
RY/#BY	OPEN DRAIN OUTPUT	**READY/#BUSY**: Indicates the status of the internal WSM. When low, the WSM is performing an internal operation (block erase, full chip erase, word/byte write or lock-bit configuration). RY/#BY-high Z indicates that the WSM is ready for new commands, block erase is suspended, and word/byte write is inactive, word/byte write is suspended, or the device is in reset mode.
V_{PP}	SUPPLY	**BLOCK ERASE, FULL CHIP ERASE, WORD/BYTE WRITE OR LOCK-BIT CONFIGURATION POWER SUPPLY**: For erasing array blocks, writing words/bytes or configuring lock-bits. With $V_{PP} \le V_{PPLK}$, memory contents cannot be altered. Block erase, full chip erase, word/byte write and lock-bit configuration with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted. Applying 12V ±0.3V to V_{PP} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{PP} may be connected to 12V ±0.3V for a total of 80 hours maximum.
V_{DD}	SUPPLY	**DEVICE POWER SUPPLY**: Do not float any power pins. With $V_{DD} \le V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{DD} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V_{SS}	SUPPLY	**GROUND**: Do not float any ground pins.

Table 1

7. PRINCIPLES OF OPERATION

The W28J320B/T flash memory includes an on-chip WSM to manage block erase, full chip erase, word/byte write and lock-bit configuration functions. It allows for: fixed power supplies during block erase, full chip erase, word/byte write and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from reset mode (see Bus Operations Section), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby and output disable operations.

Status register and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erase, full chip erase, word/byte write and lock-bit configurations. All functions associated with altering memory contents (block erase, full chip erase, word/byte write, lock-bit configuration, status and identifier codes) are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, word/byte write and lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Addresses and data are internally latched during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, word/byte write and lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read/write data from/to blocks other than that which is suspend. Word/byte write suspend allows system software to suspend a word/byte write to read data from any other flash memory array location.

Data Protection

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with two-step block erase, full chip erase, word/byte write or lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{DD} is below the write lockout voltage V_{LKO} or when #RESET is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and word/byte write operations. Refer to Table 5 for write protection alternatives.

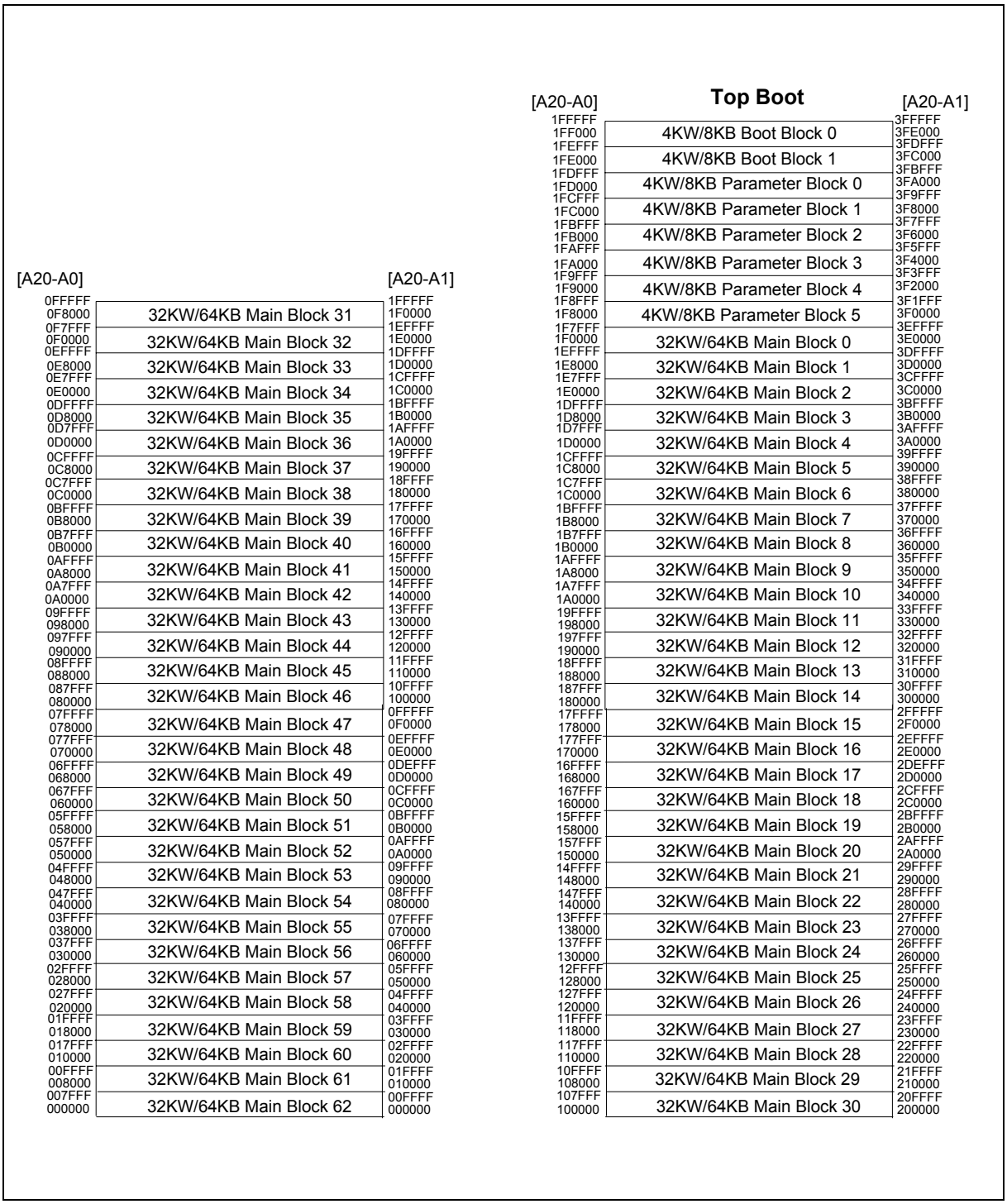


Figure 3.1 Top Boot Memory Map

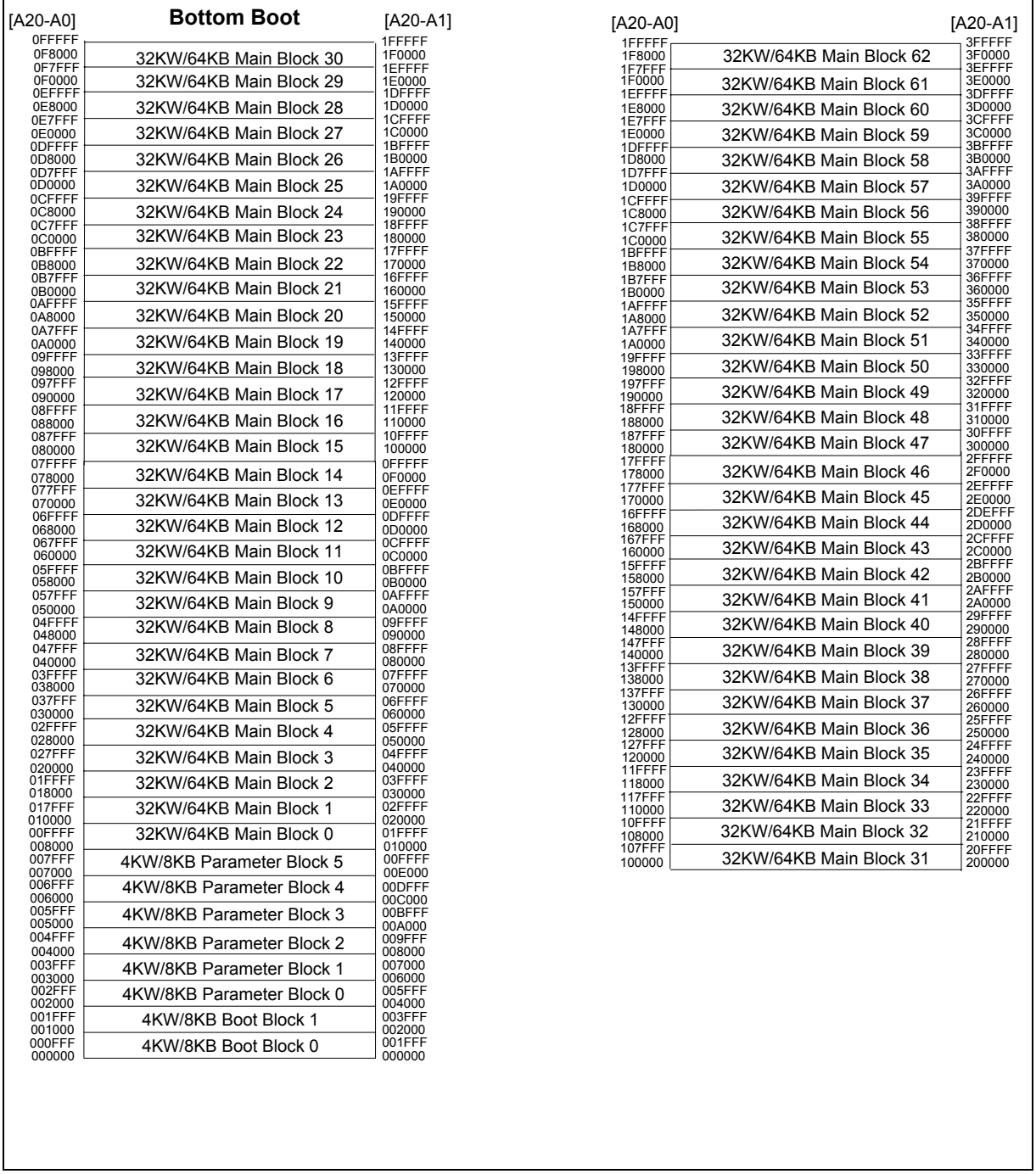


Figure 3.2 Bottom Boot Memory Map

8. BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Read

Information can be read from any block, identifier codes or status register independent of the V_{PP} voltage. #RESET can be at V_{IH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes or Read Status Register) to the CUI. Upon initial device power-up or after exit from reset mode, the device automatically resets to read array mode. Six control pins dictate the data flow in and out of the component: #CE, #OE, #BYTE, #WE, #RESET and #WP. #CE and #OE must be driven active to obtain data at the outputs. #CE is the device selection control, and when active enables the selected memory device. #OE is the data output (DQ_0 – DQ_{15}) control and when active drives the selected memory data onto the I/O bus. #BYTE is the device I/O interface mode control. #WE must be at V_{IH}, #RESET must be at V_{IH}, and #BYTE and #WP must be at V_{IL} or V_{IH}. Figure 16, 17 illustrates read cycle.

Output Disable

With #OE at a logic-high level (V_{IH}), the device outputs are disabled. Output pins (DQ0 – DQ15) are placed in a high-impedance state.

Standby

Setting #CE to a logic-high level (V_{IH}) deselects the device and places it in standby mode, which substantially reduces device power consumption. DQ0 – DQ15 outputs are placed in a high impedance state independent of #OE. If deselected during block erase, full chip erase, word/byte write or lock-bit configuration, the device continues functioning, and it continues to consume active power until the operation is completed.

Reset

Setting #RESET to V_{IL} initiates the reset mode.

In read modes, setting #RESET at V_{IL} deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. #RESET must be held low for a minimum of 100ns. A delay (t_{PHQV}) is required after return from reset until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode status register is set to 80H, and all blocks are locked.

During block erase, full chip erase, word/byte write or lock-bit configuration modes, #RESET at V_{IL} will abort the operation. RY/#BY remains low until the reset operation is complete. Memory contents at the aborted location are no longer valid since the data may be partially erased or written. A delay (t_{PHWL}) is required after #RESET goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert #RESET during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, word/byte write or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Winbond's flash memory solutions allow proper CPU initialization following a system reset through the use of the #RESET input. In this application, #RESET is controlled by the same #RESET signal that resets the system CPU.

Read Identifier Codes

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block and the permanent lock configuration code (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and permanent lock configuration codes identify locked and unlocked blocks and permanent lock-bit setting.

* Address A-1 don't care.

Figure 4. Device Identifier Code Memory Map

OTP(One Time Program) Block

The OTP block is a special block that can not be erased. The block is divided into two parts. One is a factory program area where a unique number can be written according to customer requirements in Winbond factory. This factory program area is "READ ONLY" (Already locked). The other is a customer program area that can be used by customers. This customer program area can be locked. After locking, this customer program area is protected permanently.

The OTP block is read in Configuration Read Mode by writing Read Identifier Codes command(90H). To return to Read Array Mode, write Read Array command(FFH).

The OTP block is programmed by writing OTP Program command(C0H). First write OTP Program command and then write data with address to the device (See Figure 5).

If OTP program is failed, SR.4(WORD/BYTE WRITE AND SET LOCK-BIT STATUS) bit is set to "1". And if this OTP block is locked, SR.1(DEVICE PROTECT STATUS) bit is set to "1" too.

The OTP block is also locked by writing OTP Program command(C0H). First write OTP Program command and then write data "FFFDH" with address "80H" to the device. Address "80H" of OTP block is OTP lock information. Bit 0 of address "80H" means factory program area lock status("1" is "NOT LOCKED", "0" is "LOCKED"). Bit 1 of address "80H" means customer program area lock status. The OTP lock information can not be cleared, after once it is set.

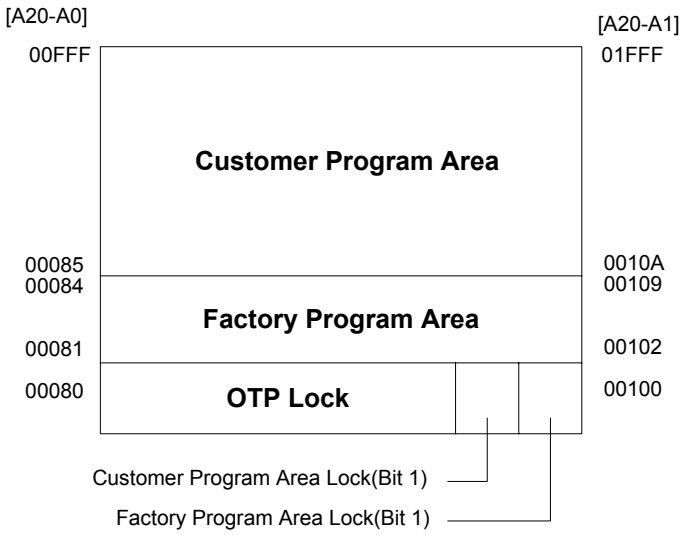


Figure 5. OTP Block Address Map

Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When V_{DD} = 2.7V to 3.6V and V_{PP} = $V_{PPH1/2}$, the CUI additionally controls block erase, full chip erase, word/byte write and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Full Chip Erase command requires appropriate command data and an address within the device. The Word/Byte Write command requires the command and address of the location to be written. Set Permanent and Block Lock-Bit commands require the command and address within the

device (Permanent Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. A write occurs when #WE and #CE are active. The address and data needed to execute a command are latched on the rising edge of #WE or #CE, whichever occurs first. Standard microprocessor write timings are used.

Figures 18 and 19 illustrate #WE and #CE controlled write operations.

9. COMMAND DEFINITIONS

When $V_{PP} \le V_{PPLK}$, read operations from the status register, identifier codes, or blocks are enabled. Setting $V_{PPH1/2} = V_{PP}$ enables successful block erase, full chip erase, word/byte write and lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 3 defines these commands.

Table 2.1. Bus Operations (#BYTE = V_{IH}) (note 1, 2)

MODE	#RESET	#CE	#OE	#WE	ADDRESS	V_{PP}	DQ0 – 15	RY/#BY(3)
Read (note 8)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	DOUT	X
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	V_{IH}	V_{IH}	X	X	X	X	High Z	X
Reset (note 4)	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes (note 8)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4, 5	X	Note 5	High Z
Write (note 6, 7, 8)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	DIN	X

Table 2.2. Bus Operations (#BYTE = V_{IL}) (note 1, 2)

MODE	#RESET	#CE	#OE	#WE	ADDRESS	V_{PP}	DQ0 – 7	RY/#BY(3)
Read (note 8)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	DOUT	X
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	V_{IH}	V_{IH}	X	X	X	X	High Z	X
Reset (note 4)	V_{IL}	X	X	X	X	X	High Z	High Z
Read Identifier Codes (note 8)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Figure 4,5	X	Note 5	High Z
Write (note 6, 7, 8)	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	DIN	X

Notes:

1. Refer to DC Characteristics. When $V_{PP} \le V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See DC Characteristics for V_{PPLK} voltages.
3. RY/#BY is V_{OL} when the WSM is executing internal block erase, full chip erase, word/byte write or lock-bit configuration algorithms. It is High Z during when the WSM is not busy, in block erase suspend mode (with word/byte write inactive), word/byte write suspend mode or reset mode.
4. #RESET at V_{SS} ±0.2V ensures the lowest power consumption.
5. See Read Identifier Codes Command section for details.
6. Command writes involving block erase, full chip erase, word/byte write or lock-bit configuration are reliably executed when $V_{PP} = V_{PPH1/2}$ and V_{DD} = 2.7V to 3.6V.
7. Refer to Table 3 for valid DIN during a write operation.
8. Never hold #OE low and #WE low at the same timing.

Table 3. Command Definitions(10)

COMMAND	BUS CYCLES REQ'D.	FIRST BUS CYCLE			SECOND BUS CYCLE		
		Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1	Write	X	FFH			
Read Identifier Codes	≥2 (note 4)	Write	X	90H	Read	IA	ID
Read Status Register	2	Write	X	70H	Read	X	SRD
Clear Status Register	1	Write	X	50H			
Block Erase	2 (note 5)	Write	X	20H	Write	BA	D0H
Full Chip Erase	2	Write	X	30H	Write	X	D0H
Word/Byte Write	2 (note 5, 6)	Write	X	40H or 10H	Write	WA	WD
Block Erase and Word/Byte Write Suspend	1 (note 5)	Write	X	B0H			
Block Erase and Word/Byte Write Resume	1 (note 5)	Write	X	D0H			
Set Block Lock-Bit	2 (note 8)	Write	X	60H	Write	BA	01H
Clear Block Lock-Bits	2 (note 7, 8)	Write	X	60H	Write	X	D0H
Set Permanent Lock-Bit	2 (note 9)	Write	X	60H	Write	X	F1H
OTP Program	2	Write	X	C0H	Write	OA	OD

Notes:

1. BUS operations are defined in Table 2.1 and Table 2.2.
2. X = Any valid address within the device.
   IA = Identifier Code Address: see Figure 4.
   BA = Address within the block being erased.
   WA = Address of memory location to be written.
   OA = Address of OTP block to be written: see Figure 5.
3. SRD = Data read from status register. See Table 6 for a description of the status register bits.
   WD = Data to be written at location WA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).
   ID = Data read from identifier codes.
   OD = Data to be written at location OA. Data is latched on the rising edge of #WE or #CE (whichever goes high first).
4. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock configuration and permanent lock configuration codes. See Read Identifier Codes Command section for details.
5. If #WP is V_{IL}, boot blocks are locked without block lock-bits state. If #WP is V_{IH}, boot blocks are locked by block lockbits. The parameter and main blocks are locked by block lock-bits without #WP state.
6. Either 40H or 10H are recognized by the WSM as the word/byte write setup.
7. The clear block lock-bits operation simultaneously clears all block lock-bits.
8. If the permanent lock-bit is set, Set Block Lock-Bit and Clear Block Lock-Bits commands can not be done.
9. Once the permanent lock-bit is set, permanent lock-bit reset is unable.
10. Commands other than those shown above are reserved by Winbond for future device implementations and should not be used.

Read Array Command

Upon initial device power-up and after exit from reset mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, word/byte write or lock-bit configuration the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend or Word/Byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and #RESET can be V_{IH}.

Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and permanent lock configuration codes (see Table 4 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and #RESET can be V_{IH}. Following the Read Identifier Codes command, the following information can be read:

Table 4. Identifier Codes

CODE		ADDRESS(2) [A20 – A0]	DATA(3) [DQ7 – DQ0]
Manufacture Code		00000H	B0H
Device Code	Top Boot	00001H	E2H
	Bottom Boot		E3H
Block Lock Configuration		BA(1)+2	
• Block is Unlocked			DQ0 = 0
• Block is Locked			DQ0 = 1
• Reserved for Future Use			DQ1 – 7
Permanent Lock Configuration		00003H	
• Device is Unlocked			DQ0 = 0
• Device is Locked ed			DQ0 = 1
• Reserved for Future Use			DQ1 – 7

Notes:

1. BA selects the specific block lock configuration code to be read. See Figure 4 for the device identifier code memory map.
2. A-1 don't care in byte mode.
3. DQ15 – DQ8 outputs 00H in word mode.

Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, word/byte write or lock-bit configuration is complete and whether the operation completed successfully. It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of #OE or #CE, whichever occurs last. #OE or #CE must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. #RESET can be V_{IH}.

Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 or SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing multiple blocks or writing several words/bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} voltage. #RESET can be V_{IH}. This command is not functional during block erase or word/byte write suspend modes.

Block Erase Command

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by a block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFFFH/FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect block erase completion by analyzing the output data of the RY/#BY pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when V_{DD} = 2.7V to 3.6V and $V_{PP} = V_{PPH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP} \le V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase for boot blocks requires that #WP = V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must be cleared the corresponding block lock-bit. If block erase is attempted when the excepting above conditions, SR.1 and SR.5 will be set to "1".

Full Chip Erase Command

This command followed by a confirm command erases all of the unlocked blocks. A full chip erase setup (30H) is first written, followed by a full chip erase confirm (D0H). After a confirm command is written, device erases the all unlocked blocks block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when can be read (see Figure 7). The CPU can detect full chip erase completion by analyzing the output data of the RY/#BY pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing. Full chip erase operation start from lower address block, finish the higher address block. Full chip erase can not be suspended.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when V_{DD} = 2.7V to

3.6V and V_{PP} = $V_{PPH1/2}$. In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful full chip erase requires for boot blocks that #WP is V_{IH} and the corresponding block lock-bit be cleared. In parameter and main blocks case, it must clear the corresponding block lock-bit. If all blocks are locked, SR.1 and SR.5 will be set to "1".

Word/Byte Write Command

Word/Byte write is executed by a two-cycle command sequence. Word/Byte write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of #WE). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 8). The CPU can detect the completion of the word/byte write event by analyzing the RY/#BY pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when V_{DD} = 2.7V to 3.6V and V_{PP} = V_{PPH1}/2. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write for boot blocks requires that #WP = V_{IH} and the corresponding block lockbit be cleared. In parameter and main blocks case, the corresponding block lock-bit must be cleared. If word/byte write is attempted under these conditions, SR.1 and SR.4 will be set to "1".

Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or word/byte write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data that must be read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). RY/#BY will also transition to High Z. The period t_{WHRZ2} defines the block erase suspend latency.

When Block Erase Suspend command writes to the CUI, if block erase is finished, the device is placed in read array mode. Therefore, after Block Erase Suspend command writes to the CUI, Read Status Register command (70H) has to write to CUI, and then status register bit SR.6 should be checked to confirm that the device is in suspend mode. At this point, a Read Array command can be written to read data from blocks other than that which is suspended.

To program data in other blocks, a Word/Byte Write command sequence can also be issued during erase suspend. Using the Word/Byte Write Suspend command (reference the Word/Byte Write Suspend Command subsection), a word/byte write operation can also be suspended. During a word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the RY/#BY output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RY/#BY will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (refer to Figure 9). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP}

level used for block erase) while block erase is suspended. #RESET must also remain at V_{IH}. #WP must also remain at V_{IL} or V_{IH} (the same #WP level used for block erase). Block erase cannot resume until word/byte write operations initiated during block erase suspend have completed.

If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than t_{ERES} and both commands are written repeatedly, a longer time is required than standard block erase until the commpletion of the operation.

Word/Byte Write Suspend Command

The Word/Byte Write Suspend command allows word/byte write interruption to read data in other flash memory locations. Once the word/byte write process starts, sending the Word/Byte Write Suspend command causes the WSM to suspend the Word/Byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the word/byte write operation has been suspended (both will be set to "1"). RY/#BY will also transition to High Z. The period t_{WHRZ1} defines the word/byte write suspend latency parameters.

When Word/Byte Write Suspend command writes to the CUI, the device is placed in read array mode if word/byte write is finished. Therefore, after Word/Byte Write Suspend command writes to the CUI, the Read Status Register command (70H) has to write to CUI, then status register bit SR.2 should be checked to confirm the device is in suspend mode.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while word/byte write is suspended are Read Status Register and Word/Byte Write Resume. After Word/Byte Write Resume command is written to the flash memory, the WSM will continue the word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and RY/#BY will return to V_{OL}. After the Word/Byte Write Resume command is written, the device automatically outputs status register data when read (reference Figure 10). V_{PP} must remain at $V_{PPH1/2}$ (the same V_{PP} level used for word/byte write) while in word/byte write suspend mode. #RESET must also remain at V_{IH}. #WP must also remain at V_{IH} or V_{OL} (the same #WP level used for word/byte write).

If the period from Word/Byte Write Resume command write to Word/Byte Write Suspend command write is too short, it can be repeated, and the write time will be prolonged.

Set Block and Permanent Lock-Bit Commands

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits, a permanent lock-bit and #WP pin. The block lock-bits and #WP pin gates program and erase operations while the permanent lock-bit gates block-lock bit modification. With the permanent lock-bit not set, individual block lock-bits can be set via the Set Block Lock-Bit command. The Set Permanent Lock-Bit command sets the permanent lock-bit. After the permanent lock-bit is set, block lock-bits and locked block contents cannot be altered. Refer to Table 5 for a summary of hardware and software write protection options.

Set block lock-bit and permanent lock-bit are executed via a two-cycle command sequence. The set block or permanent lock-bit setup, along with appropriate block or device address, is written followed by either the set block lock-bit confirm (and an address within the block to be locked) or the set permanent lock-bit confirm (and any device address). The WSM then executes the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (reference Figure 11). The CPU can detect the completion of the set lock-bit event by analyzing the RY/#BY pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up, followed by execution, ensures that lock-bits are not accidentally set. An invalid Set Block or Permanent Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when V_{DD} = 2.7V to 3.6V and V_{PP} = $V_{PPH1/2}$. In the absence of this high voltage, lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires that the permanent lock-bit be cleared. If it is attempted with the permanent lock-bit set, SR.1 and SR.4 will be set to "1" and the operation will fail.

Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. If the permanent lock-bit is not set, block lock-bits can be cleared using only the Clear Block Lock-Bits command. If the permanent lock-bit is set, block lock-bits cannot be cleared. Refer to Table 5 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (refer to Figure 12). The CPU can detect completion of the clear block lock-bits event by reading the RY/#BY Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when V_{DD} = 2.7V to 3.6V and V_{PP} = $V_{PPH1/2}$. If a clear block lock-bits operation is attempted while $V_{PP} \leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires that the permanent lock-bit is not set. If it is attempted with the permanent lock-bit set, SR.1 and SR.5 will be set to "1" and the operation will fail.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{DD} transitioning out of valid range or #RESET active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values. Once the permanent lock-bit is set, it cannot be cleared.

OTP Program Command

OTP program is executed by a two-cycle command sequence. OTP program command(C0H) is written, followed by a second write cycle that specifies the address and data (latched on the rising edge of #WE). The WSM then takes over, controlling the OTP program and program verify algorithms internally. After the OTP program command sequence is completed, the device automatically outputs status register data when read (see Figure 13). The CPU can detect the completion of the OTP program by analyzing the output data of the RY/#BY pin or status register bit SR.7.

When OTP program is completed, status register bit SR.4 should be checked. If OTP program error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully program to "0"s. The CUI remains in read status register mode until it receives other commands.

Reliable OTP program can be executed only when V_{DD} = 2.7V to 3.6V and V_{PP} = $V_{PPH1/2}$. In the absence of this voltage, memory contents are protected against OTP programs. If OTP program is attempted while $V_{PP} \le V_{PPLK}$, status register bits SR.3 and SR.4 is set to "1". If OTP write is attempted when the OTP Lock-bit is set, SR.1 and SR.4 is set to "1".

Block Locking by the #WP

This Boot Block Flash memory architecture features two hardware-lockable boot blocks so that the kernel code for the system can be kept secure while other blocks are programmed or erased as necessary.

The lockable two boot blocks are locked when #WP = V_{IL}; any program or erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two boot blocks are lockable. For the bottom configuration, the bottom two boot blocks are lockable. If #WP is V_{IH} and block lockbit is not set, boot block can be programmed or erased normally (unless V_{PP} is below V_{PPLK}). The #WP is valid only for two boot blocks, other blocks are not affected.

Table 5. Write Protection Alternatives

OPERATION	V_{PP}	#RESET	PERMANENT LOCK-BIT	BLOCK LOCK-BIT	#WP	EFFECT
Block Erase or Word/Byte Write	$\le V_{PPLK}$	X	X	X	X	All Blocks Locked.
	$> V_{PPLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	0	V_{IL}	2 Boot Blocks Locked.
					V_{IH}	Block Erase and Word/Byte Write Enabled.
				1	V_{IL}	Block Erase and Word/Byte Write Disabled.
					V_{IH}	Block Erase and Word/Byte Write Disabled.
Full Chip Erase	$\le V_{PPLK}$	X	X	X	X	All Blocks Locked.
	$> V_{PPLK}$	V_{IL}	X	X	X	All Blocks Locked.
		V_{IH}	X	X	V_{IL}	All Unlocked Blocks are Erased. 2 Boot Blocks and Locked Blocks are NOT Erased.
					V_{IH}	All Unlocked Blocks are Erased. Locked Blocks are NOT Erased.
Set Block Lock-Bit	$\le V_{PPLK}$	X	X	X	X	Set Block Lock-Bit Disabled.
	$> V_{PPLK}$	V_{IL}	X	X	X	Set Block Lock-Bit Disabled.
		V_{IH}	0	X	X	Set Block Lock-Bit. Enabled.
			1	X	X	Set Block Lock-Bit Disabled.
Clear Block Lock-Bits	$\le V_{PPLK}$	X	X	X	X	Clear Block Lock-Bits Disabled.
	$> V_{PPLK}$	V_{IL}	X	X	X	Clear Block Lock-Bits Disabled.
		V_{IH}	0	X	X	Clear Block Lock-Bits Enabled.
			1	X	X	Clear Block Lock-Bits Disabled.
Set Permanent Lock-Bit	$\le V_{PPLK}$	X	X	X	X	Set Permanent Lock-Bit Disabled.
	$> V_{PPLK}$	V_{IL}	X	X	X	Set Permanent Lock-Bit Disabled.
		V_{IH}	X	X	X	Set Permanent Lock-Bit Enabled.

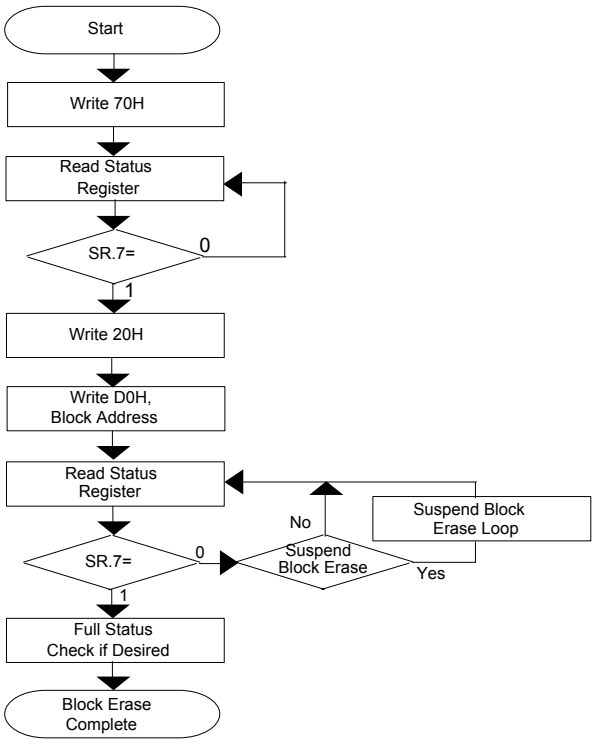
Table 6. Status Register Definition

WSMS	BESS	ECBLBS	WBWSLBS	VPPS	WBWSS	DPS	R
7	6	5	4	3	2	1	0

	Notes:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check RY/#BY or SR.7 to determine block erase, full chip erase, word/byte write or lock-bit configuration completion. SR.6-0 are invalid while SR.7 = "0".
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	
SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS (ECBLBS) 1 = Error in Block Erase, Full Chip Erase or Clear Block Lock-Bits 0 = Successful Block Erase, Full Chip Erase or Clear Block Lock-Bits	If both SR.5 and SR.4 are "1"s after a block erase, full chip erase or lock-bit configuration attempt, an improper command sequence was entered.
SR.4 = WORD/BYTE WRITE AND SET LOCK-BIT STATUS (WBWSLBS) 1 = Error in Word/Byte Write or Set Block/Permanent Lock-Bit 0 = Successful Word/Byte Write or Set Block/Permanent Lock-Bit	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPh1/2}$.
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	SR.1 does not provide a continuous indication of permanent and block lock-bit and #WP values. The WSM interrogates the permanent lock-bit, block lock-bit and #WP only after Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, permanent lock-bit is set and/or #WP is V_{IL}. Reading the block lock and permanent lock configuration codes after writing the Read Identifier Codes command indicates permanent and block lock-bit status.
SR.2 = WORD/BYTE WRITE SUSPEND STATUS (WBWSS) 1 = Word/Byte Write Suspended 0 = Word/Byte Write in Progress/Completed	

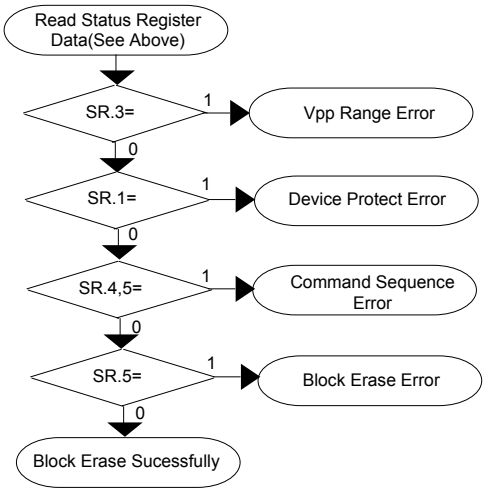
SR.1 = DEVICE PROTECT STATUS (DPS)
1 = Block Lock-Bit, Permanent Lock-Bit and/or #WP Lock Detected, Operation Abort
0 = Unlock	

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.0 is reserved for future use and should be masked out when polling the status register.



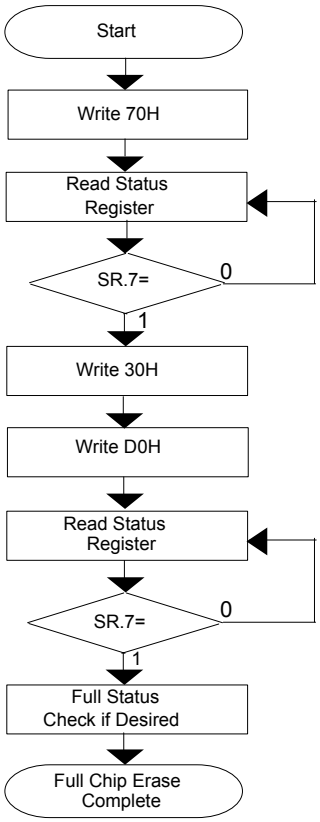
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Erase Setup	Data = 20H Addr = X
Write	Erase Confirm	Data = D0H Addr = Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent block erasures. Full status check can be done after each block erase or after a sequence of block erasures. Write FFH after the last operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



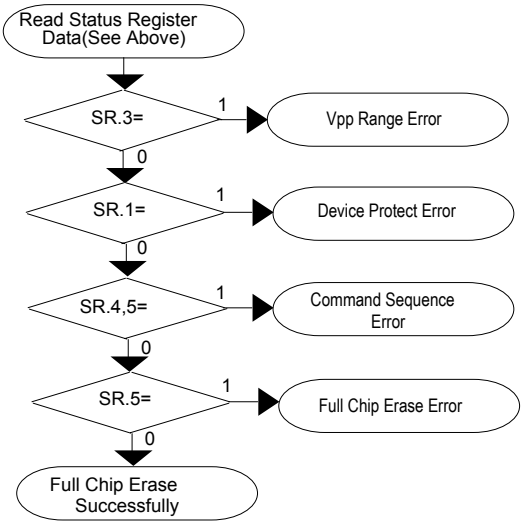
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 6. Automated Block Erase Flowchart



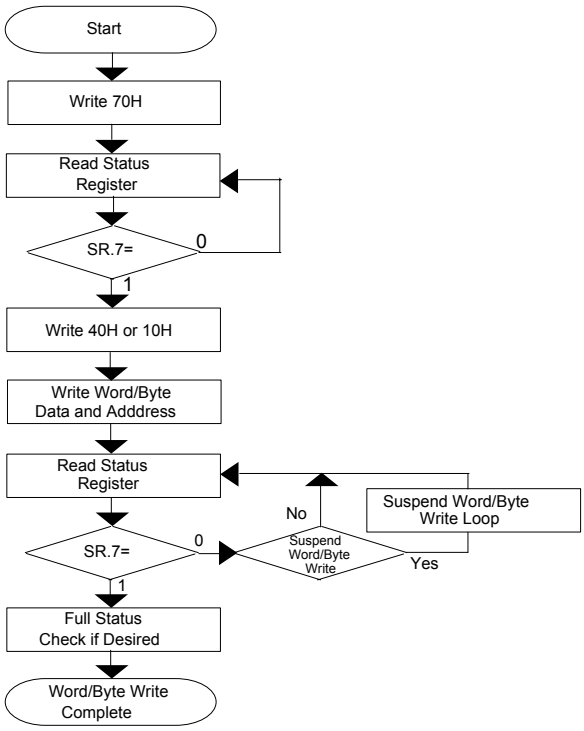
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Full Chip Erase Setup	Data = 30H Addr = X
Write	Full Chip Erase Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Full status check can be done after each full chip erase. Write FFH after the last operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



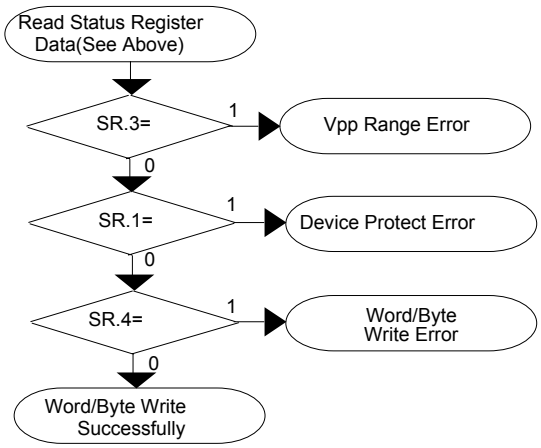
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect (All Blocks are locked)
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Full Chip Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 7. Automated Full Chip Erase Flowchart



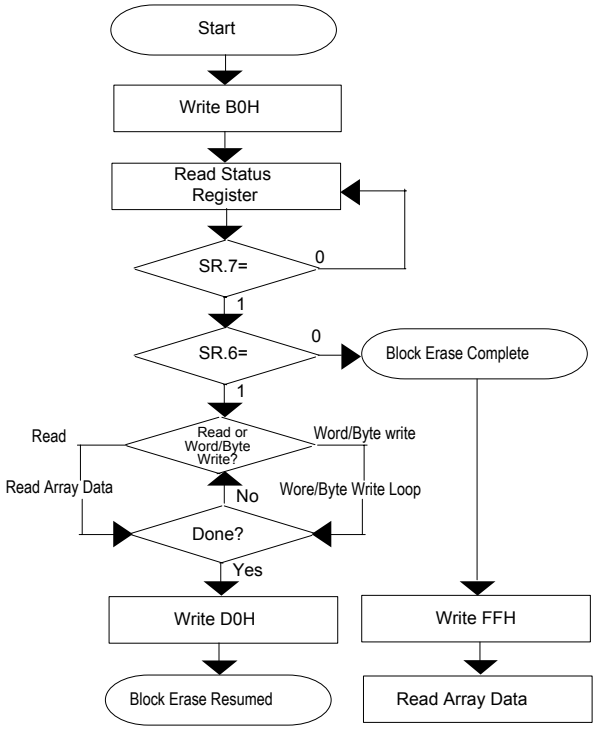
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Setup Word/Byte Write	Data = 40H or 10H Addr = X
Write	Word/Byte Write	Data = Data to Be Written Addr = Location to Be written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent word/byte writes. SR full status check can be done after each word/byte write, or after a sequence of word/byte writes. Write FFH after the last word/byte write operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



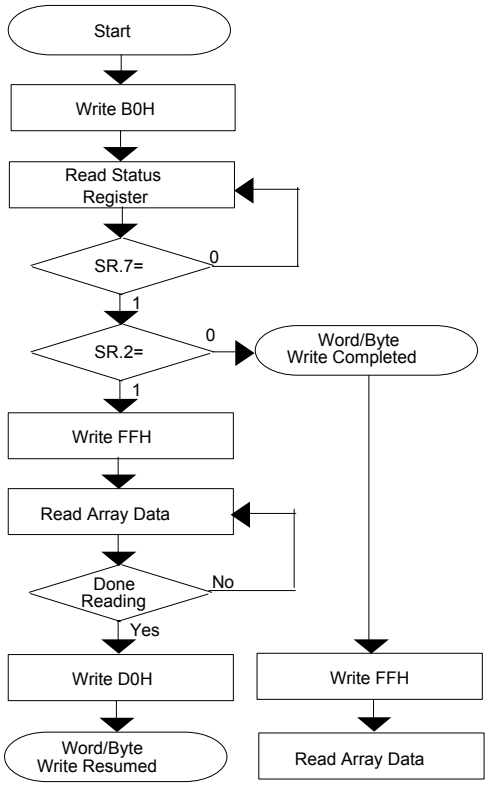
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4 1 = Data Write Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 8. Automated Word/Byte Write Flowchart



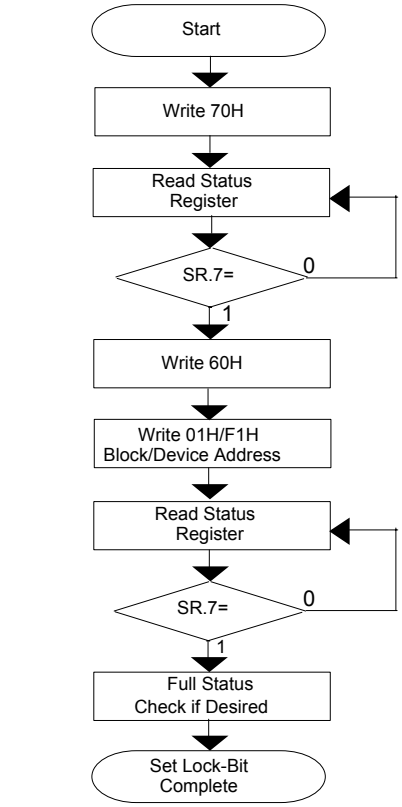
Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Block Erase Suspended 0 = Block Erase Completed
Write	Erase Resume	Data = D0H Addr = X

Figure 9. Block Erase Suspend/Resume Flowchart



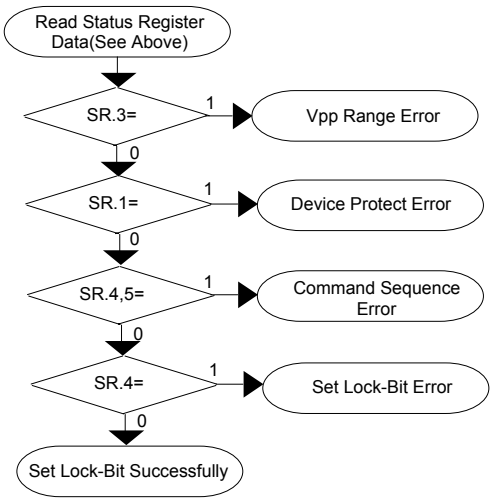
Bus Operation	Command	Comments
Write	Word/Byte Write Suspend	Data = B0H Addr = X
Read		Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Word/Byte Write Suspended 0 = Word/Byte Write Completed
Write	Read Array	Data = FFH Addr = X
Read		Read Array locations other than that being written.
Write	Word/Byte Write Resume	Data = D0H Addr = X

Figure 10. Word/Byte Write Suspend/Resume Flowchart



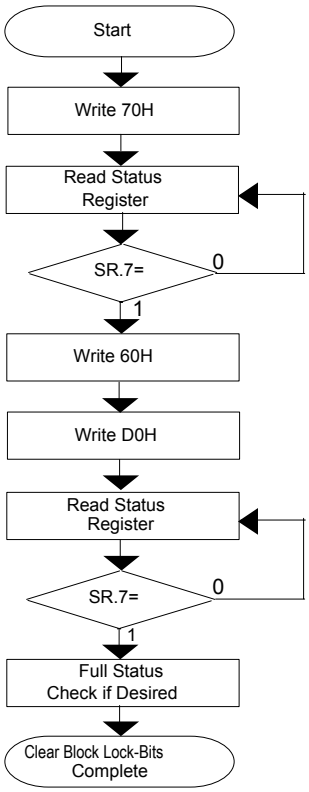
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Set Block/Permanent Lock-Bit Setup	Data = 60H Addr = X
Write	Set Block or Permanent Lock-Bit Confirm	Data = 01H (Block), F1H (Permanent) Addr = Block Address(Block), Device Address (Permanent)
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent lock-bit set operations. Full status check can be done after each lock-bit set operation or after a sequence of lock-bit set operations. Write FFH after the last lock-bit set operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



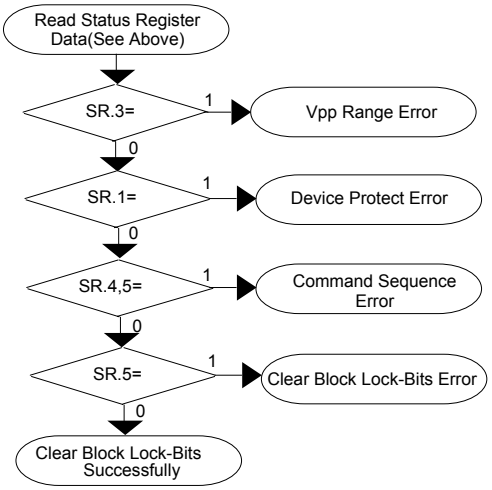
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect Permanent Lock-Bit is Set (Set Block Lock-Bit Operation)
Standby		Check SR.4, 5 Both 1 = Command Sequence Error
Standby		Check SR.4 1 = Set Lock-Bit Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple lock-bits are set before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 11. Set Block and Permanent Lock-Bit Flowchart



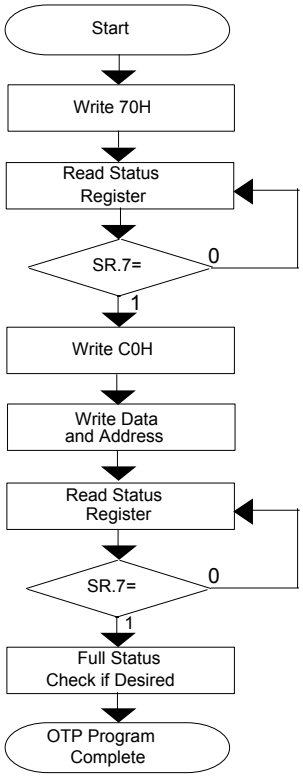
Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Clear Block Lock-Bits Setup	Data = 60H Addr = X
Write	Clear Block Lock-Bits Confirm	Data = D0H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



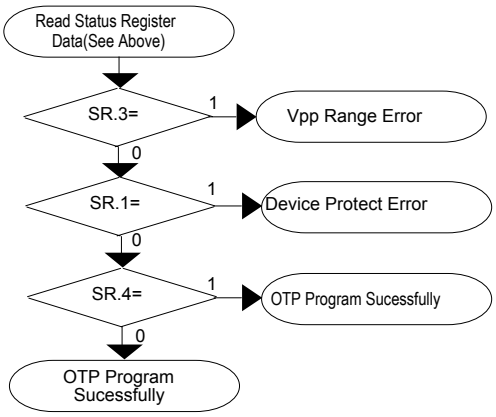
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect Permanent Lock-Bit is Set
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Clear Block Lock-Bits Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 12. Clear Block Lock-Bits Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data = 70H Addr = X
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Write	Setup OTP Program	Data = C0H Addr = X
Write	OTP Program	Data = Data to Be Written Addr = Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent OTP programs. SR full status check can be done after each OTP program, or after a sequence of OTP programs. Write FFH after the last OTP program operation to place device in read array mode.		

Full STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Error Detect
Standby		Check SR.1 1 = Device Protect Detect
Standby		Check SR.4 1 = Data Write Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 13. Automated OTP Program Flowchart

10. DESIGN CONSIDERATIONS

Three-Line Output Control

This device will often be used in large memory arrays. Winbond provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

a. Lowest possible memory power dissipation.
b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable #CE while #OE should be connected to all memory devices and the system's #READ control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. #RESET should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

RY/#BY and WSM Polling

RY/#BY is an open drain output that should be connected to V_{DD} by a pull up resistor to provides a hardware method of detecting block erase, full chip erase, word/byte write and lock-bit configuration completion. It transitions low after block erase, full chip erase, word/byte write or lockbit configuration commands and returns to V_{OH} (while RY/#BY is pull up) when the WSM has finished executing the internal algorithm.

RY/#BY can be connected to an interrupt input of the system CPU or controller. It is active at all times. RY/#BY is also high impedance when the device is in block erase suspend (with word/byte write inactive), word/byte write suspend or reset modes.

Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of #CE and #OE. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks.

Each device should have a 0.1μF ceramic capacitor connected between V_{DD} and V_{SS} and between V_{PP} and V_{SS}. These high frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection between V_{DD} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} power supply trace. The V_{PP} pin supplies the memory cell current for word/byte writing and block erasing. Use similar trace widths and layout considerations given to the V_{DD} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

V_{DD}, V_{PP}, #RESET Transitions

Block erase, full chip erase, word/byte write and lock-bit configuration are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2}$ range, V_{DD} falls outside of a valid 2.7V to 3.6V range, or #RESET ≠ V_{IH}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If #RESET transitions to V_{IL} during block erase, full chip erase, word/byte write or

lock-bit configuration, RY/#BY will remain low until the reset operation is complete. Then, the operation will abort and the device will enter reset mode. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or #RESET transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or #CE transitions or WSM actions. Its state is read array mode upon power-up, after exit from reset mode or after V_{DD} transitions below V_{LKO}.

Power-Up/Down Protection

The device is designed to offer protection against accidental block erase, full chip erase, word/byte write or lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{DD}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{DD} voltages above V_{LKO} when V_{PP} is active. Since both #WE and #CE must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while #RESET = V_{IL} regardless of its control inputs state.

Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's non-volatility increases usable battery life because data is retained when system power is removed.

Data Protection Method

On some systems, noise having a level exceeding the limit dictated in the specification may be generated under specific operating conditions. Such noise, when induced onto #WE signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against undesired overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block

When a lock bit is set, the corresponding block (includes the 2 boot blocks) is protected against overwriting. By setting a #WP low, only the 2 boot blocks can be protected against overwriting. By using this feature, the flash memory space can be divided into the program section (locked section) and data section (unlocked section). The permanent lock bit can be used to prevent false block bit setting. For further information on setting/resetting lock-bit, refer to the specification.

2) Data protection through V_{PP}

When the level of V_{PP} is lower than V_{PPLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected. For the lockout voltage, refer to the specification.

3) Data protection through #RESET

When the #RESET is kept low during read mode, the flash memory will be in reset mode, write protecting all blocks. When the #RESET is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks. For the details of #RESET control, refer to the specification.

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings*

Operating Temperature
During Read, Block Erase, Full Chip Erase, Word/Byte Write
and Lock-Bit Configuration ..... -40°C to +85°C (1)

Storage Temperature
During under Bias ..... -40°C to +85°C
During non Bias ..... –65°C to +125C

Voltage On Any Pin
(except V_{DD} and V_{PP}) ..... -0.5V to V_{DD} +0.5V(2)

V_{DD} Supply Voltage..... -0.2V to +4.6V(2)

V_{PP} Supply Voltage..... -0.2V to +13.0V(2,3)

Output Short Circuit Current.....100 mA(4)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Notes:

1. The operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to V_{SS}. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{DD} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20 nS. Maximum DC voltage on input/output pins are V_{DD} +0.5V which, during transitions, may overshoot to V_{DD} +2.0V for periods <20 nS.
3. Maximum DC voltage on V_{PP} may overshoot to +13.0V for periods <20 nS. Applying 12V ±0.3V to V_{PP} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{PP} may be connected to 12V ±0.3V for a total of 80 hours maximum.
4. Output shorted for no more than one second. No more than one output shorted at a time.

Operating Conditions

Temperature and V_{DD} Operating Conditions

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	TEST CONDITION
Operating Temperature	T_A	-40	+85	°C	Ambient Temperature
V_{DD} Supply Voltage (2.7V to 3.6V)	V_{DD}	2.7	3.6	V	

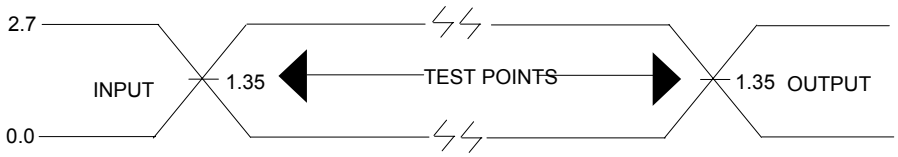
Capacitance(1)

T_A = +25° C, f = 1 MHz

PARAMETER	SYMBOL	TYP.	MAX.	UNIT	CONDITION
Input Capacitance	C_{IN}	7	10	pF	V_{IN} = 0.0V
Output Capacitance	C_{OUT}	9	12	pF	V_{OUT} = 0.0V

Note: Sampled, not 100% tested.

AC Input/Output Test Conditions



AC test inputs are driven at 2.7V for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends, at 1.35V. Input rise and fall times (10% to 90%) <10 nS.

Figure 14. Transient Input/Output Reference Waveform for V_{DD} = 2.7V to 3.6V

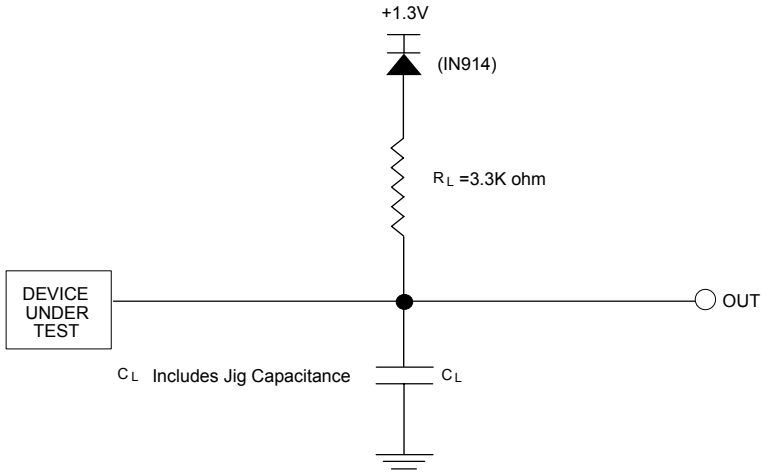


Figure 15. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

TEST CONFIGURATION	CL (pF)
V_{DD} = 2.7V to 3.6V	50

DC Characteristics

PARAMETER	SYM.	TEST CONDITIONS	V_{DD} = 2.7V – 3.6V		UNIT
			Typ.	Max.	
Input Load Current (note 1)	I_{LI}	$V_{DD} = V_{DD}$ Max. VIN = V_{DD} or V_{SS}		±0.5	µA
Output Leakage Current (note 1)	I_{LO}	$V_{DD} = V_{DD}$ Max. VOUT = V_{DD} or V_{SS}		±0.5	µA
V_{DD} Standby Current (note1, 3)	I_{CCS}	$V_{DD} = V_{DD}$ Max. #CE = #RESET = V_{DD} ±0.2V	4	20	µA
V_{DD} Auto Power-Save Current (note1, 5)	I_{CCAS}	$V_{DD} = V_{DD}$ Max. #CE = V_{SS} ±0.2V	4	20	µA
V_{DD} Reset Power-Down Current (note 1)	I_{CCD}	#RESET = V_{SS} ±0.2V IOUT (RY/#BY) = 0 mA	4	20	µA

V_{DD} Read Current (note 1)	I_{CCR}	$V_{DD} = V_{DD}$ Max., #CE = V_{SS},
		f = 5 MHz, I_{OUT} = 0 mA
			15	30	mA

V_{DD} Word/Byte Write or Set Lock-Bit Current (note 1, 6)	I_{CCW}	V_{PP} = 2.7V – 3.6V	5	17	mA
		V_{PP} = 11.7V – 12.3V	5	12	mA
V_{DD} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current (note 1, 6)	I_{CCE}	V_{PP} = 2.7V – 3.6V	4	17	mA
		V_{PP} = 11.7V – 12.3V	4	12	mA
V_{DD} Word/Byte Write or Block Erase Suspend Current (note 1, 2)	I_{CCWS} I_{CCES}	#CE = V_{IH}	1	6	mA
V_{PP} Standby or Read Current (note 1)	I_{CCWS}	$V_{PP} \leq V_{DD}$	±2	±15	µA
	I_{CCWR}	$V_{PP} > V_{DD}$	10	200	µA
V_{PP} Auto Power-Save Current (note 1, 5)	I_{CCWAS}	$V_{DD} = V_{DD}$ Max. #CE = V_{SS} ±0.2V	0.1	5	µA
V_{PP} Reset Power-Down Current (note 1)	I_{CCWD}	#RESET = V_{SS} ±0.2V	0.1	5	µA
V_{PP} Word/Byte Write or Set Lock-Bit Current (note 1, 6)	I_{CCWW}	V_{PP} = 2.7V – 3.6V	12	40	mA
		V_{PP} = 11.7V – 12.3V		30	mA
V_{PP} Block Erase, Full Chip Erase or Clear Block Lock-Bits Current (note 1, 6)	I_{CCWE}	V_{PP} = 2.7V – 3.6V	8	25	mA
		V_{PP} = 11.7V – 12.3V		20	mA
V_{PP} Word/Byte Write or Block Erase Suspend Current (note 1)	I_{CCWWS} I_{CCWES}	$V_{PP} = V_{PPH1/2}$	10	200	µA

DC Characteristics, continued.

PARAMETER	SYM.	TEST CONDITIONS	V_{DD} = 2.7V – 3.6V		UNIT
			Typ.	Max.	
Input Low Voltage (note 6)	V_{IL}		-0.5	0.4	V
Input High Voltage (note 6)	V_{IH}		V_{DD} -0.4	V_{DD} +0.5	V
Output Low Voltage (note 3, 6)	V_{OL}	V_{DD} = V_{DD} Min. I_{OL} = 2.0 mA		0.4	V
Output High Voltage (note 6)	V_{OH}	V_{DD} = V_{DD} Min. I_{OH} = -100 mA	V_{DD} -0.4		V
V_{PP} Lockout during Normal Operations (note 4, 6)	V_{PPLK}			1.0	V
V_{PP} during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration Operations	V_{PPH1}		2.7	3.6	V
V_{PP} during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration Operations (note 7)	V_{PPH2}		11.7	12.3	V
V_{DD} Lockout Voltage	V_{LKO}		2.0		V

Notes:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{DD} voltage and T_A = +25° C.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or word/byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes RY/#BY.
4. Block erases, full chip erase, word/byte writes and lock-bit configurations are inhibited when $V_{PP} \le V_{PPLK}$, and not guaranteed in the range between V_{PPLK} (max.) and V_{PPH1} (min.), between V_{PPH1} (max.) and V_{PPH2} (min.) and above V_{PPH2} (max.).
5. The Automatic Power Savings (APS) feature is placed automatically power save mode that addresses not switching more than 300ns while read mode.
7. Sampled, not 100% tested.
8. Applying 12V ±0.3V to V_{PP} during erase/write can only be done for a maximum of 1000 cycles on each block. V_{PP} may be connected to 12V ±0.3V for a total of 80 hours maximum.

AC Characteristics – Read-only Operations(1)

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Read Cycle Time	t_{AVAV}	90		nS
Address to Output Delay	t_{AVQV}		90	nS
#CE to Output Delay (note 2)	t_{ELQV}		90	nS
#RESET High to Output Delay	t_{PHQV}		600	nS
#OE to Output Delay (note 2)	t_{GLQV}		40	nS
#CE to Output in Low Z (note 3)	t_{ELQX}	0		nS
#CE High to Output in High Z (note 3)	t_{EHQZ}		40	nS
#OE to Output in Low Z (note 3)	t_{GLQX}	0		nS
#OE High to Output in High Z (note 3)	t_{GHQZ}		15	nS
Output Hold from Address, #CE or #OE Change, Whichever Occurs First (note 3)	t_{OH}	0		nS
#BYTE to Output Delay (note 3)	t_{FVQV}		90	nS
#BYTE Low to Output in High Z (note 3)	t_{FLQZ}		25	nS
#CE to #BYTE High or Low (note 3, 4)	t_{ELFV}		5	nS

Notes:

1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. #OE may be delayed up to t_{ELQV} to t_{GLQV} after the falling edge of #CE without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. If #BYTE transfer during reading cycle, exist the regulations separately.

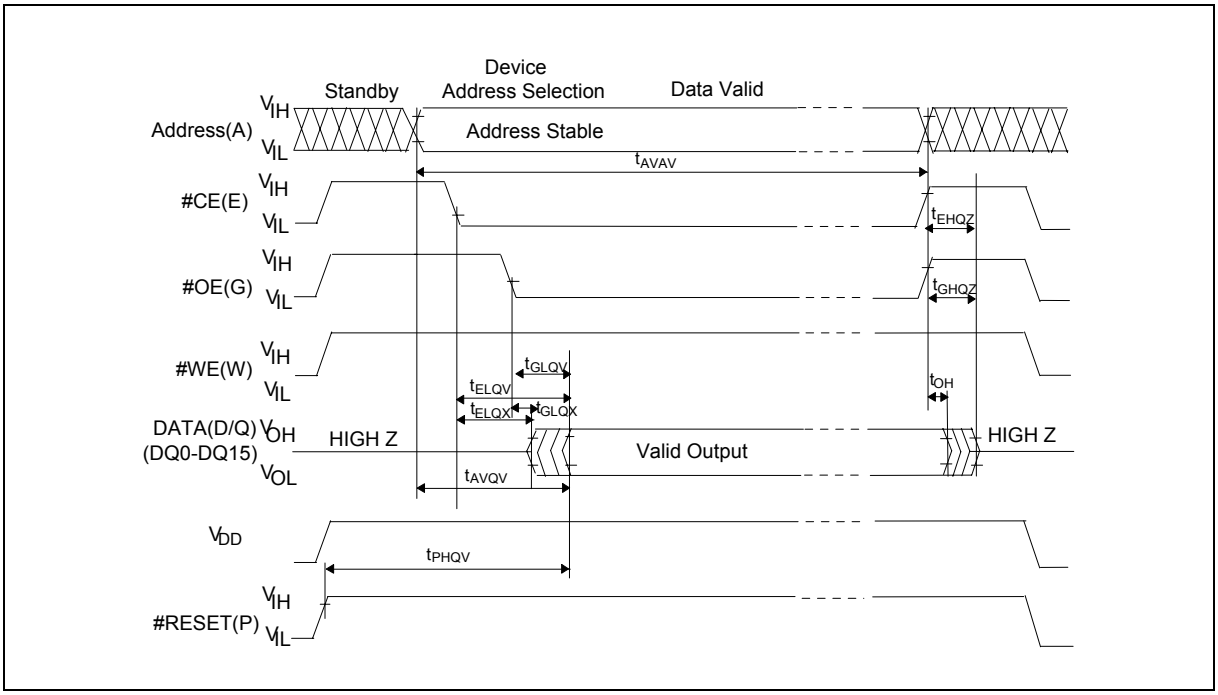


Figure 16. AC Waveform for Read Operations

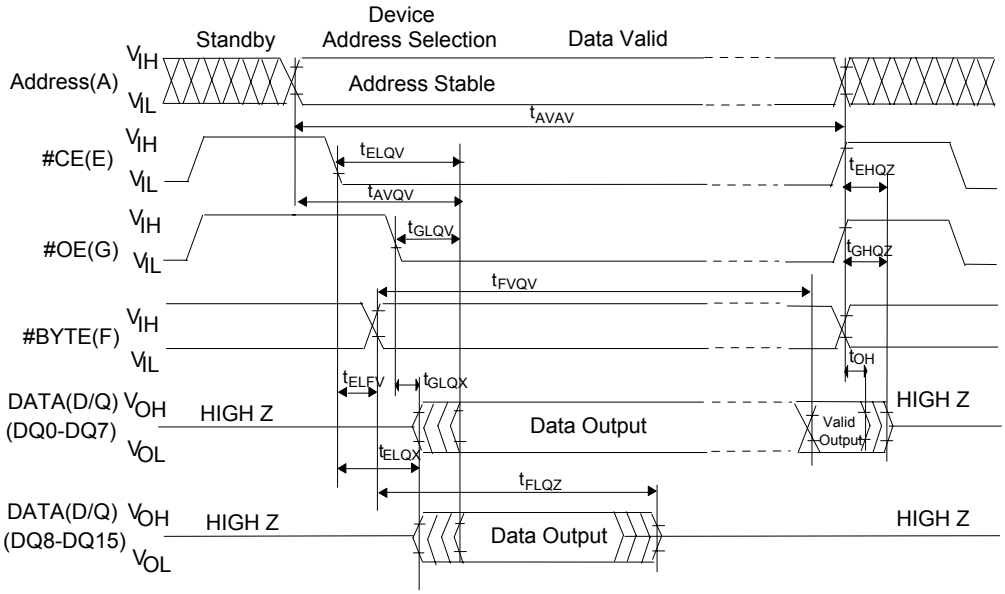


Figure 17. #BYTE timing Waveform

AC Characteristics - Write Operations(1)

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	90		nS
#RESET High Recovery to #WE Going Low (note 2)	t_{PHWL}	1		µS
#CE Setup to #WE Going Low	t_{ELWL}	10		nS
#WE Pulse Width	t_{WLWH}	50		nS
#WP V_{IH} Setup to #WE Going High (note 2)	t_{SHWH}	100		nS
V_{PP} Setup to #WE Going High (note 2)	t_{VPWH}	100		nS
Address Setup to #WE Going High (note 3)	t_{AVWH}	50		nS
Data Setup to #WE Going High (note 3)	t_{DVWH}	50		nS
Data Hold from #WE High	t_{WHDX}	0		nS
Address Hold from #WE High	t_{WHAX}	0		nS
#CE Hold from #WE High	t_{WHEH}	10		nS
#WE Pulse Width High	t_{WHWL}	30		nS
#WE High to RY/#BY Going Low or SR.7 Going "0"	t_{WHRL}		100	nS
Write Recovery before Read	t_{WHGL}	0		nS
V_{PP} Hold from Valid SRD, RY/#BY High Z (note 2, 4)	t_{QVVL}	0		nS
#WP V_{IH} Hold from Valid SRD, RY/#BY High Z (note 2, 4)	t_{QVSL}	0		nS
#BYTE Setup to #WE Going High (note 5)	t_{FVWH}	50		nS
#BYTE Hold from #WE High (note 5)	t_{WHFV}	90		nS

Notes:

1. Read timing characteristics during block erase, full chip erase, word/byte write and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase, full chip erase, word/byte write or lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2}$ until determination of block erase, full chip erase, word/byte write or lock-bit configuration success (SR.1/3/4/5 = 0).
5. If #BYTE switch during reading cycle, exist the regulations separately.

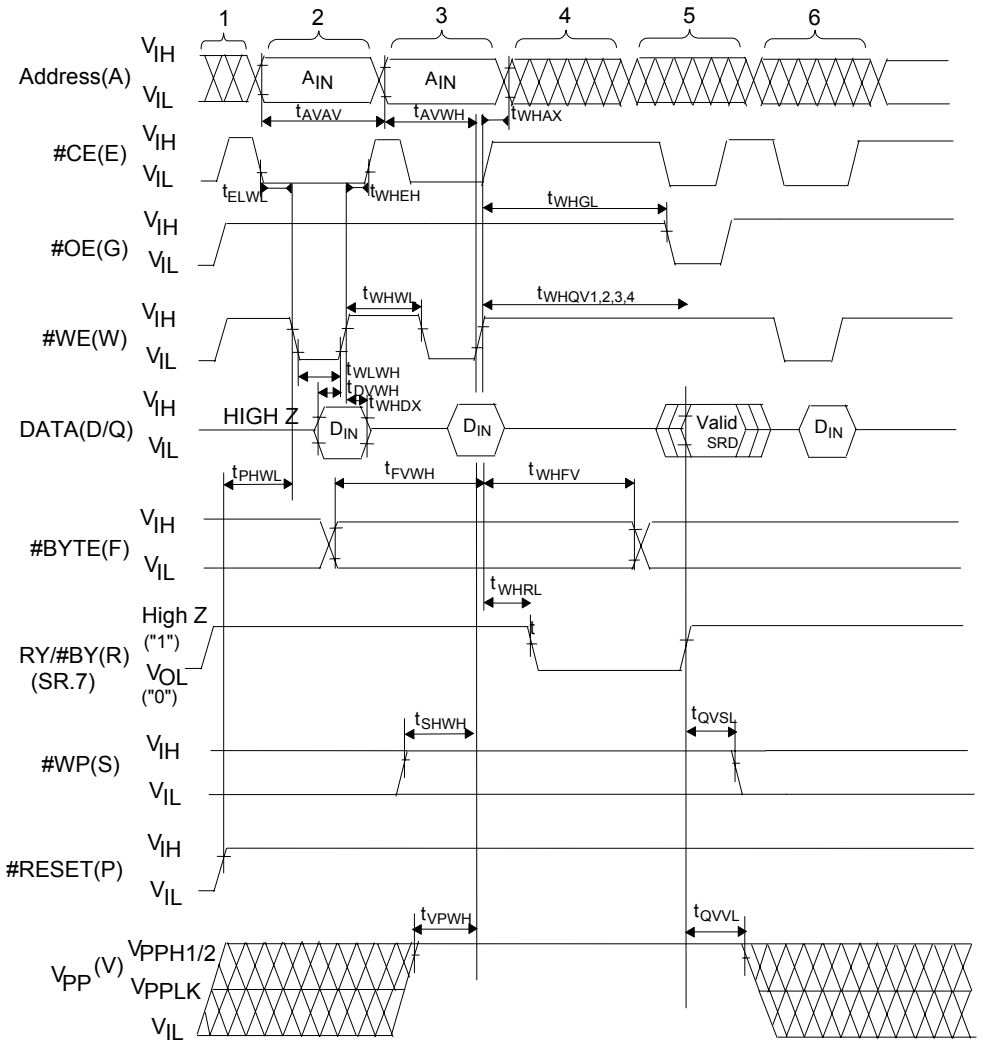


Figure 18. AC Waveform for #WE-Controlled Write Operations

Notes:

1. V_{DD} power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Alternative #CE - Controlled Writes(1)

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

PARAMETER	SYM.	MIN.	MAX.	UNIT
Write Cycle Time	t_{AVAV}	90		nS
#RESET High Recovery to #CE Going Low (note 2)	t_{PHEL}	1		µS
#WE Setup to #CE Going Low	t_{WLEL}	0		nS
#CE Pulse Width	t_{ELEH}	65		nS
#WP V_{IH} Setup to #CE Going High (note 2)	t_{SHEH}	100		nS
V_{PP} Setup to #CE Going High (note 2)	t_{VPEH}	100		nS
Address Setup to #CE Going High (note 3)	t_{AVEH}	50		nS
Data Setup to #CE Going High (note 3)	t_{DVEH}	50		nS
Data Hold from #CE High	t_{EHDX}	0		nS
Address Hold from #CE High	t_{EHAX}	0		nS
#WE Hold from #CE High	t_{EHWH}	0		nS
#CE Pulse Width High	t_{EHEL}	25		nS
#CE High to RY/#BY Going Low or SR.7 Going "0"	t_{EHRL}		100	nS
Write Recovery before Read	t_{EHGL}	0		nS
V_{PP} Hold from Valid SRD, RY/#BY High Z (note 2, 4)	t_{QVVL}	0		nS
#WP V_{IH} Hold from Valid SRD, RY/#BY High Z (note2, 4)	t_{QVSL}	0		nS
#BYTE Setup to #CE Going High (note5)	t_{FVEH}	50		nS
#BYTE Hold from #CE High (note5)	t_{EHFV}	90		nS

Notes:

1. In systems where #CE defines the write pulse width (within a longer #WE timing waveform), all setup, hold, and inactive #WE times should be measured relative to the #CE waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid AIN and DIN for block erase, full chip erase, word/byte write or lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2}$ until determination of block erase, full chip erase, word/byte write or lock-bit configuration success (SR.1/3/4/5 = 0).
5. If #BYTE switch during reading cycle, exist the regulations separately.

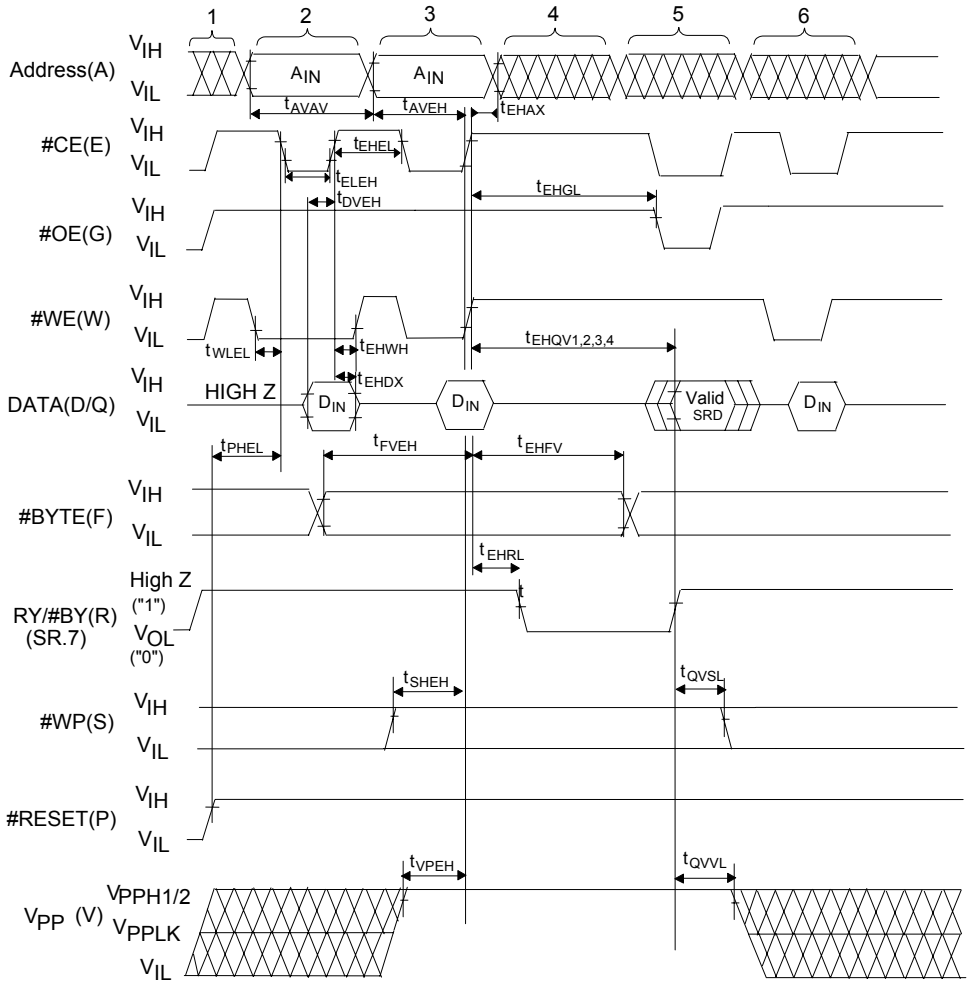


Figure 19. AC Waveform for #CE-Controlled Write Operations

Notes:

1. V_{DD} power-up and standby.
2. Write each setup command.
3. Write each confirm command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.

Reset Operations

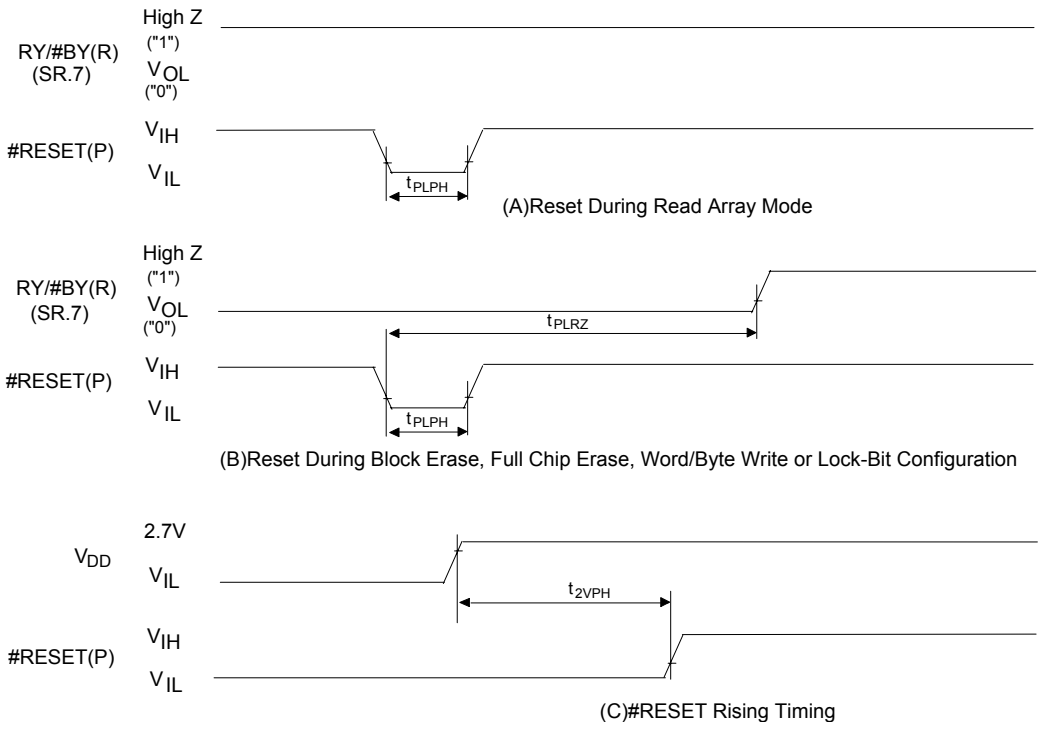


Figure 20. AC Waveform for Reset Operation

Reset AC Specifications

PARAMETER	SYM.	MIN.	MAX.	UNIT
#RESET Pulse Low Time (note 2)	t_{PLPH}	100		nS
#RESET Low to Reset during Block Erase, Full Chip Erase, Word/Byte Write or Lock-Bit Configuration (note 1, 2)	t_{PLRZ}		30	µS
V_{DD} 2.7V to #RESET High (note 2, 3)	t_{2VPH}	100		nS

Notes:

1. If #RESET is asserted while a block erase, full chip erase, word/byte write or lock-bit configuration operation is not executing, the reset will complete within 100ns.
2. A reset time, t_{PHQV}, is required from the later of RY/#BY(SR.7) going High Z("1") or #RESET going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for t_{PHQV}.
3. When the device power-up, holding #RESET low minimum 100ns is required after V_{DD} has been in predefined range and also has been in stable there.

Block Erase, Full Chip Erase, Word/Byte Write And Lock-Bit Configuration Performance(3)

V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C

SYM.	PARAMETER		NOTE	V_{PP} = 2.7V – 3.6V			V_{PP} = 11.7V – 12.3V			UNIT
				Min.	Typ.(1)	Max.	Min.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word Write Time	32K word Block	2		33	200		20		µS
		4K word Block	2		36	200		27		µS
	Byte Write Time	64K byte Block	2		31	200		19		µS
		8K byte Block	2		32	200		26		µS
	Block Write Time (In word mode)	32K word Block	2		1.1	4		0.66		S
		4K word Block	2		0.15	0.5		0.12		S
	Block Write Time (In byte mode)	64K byte Block	2		2.2	7		1.4		S
		8K byte Block	2		0.3	1		0.25		S
t_{WHQV2} t_{EHQV2}	Block Erase Time	32K word Block 64K byte Block	2		1.2	6		0.9		S
		4K word Block 8K byte Block	2		0.6	5		0.5		S
	Full Chip Erase Time		2		84	420		64		S
t_{WHQV3} t_{EHQV3}	Set Lock-Bit Time		2		56	200		42		µS
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time		2		1	5		0.69		S
t_{WHRZ1} t_{EHRZ1}	Word/Byte Write Suspend Latency Time to Read		4		6	15		6	15	µS
t_{WHRZ2} t_{EHRZ2}	Block Erase Suspend Latency Time to Read		4		16	30		16	30	µS
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command		5	600			600			µS

Notes:

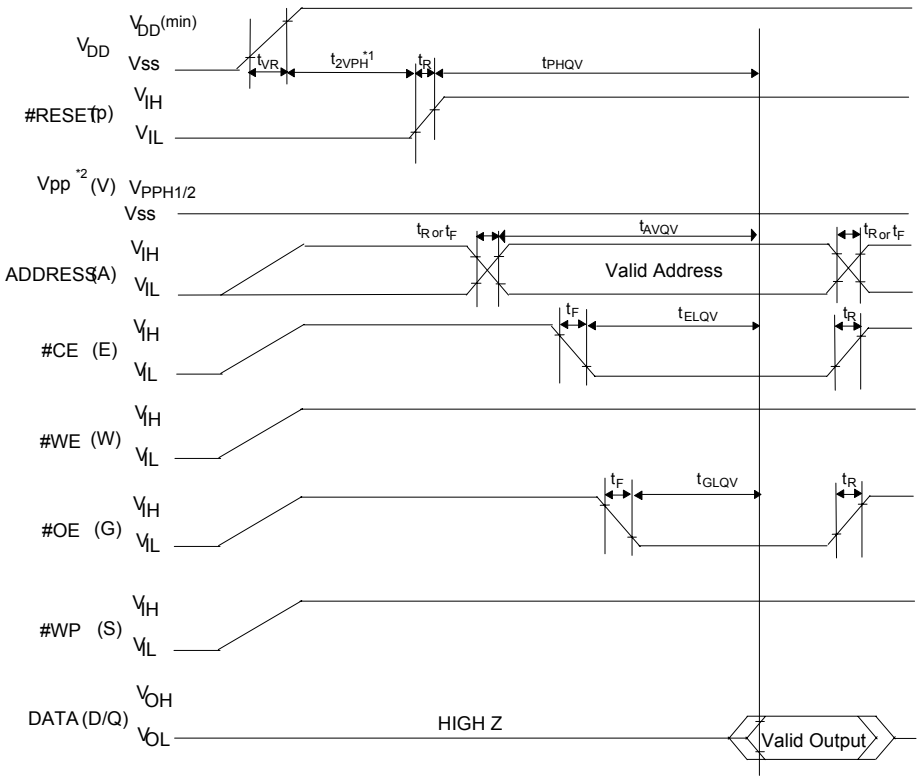
1. Typical values measured at T_A = +25° C and V_{DD} = 3.0V, V_{PP} = 3.0V or 12.0V. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. Sampled but not 100% tested.
4. A latency time is required from issuing suspend command (#WE or #CE going high) until RY/#BY going High Z or SR.7 going "1".
5. If the time between writing the Block Erase Resume command and writing the Block Erase Suspend command is shorter than t_{ERES} and both commands are written repeatedly, a longer time is required than standard block erase until the completion of the operation.

12. ADDITIONAL INFORMATION

Recommended Operating Conditions

At Device Power-Up

AC timing illustrated in Figure 21 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 t_{5VPH} for the device in 5V operations.

*2 To prevent the unwanted writes, system designers should consider the V_{PP} switch, which connects V_{PP} to V_{SS} during read operations and $V_{PPH1/2}$ during write or erase operations.

Figure 21. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

Rise and Fall Time

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
V_{DD} Rise Time (note 1)	t_{VR}	0.5	30000	μS V
Input SignalRise Time (note 1, 2)	t_R		1	μS/ V
Input SignalFall Time (note 1, 2)	t_F		1	μS/ V

Notes:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations. t_R(Max.) and t_F(Max.) for #RESET are 50 μS/V

Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure 22 (b). The acceptable glitch noises are illustrated in Figure 22 (a).

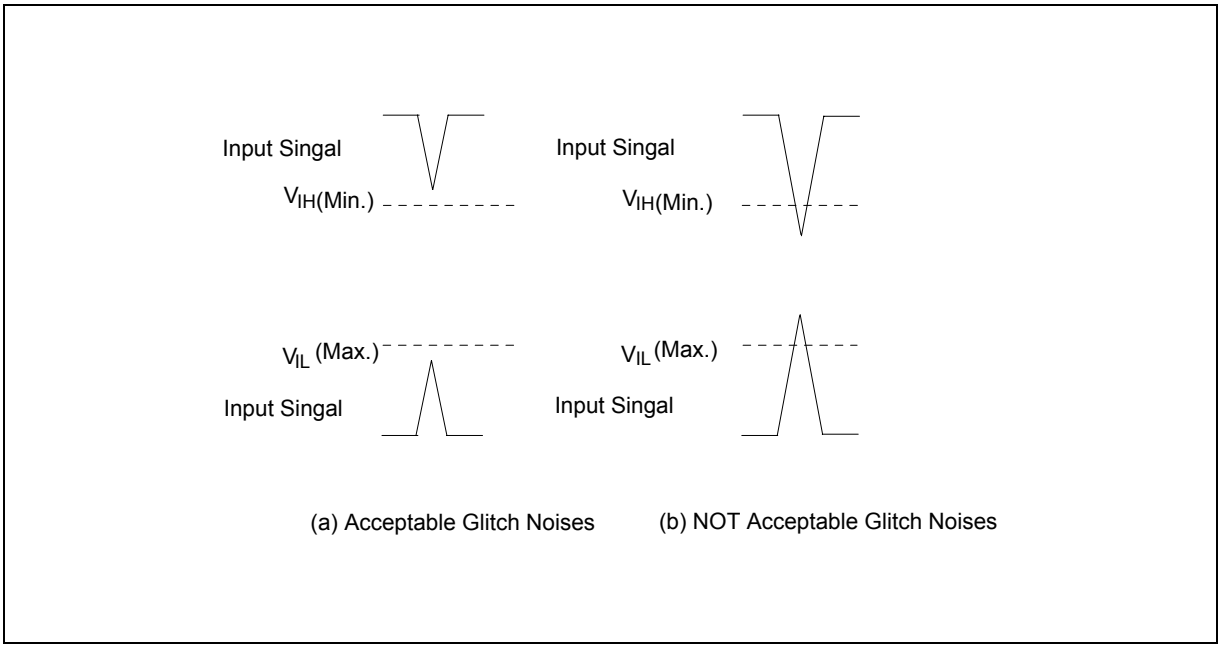


Figure 22. Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

13. ORDERING INFORMATION

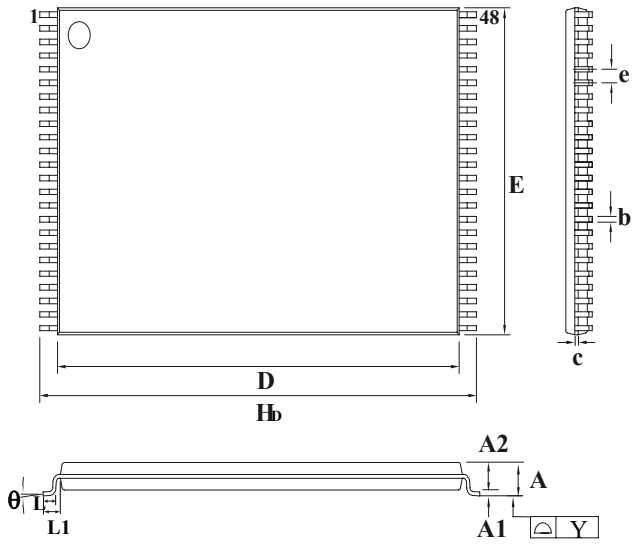
PART NO.	ACCESS TIME (nS)	OPERATING TEMPERATURE (°C)	BOOT BLOCK	PACKAGE
W28J320BT90L	90	-40° C to 85° C	Bottom Boot	48L TSOP
W28J320TT90L	90	-40° C to 85° C	Top Boot	48L TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

14. PACKAGE DIMENSION

48-Lead Standard Thin Small Outline Package (measured in millimeters)



Sym.	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
H_D	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 12, 2002	-	Initial Issued
A2	Aug. 6, 2002	All	Update description and correct typo
A3	Nov. 18, 2002	45	Correct the typo in Figure 21
A4	Apr. 11, 2003	All	Update description and correct typo

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