



CYPRESS

W152

Spread Aware™, Eight Output Zero Delay Buffer

Features

- Spread Aware™—designed to work with SSFTG reference signals
- Two banks of four outputs each
- Configuration options to halve, double, or quadruple the reference frequency refer to *Table 1* to determine the specific option which meets your multiplication needs
- Outputs may be three-stated
- Available in 16-pin SOIC package
- Extra strength output drive available (-11/-12 versions)
- Contact factory for availability information on 16-pin TSSOP

Key Specifications

Operating Voltage: 3.3V±10%
 Operating Range: 15 MHz < f_{OUTQA} < 140 MHz
 Cycle-to-Cycle Jitter: (Refer to *Figure 3*) 175 ps
 Cycle-to-Cycle Jitter: Frequency Range
 25 to 140 MHz 150 ps

Output to Output Skew: Between Banks 200 ps
 Output to Output Skew: Within Banks
 (Refer to *Figure 4*) 100ps
 Total Timing Budget Impact: 355 ps
 Max. Phase Error Variation: ±225 ps
 Tracking Skew: ±130 ps

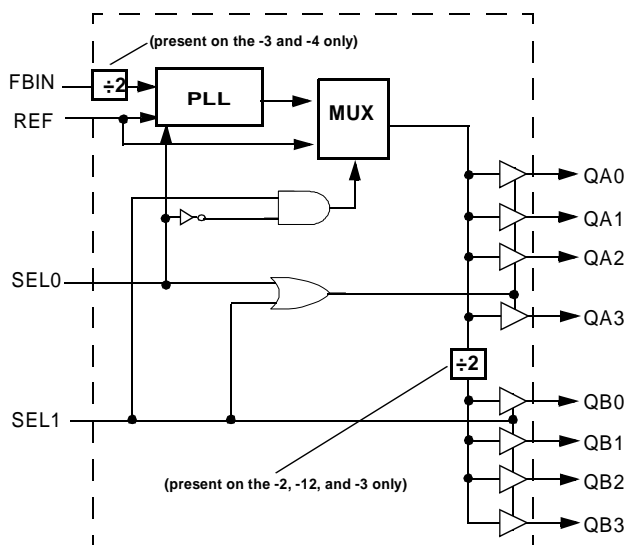
Table 1. Configuration Options

| Device | Feedback Signal | QA0:3 | QB0:3 |
|--------------------------|-----------------|-------|-------|
| W152-1/11 ^[1] | QA0:3 or QB0:3 | REFx1 | REFx1 |
| W152-2/12 ^[2] | QA0:3 | REFx1 | REF/2 |
| W152-2/12 ^[2] | QB0:3 | REFx2 | REFx1 |
| W152-3 | QA0:3 | REFx2 | REFx1 |
| W152-3 | QB0:3 | REFx4 | REFx2 |
| W152-4 | QA0:3 or QB0:3 | REFx2 | REFx2 |

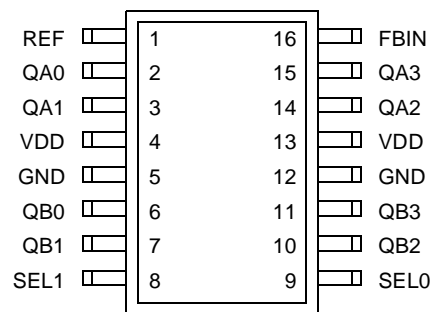
Notes:

1. W152-11 has stronger output drive than the W152-1.
2. W152-12 has stronger output drive than the W152-2.

Block Diagram



Pin Configuration



Spread Aware is a trademark of Cypress Semiconductor Corporation.

Pin Definitions

| Pin Name | Pin No. | Pin Type | Pin Description |
|----------|--------------|----------|--|
| REF | 1 | I | Reference Input: The output signals QA0:3 through QB0:3 will be synchronized to this signal unless the device is programmed to bypass the PLL. |
| FBIN | 16 | I | Feedback Input: When programmed to zero delay buffer mode, this input must be fed by one of the outputs (QA0:3 or QB0:3) to ensure proper functionality. If the trace between FBIN and the output pin being used for feedback is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the REF signal input. |
| QA0:3 | 2, 3, 14, 15 | O | Outputs from Bank A: The frequency of the signals provided by these pins is determined by the feedback signal connected to FBIN, and the specific W152 option being used. See <i>Table 2</i> . |
| QB0:3 | 6, 7, 10, 11 | O | Outputs from Bank B: The frequency of the signals provided by these pins is determined by the feedback signal connected to FBIN, and the specific W152 option being used. See <i>Table 2</i> . |
| VDD | 4, 13 | P | Power Connections: Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance. |
| GND | 5, 12 | G | Ground Connections: Connect all grounds to the common system ground plane. |
| SEL0:1 | 9, 8 | I | Function Select Inputs: Tie to V _{DD} (HIGH, 1) or GND (LOW, 0) as desired per <i>Table 2</i> . |

Overview

The W152 products are eight-output zero delay buffers. A Phase-Locked Loop (PLL) is used to take a time-varying signal and provide eight copies of that same signal out. The external feedback to the PLL provides outputs in phase with the reference inputs.

Internal dividers exist in some options allowing the user to get a simple multiple ($/2$, $\times 2$, $\times 4$) of the reference input, for details see *Table 1*. Because the outputs are separated into two banks, it is possible to provide some combination of these multiples at the same time.

Spread Aware

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note titled, "EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs."

Functional Description

Logic inputs provide the user the ability to turn off one or both banks of clocks when not in use, as described in *Table 2*. Disabling a bank of unused outputs will reduce jitter and power consumption, and will also reduce the amount of EMI generated by the W152.

These same inputs allow the user to bypass the PLL entirely if so desired. When this is done, the device no longer acts as a zero delay buffer, it simply reverts to a standard eight-output clock driver.

The W152 PLL enters an auto power-down mode when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off.

Table 2. Input Logic

| SEL1 | SEL0 | QA0:3 | QB0:3 | PLL |
|------|------|-------------|-------------|--------------------|
| 0 | 0 | Three-State | Three-State | Shutdown |
| 0 | 1 | Active | Three-State | Active, Utilized |
| 1 | 0 | Active | Active | Shutdown, Bypassed |
| 1 | 1 | Active | Active | Active, Utilized |

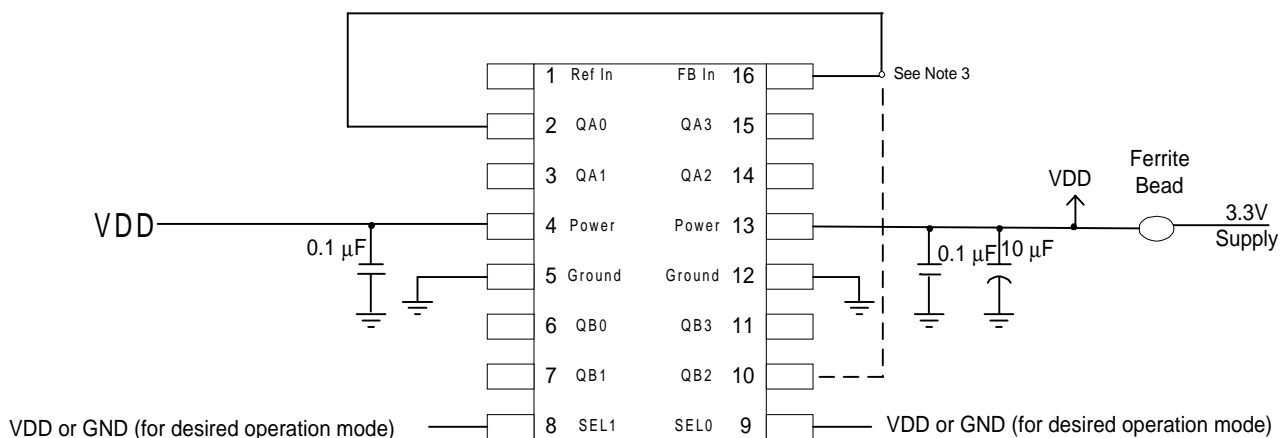


Figure 1. Schematic

Note:

- Pin 16 needs to be connected to one of the outputs from either bank A or bank B, it should not be connected to both. Pins 2 and 10 are shown here as examples. None of the outputs should be considered as preferred for the feedback path.

How to Implement Zero Delay

Typically, zero delay buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described below.

External feedback is the trait that allows for this compensation. The PLL on the ZDB will cause the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feedback and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be affected by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals up to the signal coming from

some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) which is put into the feedback path.

Referring to *Figure 2*, if the traces between the ASIC/buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device will be driven HIGH at the same time the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay in the ASIC/Buffer must be accounted for.

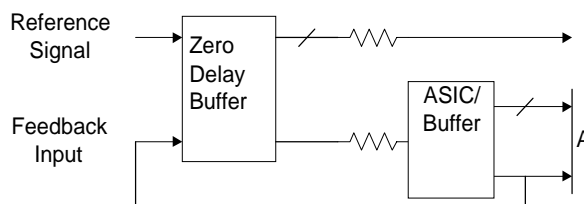


Figure 2. 6 Output Buffer in the Feedback Path

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions

above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

| Parameter | Description | Rating | Unit |
|------------------|--|--------------|------|
| V_{DD}, V_{IN} | Voltage on any pin with respect to GND | -0.5 to +7.0 | V |
| T_{STG} | Storage Temperature | -65 to +150 | °C |
| T_A | Operating Temperature | 0 to +70 | °C |
| T_B | Ambient Temperature under Bias | -55 to +125 | °C |
| P_D | Power Dissipation | 0.5 | W |

DC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to 70°C , $V_{DD} = 3.3\text{V} \pm 10\%$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|-----------|---------------------|---|------|------|------|---------------|
| I_{DD} | Supply Current | Unloaded, 100 MHz | | | 40 | mA |
| V_{IL} | Input Low Voltage | | | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 12\text{ mA} (-11, -12)$ $I_{OL} = 8\text{ mA} (-1, -2, -3, -4)$ | | | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = 12\text{ mA} (-11, -12)$ $I_{OH} = 8\text{ mA} (-1, -2, -3, -4)$ | 2.4 | | | V |
| I_{IL} | Input Low Current | $V_{IN} = 0\text{V}$ | | | 50 | μA |
| I_{IH} | Input High Current | $V_{IN} = V_{DD}$ | | | 50 | μA |

AC Electrical Characteristics: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 10\%$

| Parameter | Description | Test Condition | Min. | Typ. | Max. | Unit |
|-------------|--------------------------------------|------------------------------|------|------|------|------|
| f_{IN} | Input Frequency | Note 4 | 15 | | 140 | MHz |
| f_{OUT} | Output Frequency | 15-pF load ^[9] | 15 | | 140 | MHz |
| t_R | Output Rise Time (-1, -2, -3, -4) | 0.8V to 0.8V, 15-pF load | | 2 | 2.5 | ns |
| | Output Rise Time (-11, -12) | 0.8V to 0.8V, 15-pF load | | | 1.5 | ns |
| t_F | Output Fall Time (-1, -2, -3, -4) | 2.0V to 0.8V, 15-pF load | | 2 | 2.5 | ns |
| | Output Rise Time (-11, -12) | 2.0V to 0.8V, 20-pF load | | | 1.5 | ns |
| t_{iCLKR} | Input Clock Rise Time ^[5] | | | | 4.5 | ns |
| t_{iCLKF} | Input Clock Fall Time ^[5] | | | | 4.5 | ns |
| t_{PD} | FBIN to REF Skew ^[6, 7] | | | | 350 | ps |
| t_{SK} | Output to Output Skew | All outputs loaded equally | | | 250 | ps |
| t_D | Duty Cycle | 15-pF load ^[8, 9] | 45 | 50 | 55 | % |
| t_{LOCK} | PLL Lock Time | Power supply stable | | | 1.0 | ms |
| t_{JC} | Jitter, Cycle-to-Cycle | Note 10 | | | 200 | ps |

Notes:

- Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration). See Table 1.
- Longer input rise and fall time will degrade skew and jitter performance.
- All AC specifications are measured with a 50 Ω transmission line.
- Skew is measured at $V_{DD}/2$ on rising edges.
- Duty cycle is measured at $V_{DD}/2$.
- For the higher drive -11 and -12, the load is 20 pF.
- For frequencies above 25 MHz CY - CY = 125.

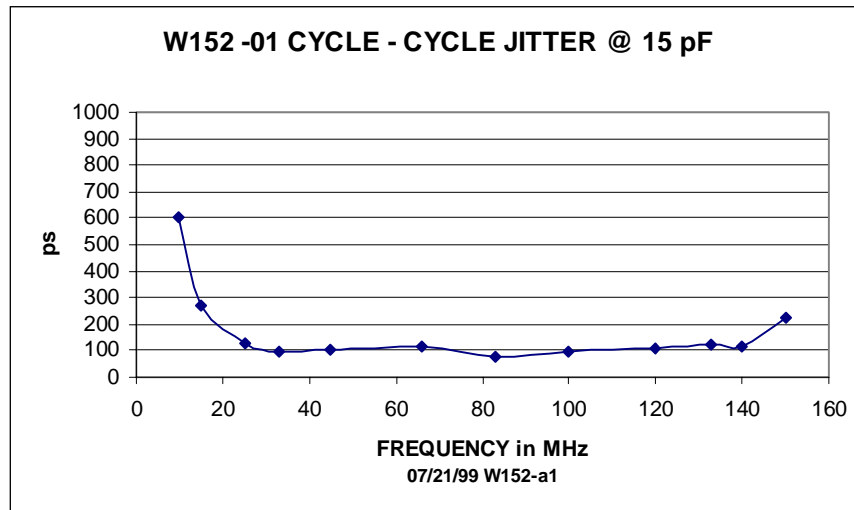


Figure 3. Cycle to Cycle Jitter at 15 pF

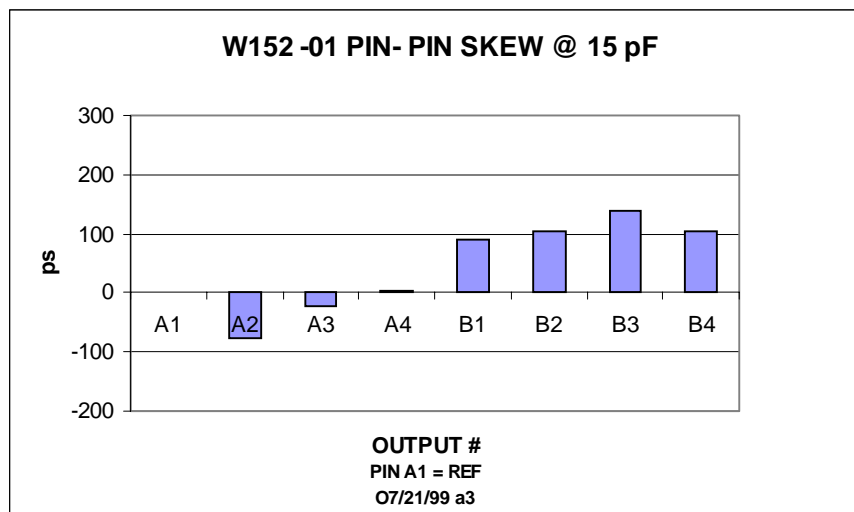
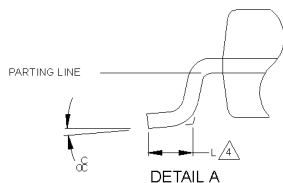
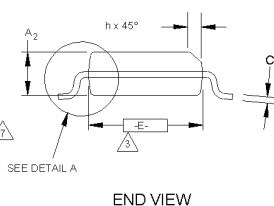
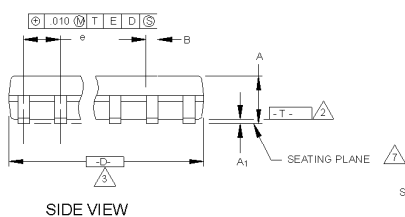
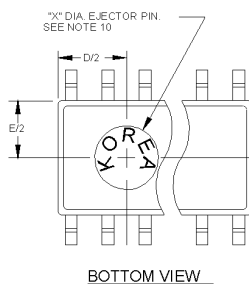
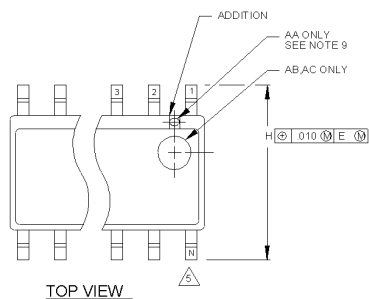


Figure 4. Pin to Pin Skew at 15 pF

Ordering Information

| Ordering Code | Option | Package Name | Package Type |
|---------------|--------------------------|--------------|--|
| W152 | -1, -11, -2, -12, -3, -4 | G X | 16-pin SOIC (150 mil) 16-pin TSSOP (4.4 mm) |

Document #: 38-00786-*A

Package Diagrams
16-Pin Small Outline Integrated Circuit (SOIC, 150 mils)

NOTES:

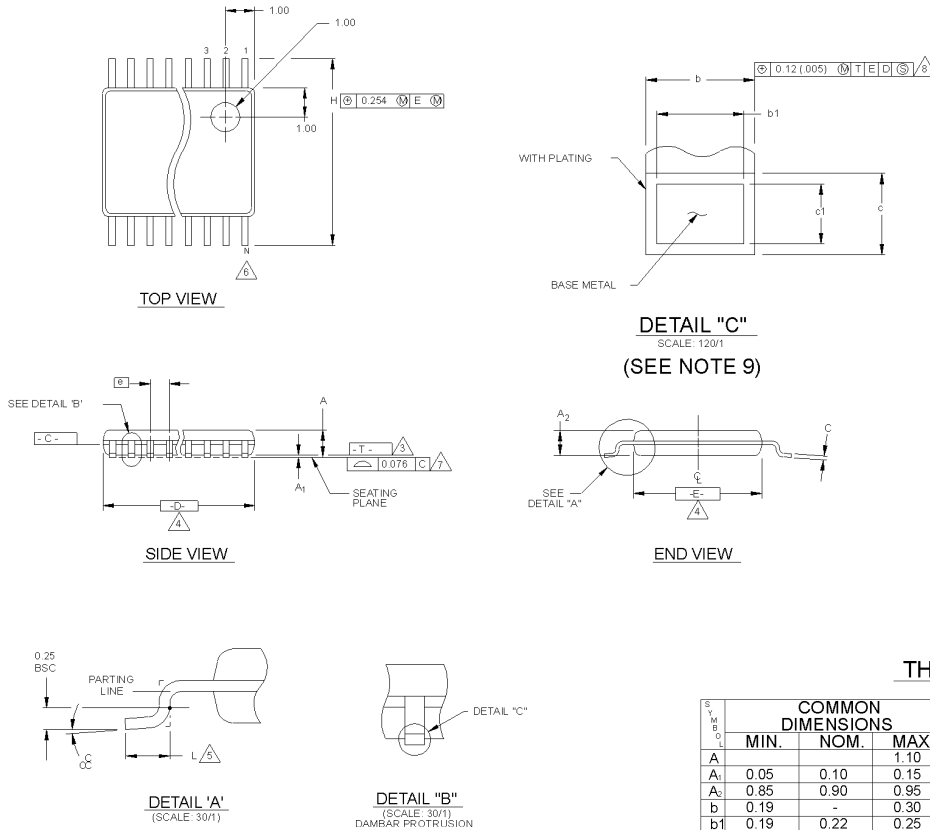
1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D. ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.
10. COUNTRY OF ORIGIN LOCATION AND EJECTOR PIN ON PACKAGE BOTTOM IS OPTIONAL AND DEPEND ON ASSEMBLY LOCATION.
11. CONTROLLING DIMENSION: INCHES.

THIS TABLE IN INCHES

| SYMBOL | COMMON DIMENSIONS | | | NOTE VARIATIONS | 3 D | | | 5 N |
|----------------|-------------------|------|-------|-----------------|------|------|------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | .061 | .064 | .068 | AA | .189 | .194 | .196 | 8 |
| A ₁ | .004 | .006 | .0098 | AB | .337 | .342 | .344 | 14 |
| A ₂ | .055 | .058 | .061 | AC | .386 | .391 | .393 | 16 |
| B | .0138 | .016 | .0192 | | | | | |
| C | .0075 | .008 | .0098 | | | | | |
| D | SEE VARIATIONS | | | 3 | | | | |
| E | .150 | .155 | .157 | | | | | |
| e | .050 BSC | | | | | | | |
| H | .230 | .236 | .244 | | | | | |
| h | .010 | .013 | .016 | | | | | |
| L | .016 | .025 | .035 | | | | | |
| N | SEE VARIATIONS | | | 5 | | | | |
| α | 0° | 5° | 8° | | | | | |
| X | .085 | .093 | .100 | | | | | |

THIS TABLE IN MILLIMETERS

| SYMBOL | COMMON DIMENSIONS | | | NOTE VARIATIONS | 3 D | | | 5 N |
|----------------|-------------------|------|------|-----------------|------|------|------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | 1.55 | 1.63 | 1.73 | AA | 4.80 | 4.93 | 4.98 | 8 |
| A ₁ | 0.127 | 0.15 | 0.25 | AB | 8.58 | 8.69 | 8.74 | 14 |
| A ₂ | 1.40 | 1.47 | 1.55 | AC | 9.80 | 9.93 | 9.98 | 16 |
| B | 0.35 | 0.41 | 0.49 | | | | | |
| C | 0.19 | 0.20 | 0.25 | | | | | |
| D | SEE VARIATIONS | | | 3 | | | | |
| E | 3.81 | 3.94 | 3.99 | | | | | |
| e | 1.27 BSC | | | | | | | |
| H | 5.84 | 5.99 | 6.20 | | | | | |
| h | 0.25 | 0.33 | 0.41 | | | | | |
| L | 0.41 | 0.64 | 0.89 | | | | | |
| N | SEE VARIATIONS | | | 5 | | | | |
| α | 0° | 5° | 8° | | | | | |
| X | 2.16 | 2.36 | 2.54 | | | | | |

Package Diagrams (continued)
16-Pin Thin Shrink Small Outline Package (TSSOP, 4.4 mm)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127 (0.110±0.005 INCHES)
2. DIMENSIONING & TOLERANCES PER ANSI Y14.5M-1982.
- ▲ "T" IS A REFERENCE DATUM.
- ▲ "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- ▲ TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
- ▲ FORMED LEADS SHALL BE FLAWER WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD TO BE 0.14mm SEE DETAILS "B" AND "C".
- ▲ DETAIL "C" TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEAD TIP.
10. CONTROLLING DIMENSION: MILLIMETERS.
11. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-153. VARIATIONS AA, AB, AC, AD AND AE.

THIS TABLE IN MILLIMETERS

| SYMBOL | COMMON DIMENSIONS | | | NOTE VARIATIONS | 4 D | | | 6 N |
|----------------|-------------------|-------|-------|-----------------|------|------|------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | | | 1.10 | AA | 2.90 | 3.00 | 3.10 | 8 |
| A ₁ | 0.05 | 0.10 | 0.15 | AB | 4.90 | 5.00 | 5.10 | 14 |
| A ₂ | 0.85 | 0.90 | 0.95 | AC | 4.90 | 5.00 | 5.10 | 16 |
| b | 0.19 | - | 0.30 | 8 AD | 6.40 | 6.50 | 6.60 | 20 |
| b ₁ | 0.19 | 0.22 | 0.25 | AE | 7.70 | 7.80 | 7.90 | 24 |
| c | 0.090 | - | 0.20 | AF | 9.60 | 9.70 | 9.80 | 28 |
| c ₁ | 0.090 | 0.127 | 0.135 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | |
| E | 4.30 | 4.40 | 4.50 | 4 | | | | |
| e | 0.65 BSC | | | | | | | |
| H | 6.25 | 6.40 | 6.50 | | | | | |
| L | 0.50 | 0.60 | 0.70 | 5 | | | | |
| N | SEE VARIATIONS | | | 6 | | | | |
| α | 0° | 4° | 8° | | | | | |

THIS TABLE IN INCHES

| SYMBOL | COMMON DIMENSIONS | | | NOTE VARIATIONS | 4 D | | | 6 N |
|----------------|-------------------|-------|-------|-----------------|------|------|------|-----|
| | MIN. | NOM. | MAX. | | MIN. | NOM. | MAX. | |
| A | | | .0433 | AA | .114 | .118 | .122 | 8 |
| A ₁ | .002 | .004 | .006 | AB | .193 | .197 | .201 | 14 |
| A ₂ | .0335 | .0354 | .0374 | AC | .193 | .197 | .201 | 16 |
| b | .0075 | - | .0118 | 8 AD | .252 | .256 | .260 | 20 |
| b ₁ | .0075 | .0087 | .0098 | AE | .303 | .307 | .311 | 24 |
| c | .0035 | - | .0079 | AF | .378 | .382 | .386 | 28 |
| c ₁ | .0035 | .0050 | .0053 | | | | | |
| D | SEE VARIATIONS | | | 4 | | | | |
| E | .169 | .173 | .177 | 4 | | | | |
| e | .0256 BSC | | | | | | | |
| H | .246 | .252 | .256 | | | | | |
| L | .020 | .024 | .028 | 5 | | | | |
| N | SEE VARIATIONS | | | 6 | | | | |
| α | 0° | 4° | 8° | | | | | |

VARIATION AF IS DESIGNED BUT NOT TOOLED