ERRATA
TO THE TSB12LV21B DATA SHEET
(TEXAS INSTRUMENTS LITERATURE NO. SLLS306, JULY 1998)

1. If posted writes are enabled, a slave access to the TSB12LV21B can be continuously retried on the PCI bus under certain unusual conditions.

Workaround:

Set the EN_POST_WR bit in the miscellaneous control register to 0.

2. $\overline{\text{ISOLATE}}$ does not work properly. When the $\overline{\text{ISOLATE}}$ pin is tied low, both bus holder isolation and 1394 Annex-J isolation are enabled.

Workaround:

If isolation is required, tie $\overline{\text{ISOLATE}}$ high and use external bus holders.

3. If the PCI bus is parked on the TSB12LV21B, it is possible that the internal master address counter will not propagate to the master address latch. Consequently, on the next PCILynx transaction on the PCI bus, the value in the master address latch is 1 less than it should be and the last quadlet of data transferred will be the same as the last quadlet of data during the previous transaction.

Workaround:

Disable the TSB12LV21B latency timer by setting its value to 0x00. This allows the maximum burst of 128 bytes.

4. If the master delays asserting $\overline{\text{IRDY}}$ when the PCILynx is being accessed as a slave device, the slave burst counter will be erroneously incremented, resulting in the wrong data being returned (i.e., the data at N + 4 is read instead of the data at N).

   This problem does not occur if the master immediately asserts $\overline{\text{IRDY}}$ when it is the transaction master.

Workaround:

None

5. When the TSB12LV21B link controller is used in conjunction with the TSB21LV03 in snoop mode, there are times when the second self-ID packet of an attached 6-port PHY is not seen. This is due to a short time interval between the concatenated packets. In snoop mode, when the end of a self-ID packet is reached, the link logic must create a dummy PHY-packet acknowledge (ACK), an end-of-packet token, and then be ready for a new packet before a new packet can be received. Because the TSB12LV21B is running from a divide-by-2 of the PHY clock, this takes longer than the time between the concatenated packets, causing it to miss the start of the second self-ID packet.

   These symptoms, i.e., missing the extended self-ID packets, may not be an issue when using the TSB12LV21B link controller with PHYs other than the TSB21LV03. For example, when used with the TSB41LV03 PHY, the second self-ID is seen because the TSB41LV03 provides more delay between the concatenated packets. This provides enough time for the link to respond with the dummy ACK and end-of-packet token and be ready for the next packet.

Workaround:

Use a 41LVxx series PHY such as the TSB41LV03 400-Mbit PHY on the snooper if you need to see concatenated self-ID packets.

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