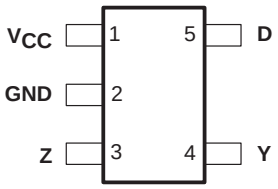
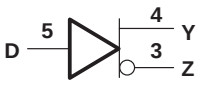
- **Meets or Exceeds ANSI TIA/EIA-644-1995 Standard**
- **Designed for Signaling Rates up to 630 Mbps**
- **Operates From a 2.4-V to 3.6-V Supply**
- **Package in Small-Outline Transistor Package**
- **Bus-Terminal ESD Exceeds 15 kV**
- **Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100-Ω Load**
- **Propagation Delay Times, 1.7 ns Typical**
- **Power Dissipation at 200 MHz, 25 mW Typical**
- **Low Voltage TTL (LVTTL) Level is 5-V Tolerant**
- **Driver is High Impedance With V_{CC} < 1.5 V**

SN65LVDS1
DBV PACKAGE
(TOP VIEW)



logic diagram



description

The SN65LVDS1 is a single low-voltage differential line driver in the small-outline transistor package. The outputs comply with the TIA/EIA-644 standard and provide a minimum differential output voltage magnitude of 247 mV into a 100-Ω load at signaling rates up to 630 Mbps.

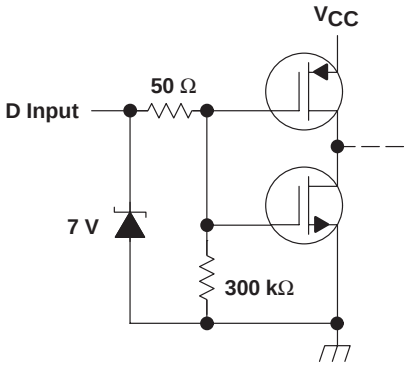
Function Table

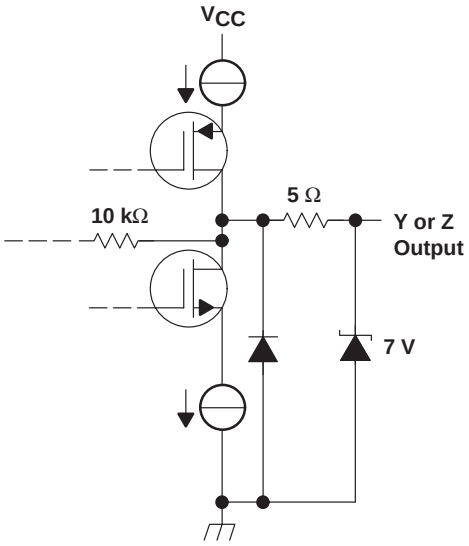
INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H
Open	L	H

When used with an LVDS receiver (such as the SN65LVDT2) in a point-to-point connection, data or clocking signals can be transmitted over printed-circuit board traces or cables at very high rates with very low electromagnetic emissions and power consumption. The packaging, low power, low EMI, high ESD tolerance, and wide supply voltage range make this device ideal for battery-powered applications.

The SN65LVDS1 is characterized for operation from –40°C to 85°C.

equivalent input and output schematic diagrams





absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 4 V
Input voltage range (D) . . . . . –0.5 V to 6 V
(Y or Z) . . . . . –0.5 V to 4 V
Electrostatic discharge: Y, Z, and GND (see Note 2) . . . . . CLass 3, A:15 kV, B:600 V
Continuous total power dissipation . . . . . See dissipation rating table
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 85°C$ POWER RATING
DBV	385 mW	3.1 mW/°C	200 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-K) and with no air flow.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.4	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	–40		85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 1	247	350	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 2	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			25	100	mV
I_{CC}	Supply current	V_I = 0 V or V_{CC}, No load		2	4	mA
		V_I = 0 V or V_{CC}, R_L = 100 Ω		5.5	8	
I_{IH}	High-level input current	V_{IH} = 5 V		2	20	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V		2	10	μA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V		3	10	mA
		V_{OD} = 0 V			10	
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0 V, V_O = 3.6 V			±1	μA
C_{IN}	Input capacitance			3		pF

† All typical values are at 25°C and with a 3.3-V.

switching characteristics over recommended operating conditions, V_{CC} = 3 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 3		1.5	2.7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.8	2.7	ns
t_r	Differential output signal rise time			0.6	1	ns
t_f	Differential output signal fall time			0.7	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)‡			0.3		ns

† All typical values are at 25°C and with a 3.3-V.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

switching characteristics over recommended operating conditions, V_{CC} = 2.4 to 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 3		1.7	3.1	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2	3.1	ns
t_r	Differential output signal rise time			0.6	1	ns
t_f	Differential output signal fall time			0.7	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)‡			0.3		ns

† All typical values are at 25°C and with a 2.7-V.
‡ $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

PARAMETER MEASUREMENT INFORMATION

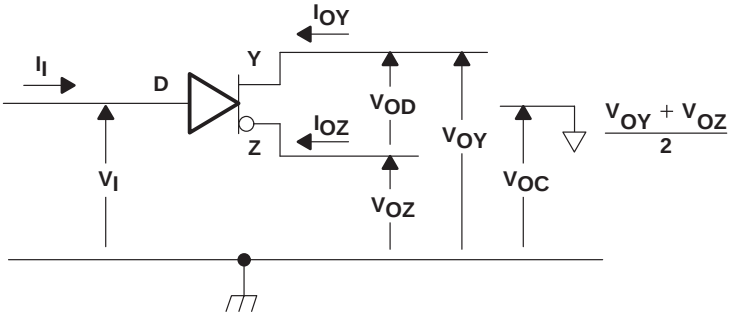
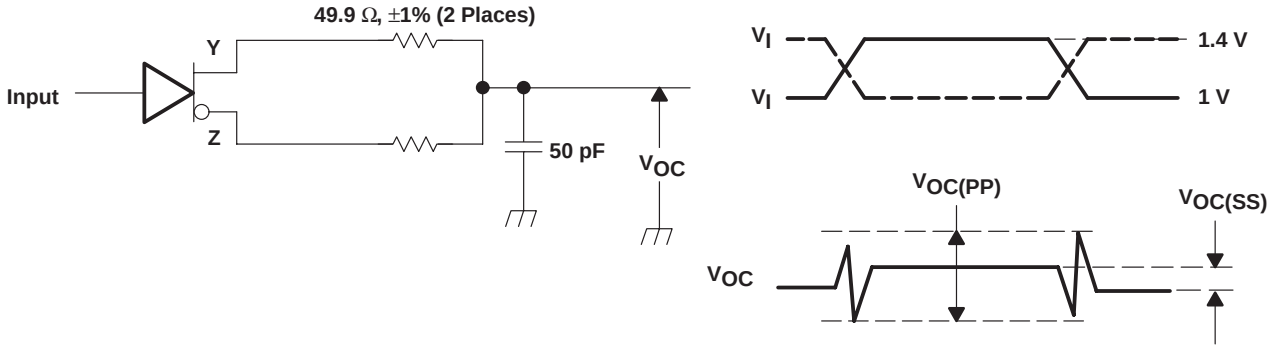


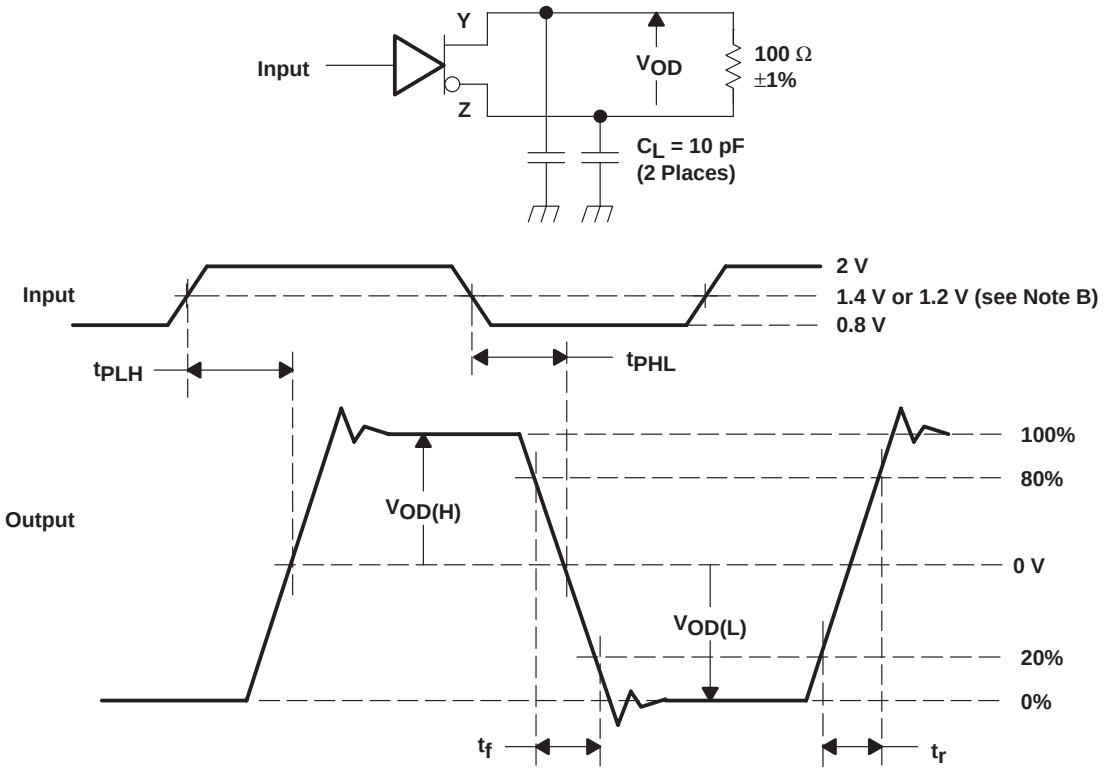
Figure 1. Driver Voltage and Current Definitions



NOTE A: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 2. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.
B. This point is 1.4 V with V_{CC} = 3.3 V or 1.2 V with V_{CC} = 2.7 V

Figure 3. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

TYPICAL CHARACTERISTICS

HIGH-TO-LOW LEVEL PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

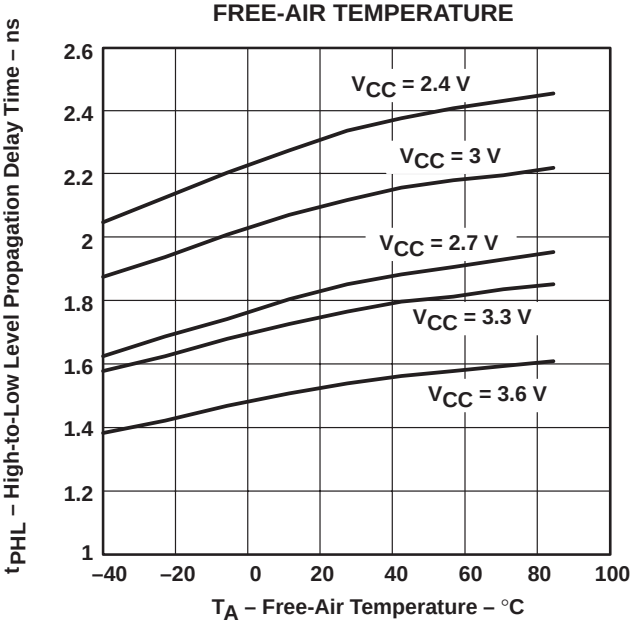


Figure 4

LOW-TO-HIGH LEVEL PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

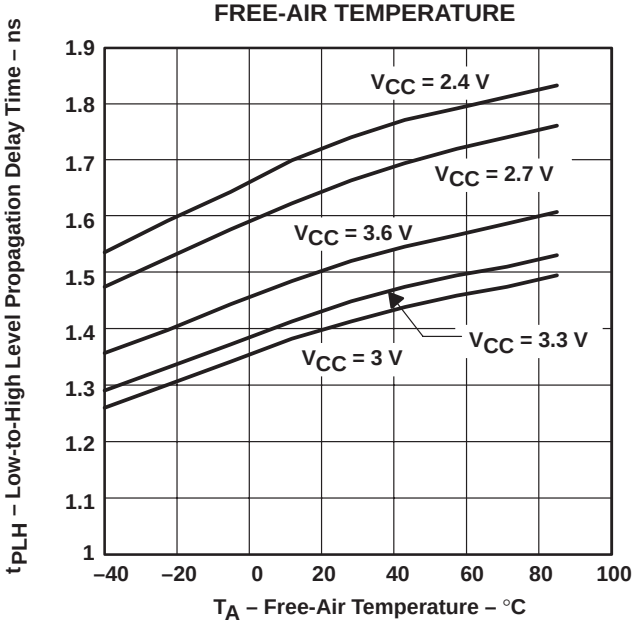
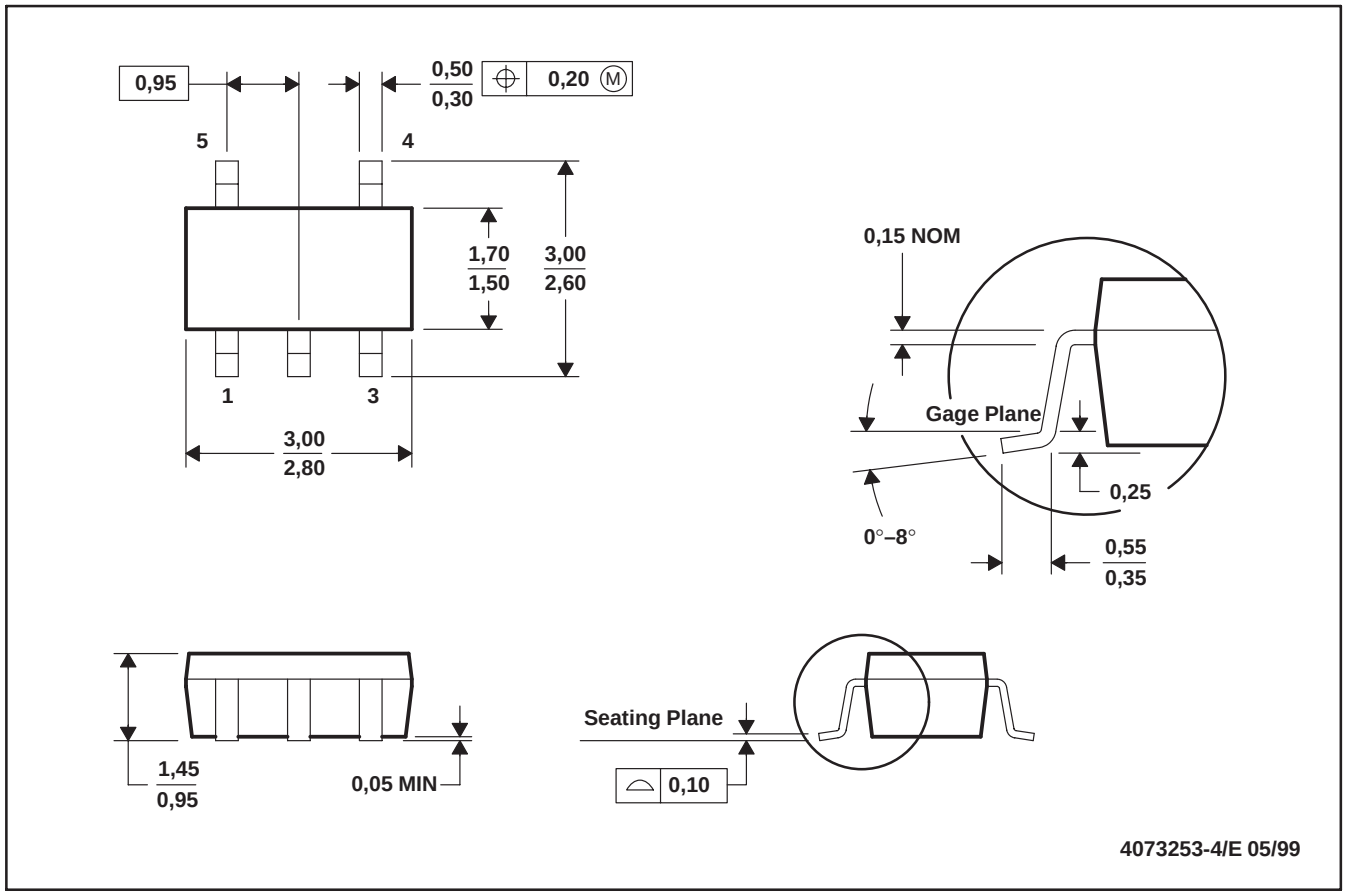


Figure 5

MECHANICAL INFORMATION

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

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