SN74AS305
OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

- **Maximum Output Skew of 1 ns**

- **Maximum Pulse Skew of 1 ns**

- **Center Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**

- **Package Options Include Plastic "Small Outline" Packages and Standard Plastic 300-mil DIPs**

description

The SN74AS305 contains eight flip-flops designed to have low skew between outputs. The eight outputs (four in-phase with CLK and four out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the CLK pin.

The SN74AS305 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to guarantee performance as a clock driver when a divide-by-two function is required.
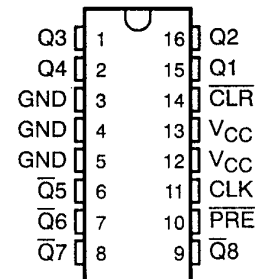
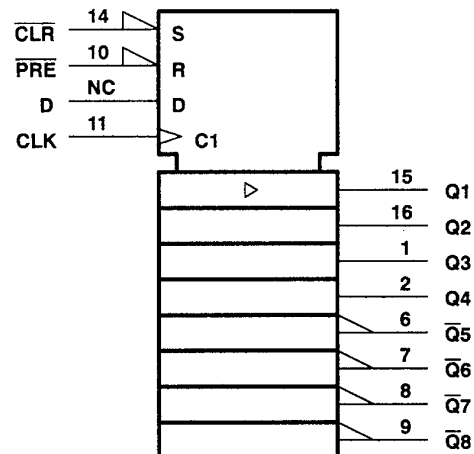The SN74AS305 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1-Q4	$\overline{Q5}$-$\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L†	L†
H	H	L	Q_0	$\overline{Q}_0$
H	H	↑	$\overline{Q}_0$	Q_0

† This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

D OR N PACKAGE
(TOP VIEW)

```
        _____
Q3 [  1      16  ] Q2
Q4 [  2      15  ] Q1
GND[  3      14  ] CLR
GND[  4      13  ] Vcc
GND[  5      12  ] Vcc
Q5 [  6      11  ] CLK
Q6 [  7      10  ] PRE
Q7 [  8       9  ] Q8
        _____
```

logic symbol‡

‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Copyright © 1990, Texas Instruments Incorporated

TEXAS
INSTRUMENTS

OCTAL DIVIDE-BY-2 CIRCUIT/CLOCK DRIVER

logic diagram (positive logic)
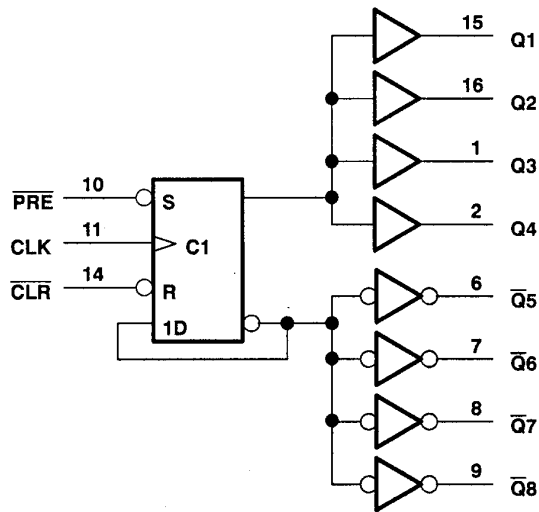
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			− 24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			-1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V,	$I_{OH} = -24$ mA	2	2.8		
V_{OL}	$V_{CC} = 4.5$ V,	$I_{OL} = 48$ mA		0.3	0.5	V
I_I	$V_{CC} = 5.5$ V,	$V_I = 7.0$ V			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			-0.5	mA
I_O‡	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	-50		-150	mA
I_{CC}	$V_{CC} = 5.5$ V,	See Note 1		40	70	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true shorst-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

| PARAMETER			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		0		80	MHz
t_w	Pulse duration	CLK high	4			
		CLK low	6			ns
		$\overline{CLR}$ or $\overline{PRE}$ low	5			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6			ns

switching characteristics over recommended operating free-air temperature range

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}‡			$R_L = 500$ Ω, $C_L = 50$ pF, $V_{CC} = 4.5$ V to 5.5 V	80			MHz
t_{PLH}	CLK	$Q, \overline{Q}$		2	6	9	ns
t_{PHL}				2	6	9	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	$Q, \overline{Q}$		3	7	12	ns
t_{PHL}				3	7	12	
$t_{sk(O)}$	CLK	$Q, \overline{Q}$	$R_L = 500$ Ω, $C_L = 10$-30 pF, $V_{CC} = 4.5$ V to 5.5 V			1	ns
	CLK	Q1 thru $\overline{Q8}$				1.5	
$t_{sk(p)}$	CLK	Q1, $\overline{Q8}$				1.5	ns
	CLK	Q2 thru $\overline{Q7}$				2	
t_r						4.5	ns
t_f						3.5	ns

‡ f_{max} minimum values are at $C_L = 0$ to 30 pF.
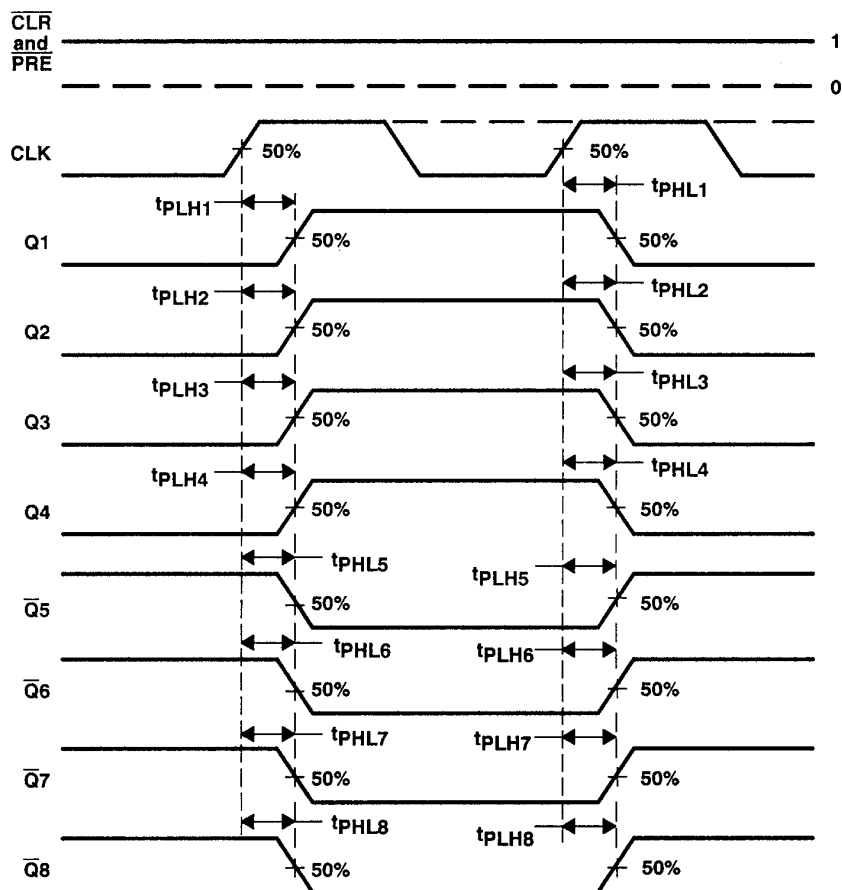
TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION
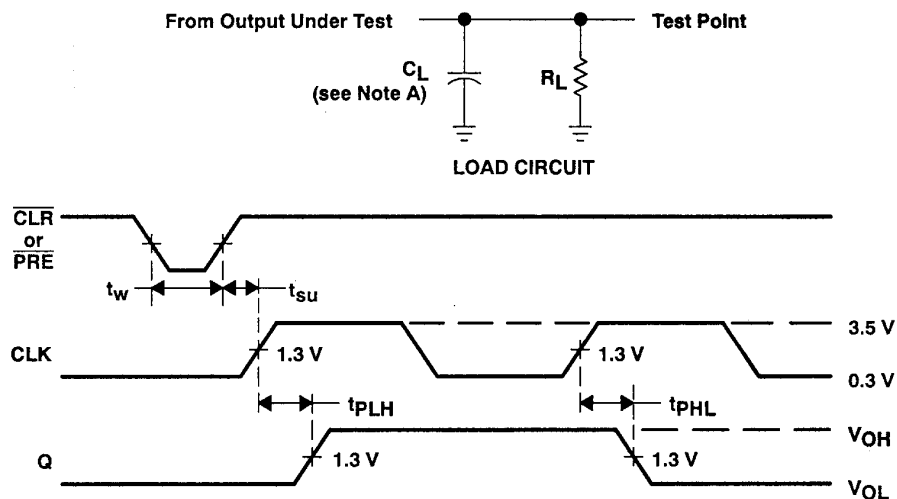
LOAD CIRCUIT

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.

Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. $t_{sk(o)}$ CLK to Q are calculated as the greater of:
1) The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4),
2) the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4).

B. $t_{sk(o)}$ CLK to $\overline{Q}$ are calculated as the greater of: 1) The difference between the fastest and slowest of t_{PLHn} (n = 5, 6, 7, 8), and 2) The difference between the fastest and slowest of t_{PHLn} (n = 5, 6, 7, 8).

C. $t_{sk(o)}$ CLK to Q and $\overline{Q}$ are calculated as the greater of:
1) The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4), t_{PHLn} (n = 5, 6, 7, 8) and
2) the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4), t_{PLHn} (n = 5, 6, 7, 8).

D. $t_{sk(p)}$ is calculated as the greater of $| t_{PLHn} - t_{PHLn} |$ (n = 1, 2, 3, . . . , 8).

Figure 2. Waveforms for Calculation of t_{sk}

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.