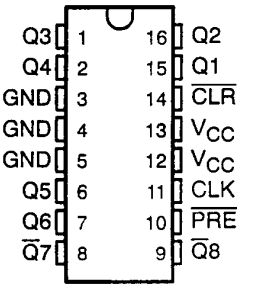
SN74AS303
OCTAL DIVIDE-BY-2 CIRCUITS/CLOCK DRIVERS

D3543, JULY 1990

- **Maximum Output Skew of 1 ns**
- **Maximum Pulse Skew of 1 ns**
- **Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN74AS303 . . . D† OR N PACKAGE
(TOP VIEW)



† Contact factory for information on availability of S.O. package.

description

The SN74AS303 contains eight flip-flops designed to have low skew between outputs. The eight outputs (six in-phase with CLK and two out-of-phase) toggle on successive CLK pulses. $\overline{PRE}$ and $\overline{CLR}$ inputs are provided to set the Q and $\overline{Q}$ outputs high or low independent of the CLK pin.

The 'AS303 has output and pulse skew parameters $t_{sk(o)}$ and $t_{sk(p)}$ to ensure performance as a clock driver when a divide-by-two function is required.

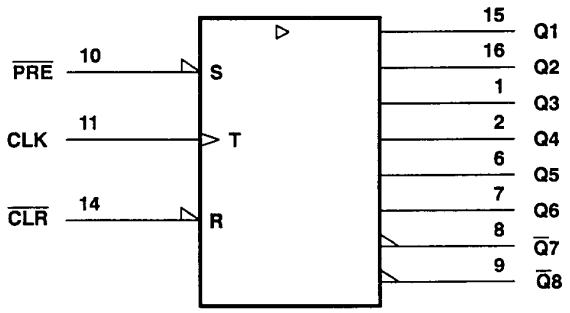
The SN74AS303 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	CLK	Q1–Q6	$\overline{Q7}$–$\overline{Q8}$
L	H	X	L	H
H	L	X	H	L
L	L	X	L‡	L‡
H	H	↑	$\overline{Q}_0$	Q_0
H	H	L	Q_0	$\overline{Q}_0$

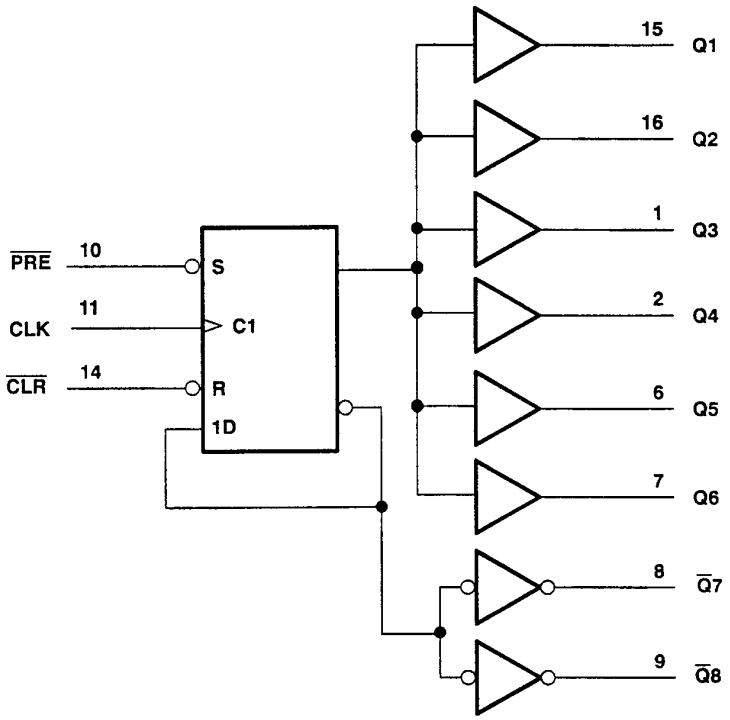
‡ This configuration will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic symbol§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = – 2 mA	V_{CC}–2			V
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA	2	2.8		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	– 50		– 150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 1		40	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with CLK and $\overline{PRE}$ grounded, then with CLK and $\overline{CLR}$ grounded.

timing requirements

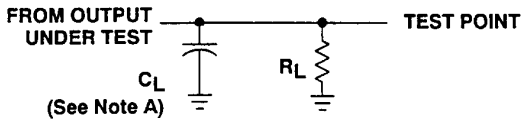
PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	80	MHz
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5		ns
		CLK high	4		
		CLK low	6		
t_{su}	Setup time before CLK↑	$\overline{CLR}$ or $\overline{PRE}$ inactive	6		ns

switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
f_{max}§				80		MHz
t_{PLH}	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	2	9	ns
t_{PHL}				2	9	ns
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 50 pF	3	12	ns
t_{PHL}				3	12	ns
$t_{sk(o)}$	CLK	Q	R_L = 500 Ω, C_L = 10 pF to 30 pF		1	ns
		$\overline{Q}$			1	
		Q, $\overline{Q}$			2	
$t_{sk(p)}$	CLK	Q, $\overline{Q}$	R_L = 500 Ω, C_L = 10 pF to 30 pF		1	ns
t_r					4.5	ns
t_f					3.5	ns

§ f_{max} minimum values are at C_L = 0 to 30 pF.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

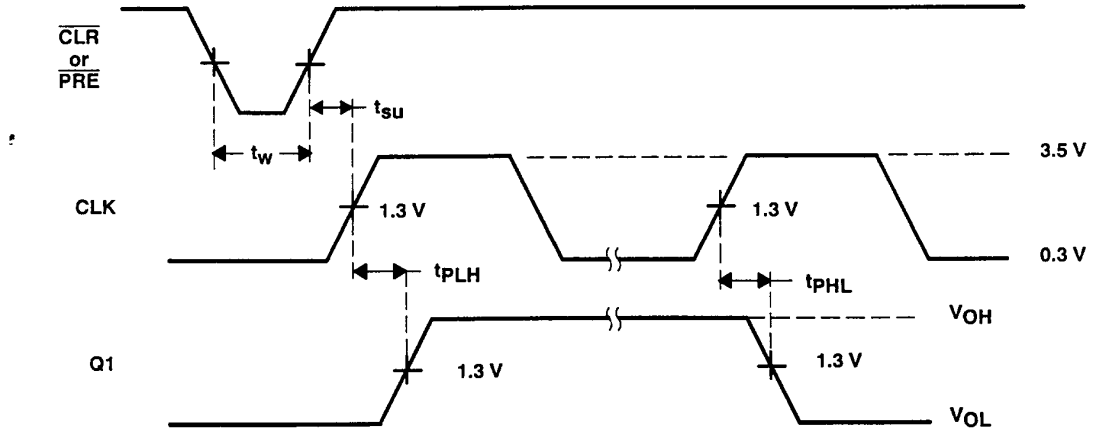
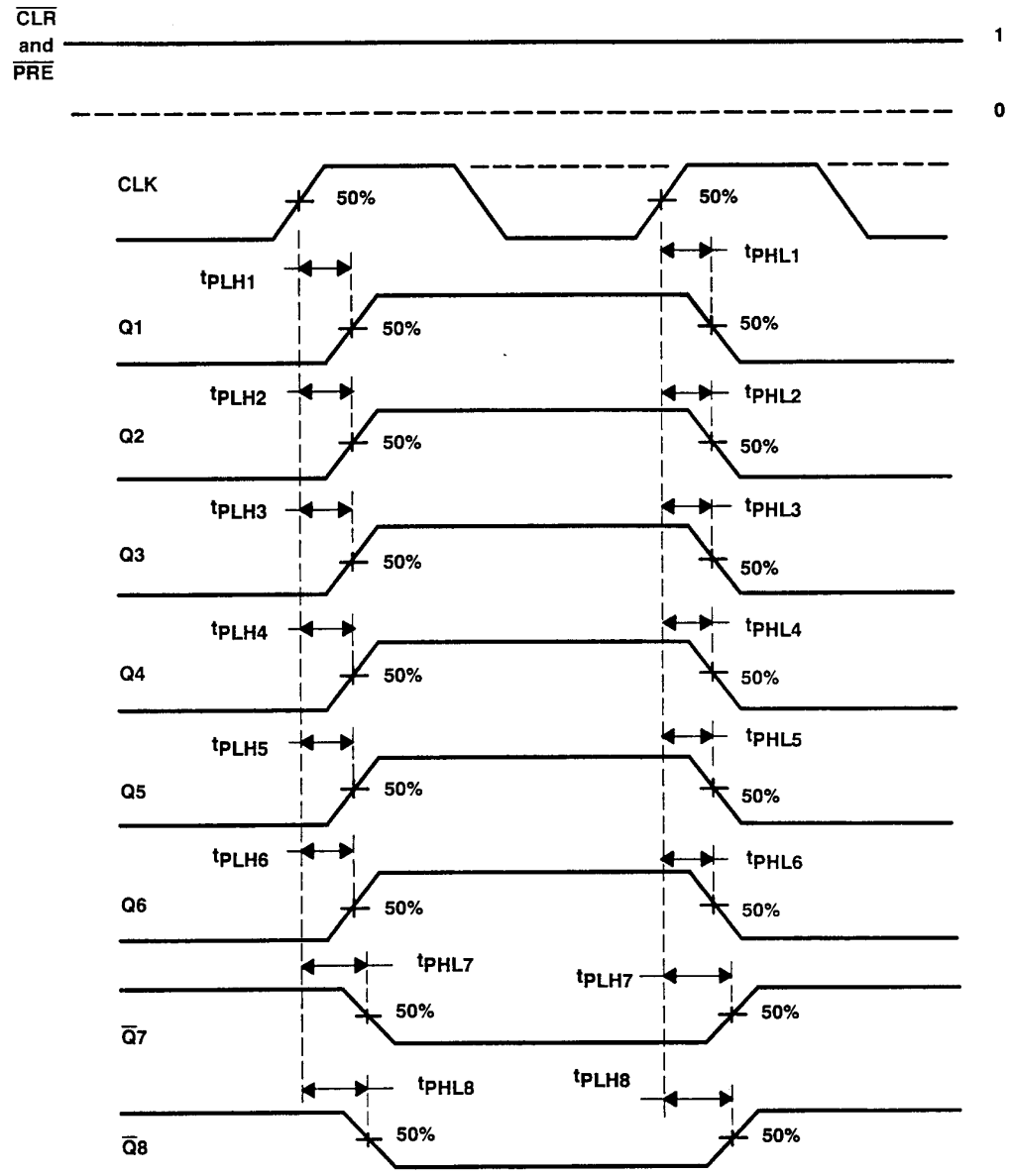


Figure 1. Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, t_r = 2.5 ns, t_f = 2.5 ns.



NOTES: A. $t_{sk(o)}$, CLK to Q, is calculated as the greater of:
1. The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6), and
2. the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6).

B. $t_{sk(o)}$, CLK to $\overline{Q}$, is calculated as the greater of: $|t_{PLH7} - t_{PLH8}|$ and $|t_{PHL7} - t_{PHL8}|$.

C. $t_{sk(o)}$, CLK to Q and $\overline{Q}$, is calculated as the greater of:
1. The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, 3, 4, 5, 6), t_{PHL7}, and t_{PHL8}, and
2. the difference between the fastest and slowest of t_{PHLn} (n = 1, 2, 3, 4, 5, 6), t_{PLH7}, and t_{PLH8}.

D. $t_{sk(p)}$ is calculated as the greater of $|t_{PLHn} - t_{PHLn}|$ (n = 1, 2, 3, . . ., 8).

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

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