- **EPIC™** (Enhanced-Performance Implanted **CMOS) Process**
- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- **Package Options Include Plastic** Small-Outline (DW), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

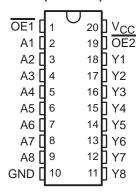
The 'AHC541 octal buffers/drivers are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

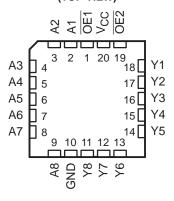
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54AHC541 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AHC541 is characterized for operation from -40°C to 85°C.

SN54AHC541 . . . J OR W PACKAGE SN74AHC541 . . . DB, DGV, DW, N, OR PW PACKAGE (TOP VIEW)



SN54AHC541 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE (each buffer/driver)

	INPUTS	ОИТРИТ	
OE1	OE2	Α	Y
L	L	L	L
L	L	Н	н
Н	X	Χ	Z
Х	Н	Χ	Z

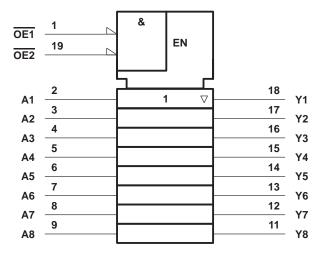


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated

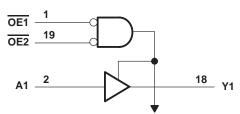


logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		0.5 V to 7 V
Input voltage range, V _I (see Note 1)		0.5 V to 7 V
Output voltage range, VO (see Note 1)		$0.5 V$ to $V_{CC} + 0.5 V$
Input clamp current, I_{IK} ($V_I < 0$)		
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CO}$		
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	·····	±25 mA
Continuous current through V _{CC} or GND		
Package thermal impedance, θ_{JA} (see Note 2):		
•	DGV package	92°C/W
	DW package	58°C/W
	N package	69°C/W
	PW package	83°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51.



recommended operating conditions (see Note 3)

			SN54A	HC541	SN74A	HC541	UNIT	
			MIN	MAX	MIN	MAX	UNIT	
Vcc	Supply voltage		2	5.5	2	5.5	V	
		V _{CC} = 2 V	1.5		1.5			
VIH	High-level input voltage	V _{CC} = 3 V	2.1		2.1		V	
		$V_{CC} = 5.5 \text{ V}$	3.85		3.85			
		V _{CC} = 2 V		0.5		0.5		
VIL	Low-level input voltage	V _{CC} = 3 V		0.9		0.9	V	
		V _{CC} = 5.5 V		1.65		1.65		
٧ı	Input voltage		0	5.5	0	5.5	V	
٧o	Output voltage		0	Vcc	0	VCC	V	
		V _{CC} = 2 V		-50		-50	μΑ	
IOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4		-4	mA	
V _{IL} V _I V _O		$V_{CC} = 5 V \pm 0.5 V$		-8		-8		
		V _{CC} = 2 V		50		50	μΑ	
lOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4		4	mA	
		$V_{CC} = 5 V \pm 0.5 V$		8		8	IIIA	
A+/A>4	Input transition rise or fell rete	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100		100	ns/V	
Δι/ΔV	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20		20	115/V	
TA	Operating free-air temperature	-	-55	125	-40	85	°C	

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	ղ = 25°C	;	SN54A	HC541	SN74AI	UNIT	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
		2 V	1.9	2		1.9		1.9		
	I _{OH} = -50 μA	3 V	2.9	3		2.9		2.9		
Voн		4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
		2 V			0.1		0.1		0.1	
	I _{OL} = 50 μA	3 V			0.1		0.1		0.1	
V _{OL}		4.5 V			0.1		0.1		0.1	V
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
lį	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1*		±1	μΑ
loz†	$V_O = V_{CC}$ or GND, $V_I (\overline{OE}) = V_{IL}$ or V_{IH}	5.5 V			±0.25		±2.5		±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	μΑ
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF
Co	$V_O = V_{CC}$ or GND	5 V		4					, and the second	pF

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0 \text{ V}$.

 $[\]ensuremath{^{\dagger}}$ For input and ouput, $\ensuremath{^{IOZ}}$ includes the input leakage current.



SN54AHC541, SN74AHC541 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS261K - DECEMBER 1995 - REVISED JANUARY 2000

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	λ = 25°C	;	SN54AI	HC541	SN74AI	HC541	UNIT	
PARAMETER	(INPUT) (OUTPUT) CAPACITANCE		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT		
t _{PLH}	А	Y	C _I = 15 pF		5*	7*	1*	8.5*	1	8.5	ns	
t _{PHL}] ^	'	CL = 13 pr		5*	7*	1*	8.5*	1	8.5	115	
^t PZH	- ŌĒ Y	C _L = 15 pF		6*	10.5*	1*	11*	1	11	ns		
tPZL		'	GL = 13 pr		6*	10.5*	1*	11*	1	11	115	
^t PHZ	ŌĒ	Y	C _L = 15 pF		7*	11*	1*	12*	1	12	ns	
tPLZ	1 OE	OE	'	CL = 13 pr		7*	11*	1*	12*	1	12	115
^t PLH	А	Υ	C ₁ = 50 pF		7.5	10.5	1	12	1	12	ns	
^t PHL	^	'	CL = 30 pi		7.5	10.5	1	12	1	12	115	
^t PZH	ŌĒ	Y	C _L = 50 pF		8	14	1	16	1	16	ns	
t _{PZL}	OE	OE	'	CL = 30 pr		8	14	1	16	1	16	115
^t PHZ	ŌĒ	Y	C _L = 50 pF		9	15.4	1	17.5	1	17.5	ns	
tPLZ			GL = 50 pr		9	15.4	1	17.5	1	17.5	115	
tsk(o)			C _L = 50 pF			1.5**				1.5	ns	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	λ = 25°C	;	SN54A	HC541	SN74AI	HC541		
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
t _{PLH}	Α	Y	C _L = 15 pF		3.5*	5*	1*	6*	1	6	ns	
t _{PHL}	A	'	CL = 15 pr		3.5*	5*	1*	6*	1	6	115	
^t PZH	OE Y	V	C _I = 15 pF		4.7*	7.2*	1*	8.5*	1	8.5	ns	
^t PZL		'	CL = 15 pr		4.7*	7.2*	1*	8.5*	1	8.5	115	
^t PHZ	<u>OE</u>	Y	C _L = 15 pF		5*	7.5*	1*	8*	1	8	ns	
^t PLZ	1 OE	OE	'	OL = 13 pi		5*	7.5*	1*	8*	1	8	115
^t PLH	Α	Y	C _L = 50 pF		5	7	1	8	1	8	ns	
^t PHL	A	'	CL = 30 pr		5	7	1	8	1	8	115	
^t PZH	<u>OE</u>	Y	C _L = 50 pF		6.2	9.2	1	10.5	1	10.5	ns	
^t PZL	OE	'	CL = 30 pr		6.2	9.2	1	10.5	1	10.5	115	
^t PHZ	ŌĒ	Y	C _I = 50 pF		6	8.8	1	10	1	10	ns	
^t PLZ		,	OL = 30 bis		6	8.8	1	10	1	10	113	
t _{sk(o)}			C _L = 50 pF			1**				1	ns	

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.



^{**} On products compliant to MIL-PRF-38535, this parameter does not apply.

^{**} On products compliant to MIL-PRF-38535, this parameter does not apply.

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

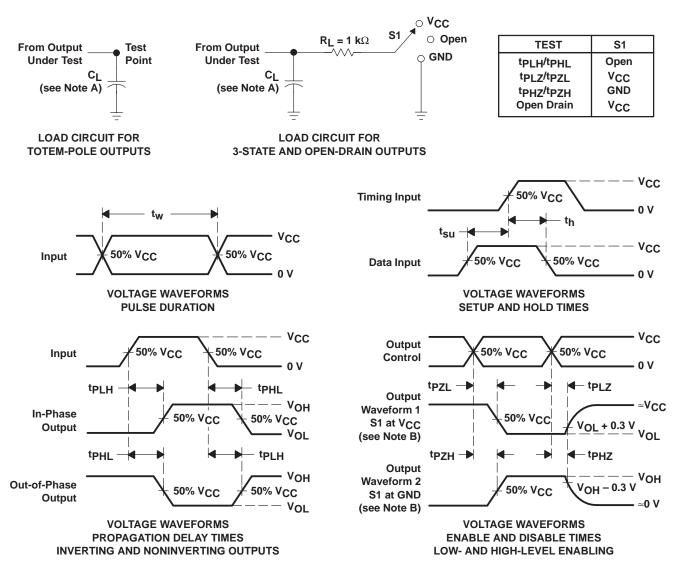
	PARAMETER SN				
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.8	V	
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}		-0.8	V	
VOH(V)	Quiet output, minimum dynamic V _{OH}	4.7		V	
VIH(D)	High-level dynamic input voltage	3.5		V	
V _{IL(D)}	Low-level dynamic input voltage		1.5	V	

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER		TEST CONDITIONS		
C _{pd}	Power dissipation capacitance	No load, f = 1	1 MHz	12	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq 3$ ns. $t_f \leq 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated