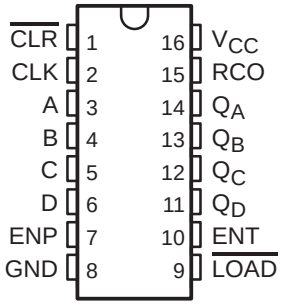
- **Synchronous Counting and Loading**
- **Two Count-Enable Inputs for n-Bit Cascading**
- **Asynchronous Reset (CD54HC160)**
- **Synchronous Reset (CD54HC162)**
- **Look-Ahead Carry for High-Speed Counting**
- **Operating Range 2-V to 6-V V_{CC}**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) Process**
- **Packaged in Ceramic (F) DIPs**

CD54HC160, CD54HC162 . . . F PACKAGE
(TOP VIEW)



description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The CD54HC160 and CD54HC162 are BCD decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with synchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, they can be preset to any number between 0 and 9. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function for the CD54HC160 is asynchronous. A low level at the clear ($\overline{CLR}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{LOAD}$), or enable inputs.

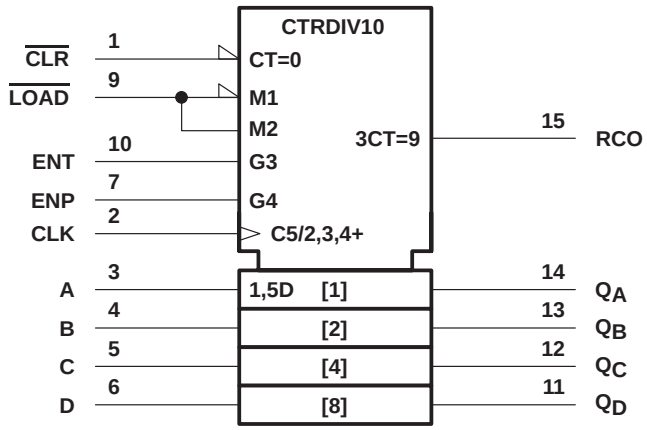
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 with Q_A high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{LOAD}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

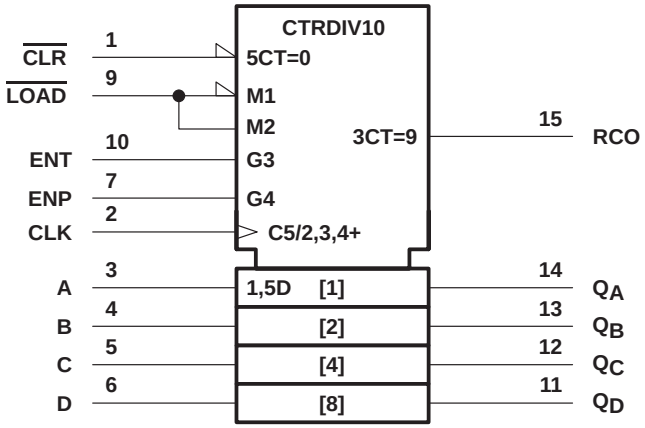
The CD54HC160 and CD54HC162 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix), and are characterized for operation over the full military temperature range of –55°C to 125°C.

logic symbol†

CD54HC160 BINARY COUNTER
WITH DIRECT CLEAR

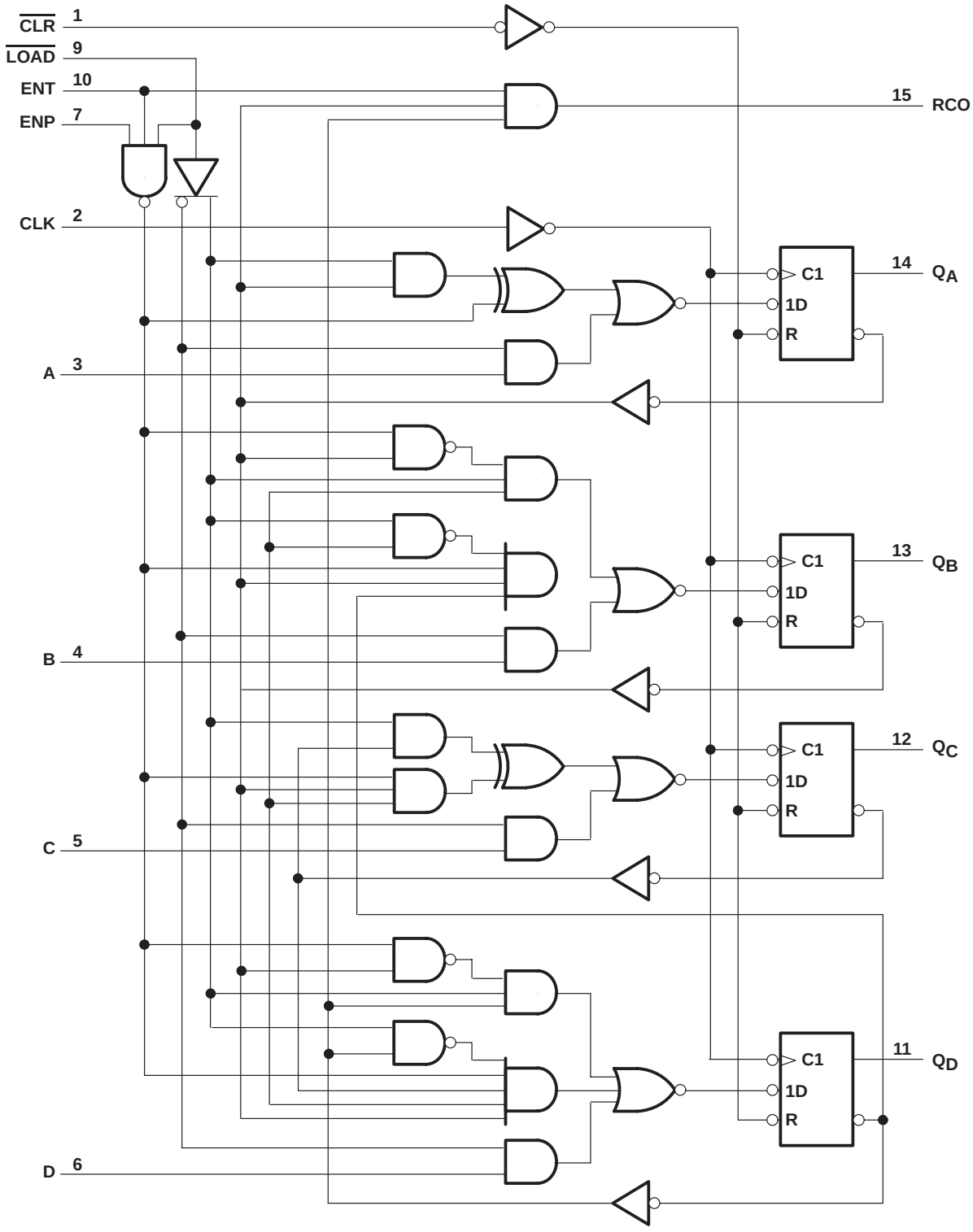


CD54HC162 BINARY COUNTER
WITH SYNCHRONOUS CLEAR



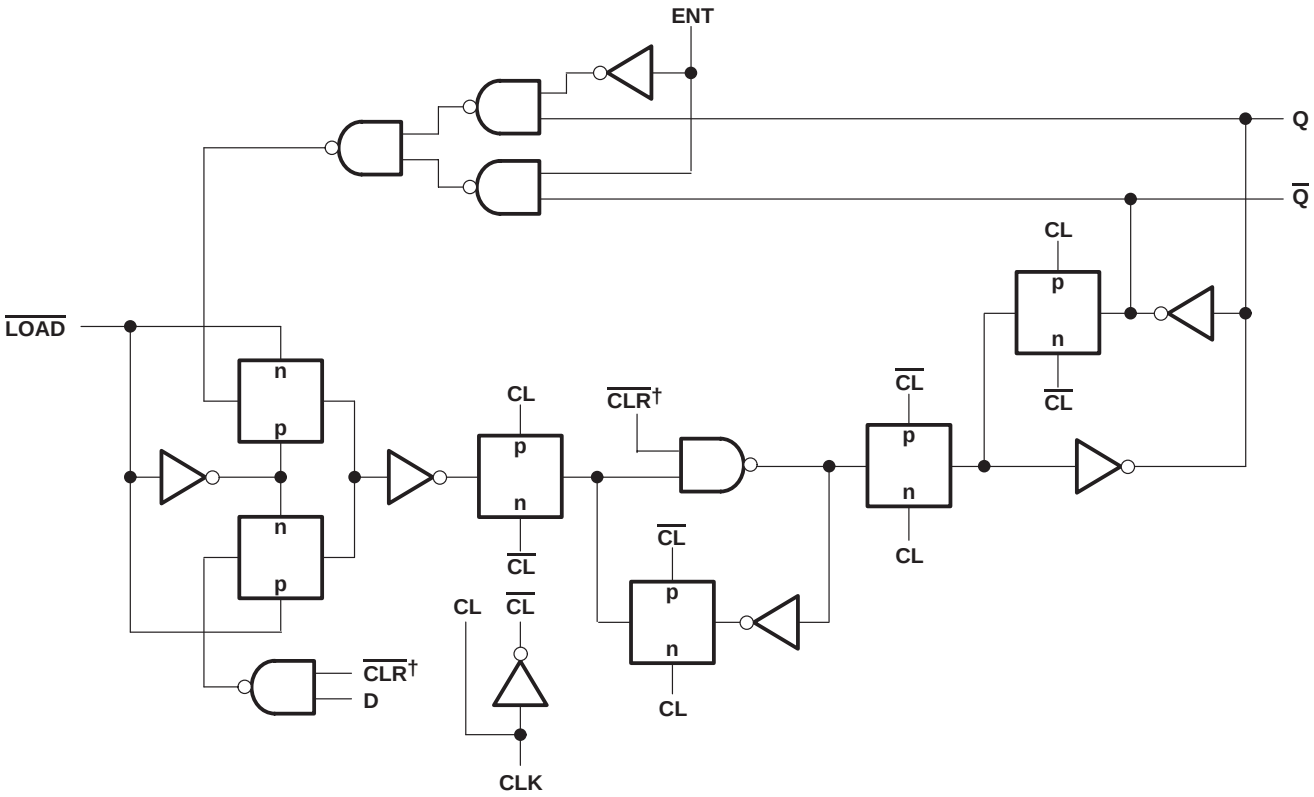
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

CD54HC160 logic diagram (positive logic)†



† CD54HC162 decade counter is similar; however, the clear is synchronous.

logic diagram, each D/T flip-flop (positive logic)

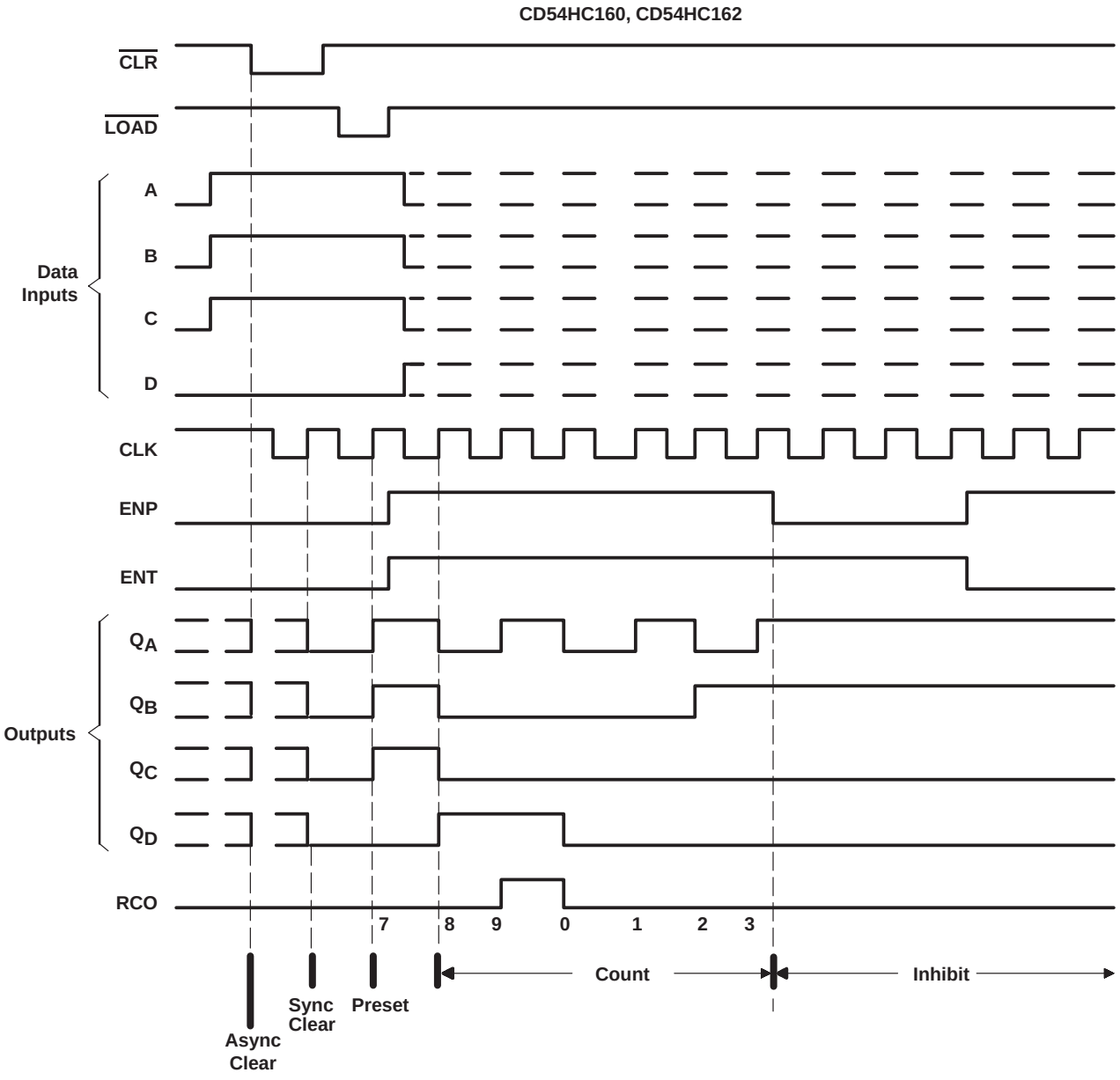


† Connect to V_{DD} for CD54HC162.

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero (CD54HC160 is asynchronous; CD54HC162 is synchronous)
2. Preset BCD to seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < –0.5 V or V_I > V_{CC} + 0.5 V) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < –0.5 V or V_O > V_{CC} + 0.5 V) . . . . . ±20 mA
Continuous output current, I_O (V_O = –0.5 V to V_{CC} + 0.5 V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Power dissipation, P_D (see Note 2) . . . . . 500 mW
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 265°C
Lead temperature, unit inserted into a PC board (minimum thickness 1,6 mm, 1/16 inch)
with solder contacting lead tips only . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 100°C, derate linearly at a factor of 8 mW/°C.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_r, t_f	Input transition rise or fall times	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		–55	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			CD54HC160 CD54HC162		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = –20 μA	2 V	1.9			1.9		V
		4.5 V	4.4			4.4		
		6 V	5.9			5.9		
	I_{OH} = –4 mA	4.5 V	3.98			3.7		
	I_{OH} = –5.2 mA	6 V	5.48			5.2		
V_{OL}	I_{OL} = 20 μA	2 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		6 V			0.1		0.1	
	I_{OL} = 4 mA	4.5 V			0.26		0.4	
	I_{OL} = 5.2 mA	6 V			0.26		0.4	
I_I	$V_I = V_{CC}$ or GND	6 V			±0.1		±1	μA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	6 V			8		160	μA
C_{IN}					10		10	pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		CD54HC160 CD54HC162		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	CLK	6		4		MHz
t_w	Pulse duration	CLK low	80		120		ns
		$\overline{CLR}$ low (’160 only)	100		150		
t_{su}	Setup time before CLK↑	Data (A, B, C, and D)	60		90		ns
		ENP, ENT	50		75		
		$\overline{LOAD}$ low	60		90		
		$\overline{CLR}$ (’162 only)	65		100		
		$\overline{CLR}$ high (’160 only)	75		110		
t_h	Hold time after CLK↑	Data (A, B, C, and D)	3		3		ns
		ENP, ENT	0		0		
		$\overline{LOAD}$ low	3		3		

timing requirements over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		CD54HC160 CD54HC162		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	CLK	30		20		MHz
t_w	Pulse duration	CLK low	16		24		ns
		$\overline{CLR}$ low (’160 only)	20		30		
t_{su}	Setup time before CLK↑	Data (A, B, C, and D)	12		18		ns
		ENP, ENT	10		15		
		$\overline{LOAD}$ low	12		18		
		$\overline{CLR}$ (’162 only)	13		20		
		$\overline{CLR}$ high (’160 only)	15		22		
t_h	Hold time after CLK↑	Data (A, B, C, and D)	3		3		ns
		ENP, ENT	0		0		
		$\overline{LOAD}$ low	3		3		

timing requirements over recommended operating free-air temperature range, V_{CC} = 6 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		CD54HC160 CD54HC162		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency	CLK	35		24		MHz
t_w	Pulse duration	CLK low	14		20		ns
		$\overline{CLR}$ low (’160 only)	17		26		
t_{su}	Setup time before CLK↑	Data (A, B, C, and D)	10		15		ns
		ENP, ENT	9		13		
		$\overline{LOAD}$ low	10		15		
		$\overline{CLR}$ (’162 only)	11		17		
		$\overline{CLR}$ high (’160 only)	13		19		
t_h	Hold time after CLK↑	Data (A, B, C, and D)	3		3		ns
		ENP, ENT	0		0		
		$\overline{LOAD}$ low	3		3		

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		CD54HC160 CD54HC162		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	CLK	RCO	C_L = 50 pF		185		280	ns
t_{PHL}					185		280	
t_{PLH}	CLK	Q	C_L = 50 pF		185		280	ns
t_{PHL}					185		280	
t_{PLH}	ENT	RCO	C_L = 50 pF		120		180	ns
t_{PHL}					120		180	
t_{PHL}	$\overline{CLR}$	Q ('160 only)	C_L = 50 pF		210		315	ns
		RCO ('160 only)			210		315	
t_{TLH}			C_L = 50 pF		75		110	ns
t_{THL}					75		110	

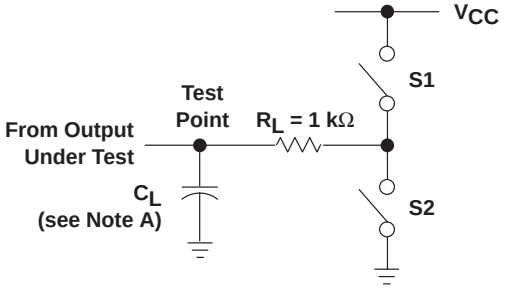
switching characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		CD54HC160 CD54HC162		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	CLK	RCO	C_L = 50 pF		37		56	ns
t_{PHL}					37		56	
t_{PLH}	CLK	Q	C_L = 50 pF		37		56	ns
t_{PHL}					37		56	
t_{PLH}	ENT	RCO	C_L = 50 pF		24		36	ns
t_{PHL}					24		36	
t_{PHL}	$\overline{CLR}$	Q ('160 only)	C_L = 50 pF		42		63	ns
		RCO ('160 only)			42		63	
t_{TLH}			C_L = 50 pF		15		22	ns
t_{THL}					15		22	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 6 V (unless otherwise noted) (see Figure 1)

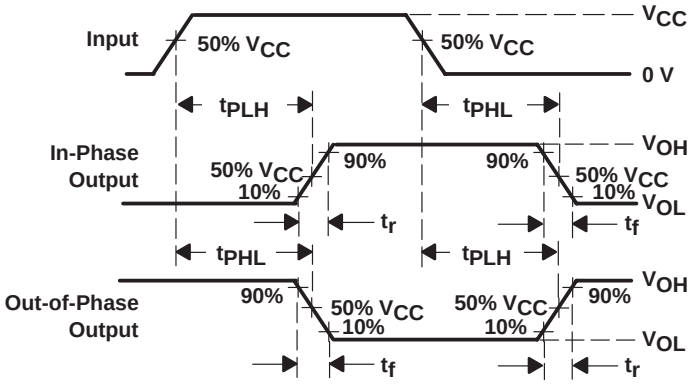
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C		CD54HC160 CD54HC162		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	CLK	RCO	C_L = 50 pF		31		48	ns
t_{PHL}					31		48	
t_{PLH}	CLK	Q	C_L = 50 pF		31		48	ns
t_{PHL}					31		48	
t_{PLH}	ENT	RCO	C_L = 50 pF		20		31	ns
t_{PHL}					20		31	
t_{PHL}	$\overline{CLR}$	Q (’160 only)	C_L = 50 pF		36		54	ns
		RCO (’160 only)			36		54	
t_{TLH}			C_L = 50 pF		13		19	ns
t_{THL}					13		19	

PARAMETER MEASUREMENT INFORMATION

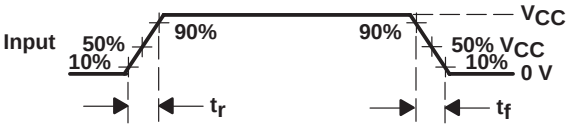


LOAD CIRCUIT

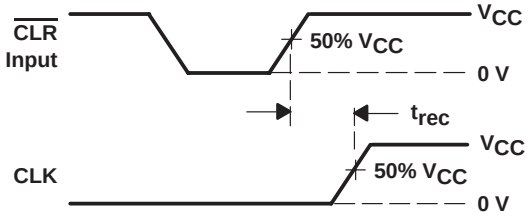
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



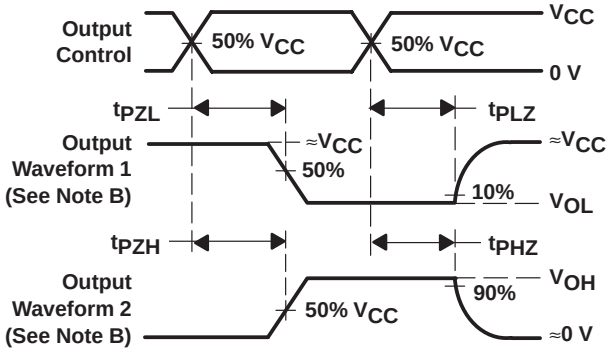
VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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