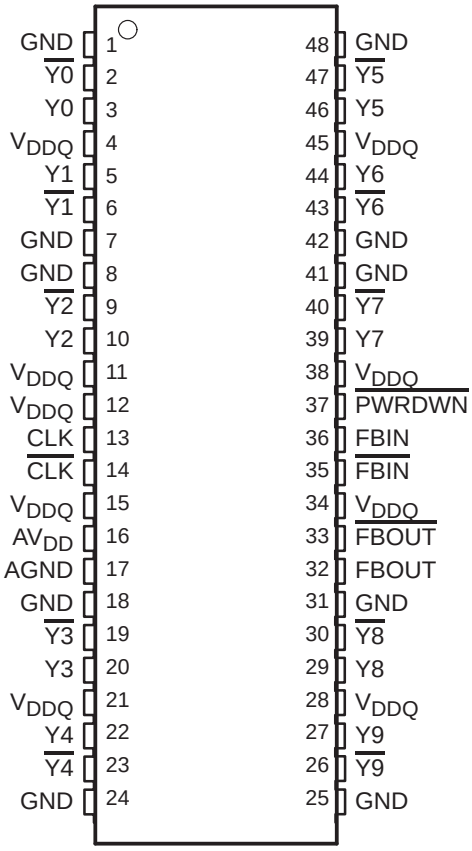
- **Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 60 to 170 MHz**
- **Low Jitter (cyc–cyc): ± 75 ps**
- **Distributes One Differential Clock Input to Ten Differential Outputs**
- **Three-State Outputs When the Input Differential Clocks Are <20 MHz**
- **Operates From Dual 2.5-V and 3.3-V Supplies**
- **48-Pin TSSOP Package**
- **Consumes < TBD-μA Quiescent Current**
- **External Feedback PIN (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**

DGG PACKAGE
(TOP VIEW)



description

The CDCV857 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair feedback clock output (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). All outputs can be enabled or disabled via a single output enable input. When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK; when $\overline{\text{PWRDWN}}$ is low, the outputs are disabled to high impedance state (3-state). When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes.

The output pairs are put into a 3-state condition, the PLL is shut down, and the device will enter a low power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typ 10 MHz). An input frequency detection circuit detects the low frequency condition and puts the output clock pairs into a high-impedance state. The CDCV857 is also able to track spread spectrum clocking for reduced EMI.

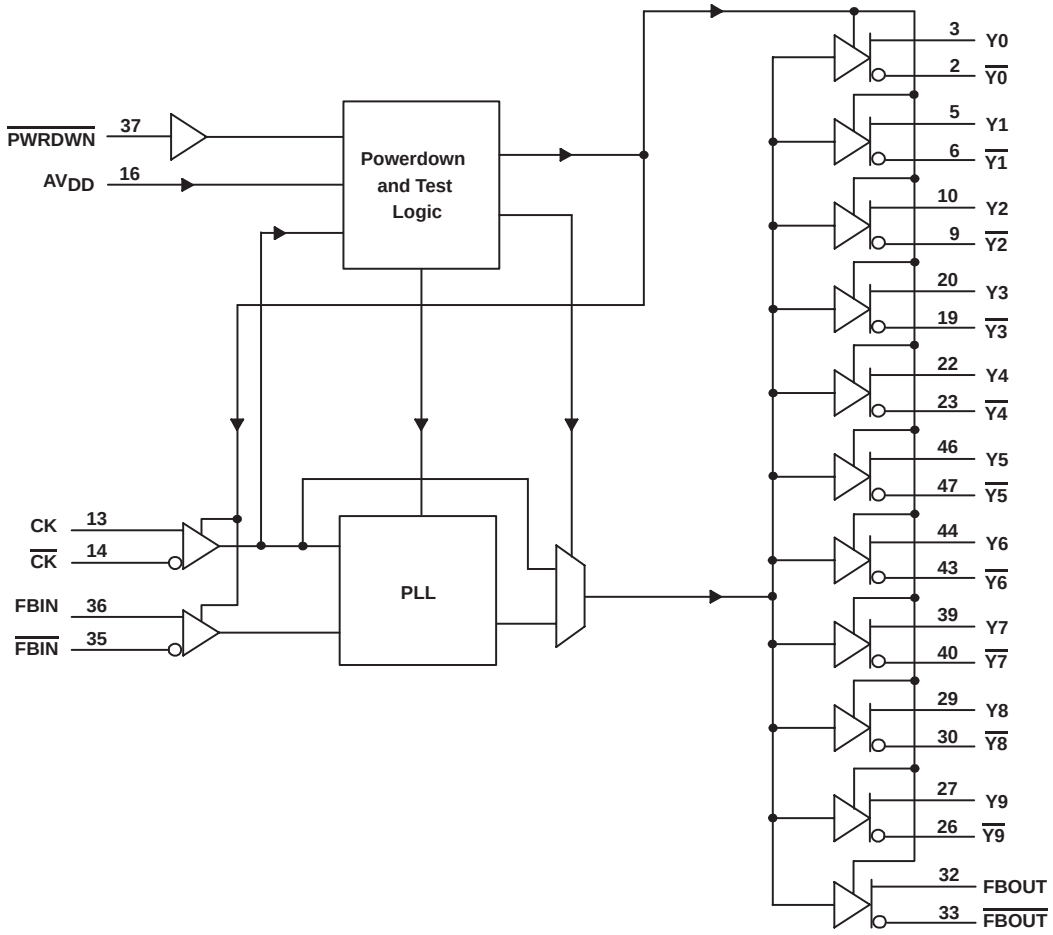
Since the CDCV857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857 is characterized for operation from 0°C to 85°C.

PRODUCT PREVIEW

FUNCTION TABLE
(Select Functions)

INPUTS				OUTPUTS				PLL
AV_{DD}	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y[0:9]	$\overline{Y[0:9]}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	17		Ground for 2.5-V analog supply
AV_{DD}	16		2.5-V Analog supply
CLK, $\overline{CLK}$	13, 14	I	Differential clock input
$\overline{FBIN}$, FBIN	35, 36	I	Feedback differential clock input
FBOUT, $\overline{FBOUT}$	32, 33	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48		Ground
$\overline{PWRDWN}$	37	I	Output enable for Y and $\overline{Y}$
V_{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45		2.5-V Supply
Y[0:9]	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	O	Buffered output copies of input clock, CLK
$\overline{Y[0:9]}$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	O	Buffered output copies of input clock, $\overline{CLK}$

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DDQ}, AV_{DD} . . . . . 0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ}) . . . . . ±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current to GND or V_{DDQ} . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 89°C/W
Storage temperature range T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

			MIN	TYP	MAX	UNIT
Supply voltage, V_{DDQ}, AV_{DD}			2.3		2.7	V
Low level input voltage, V_{IL}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$				$V_{DDQ}/2 - 0.18$	V
	$\overline{PWRDWN}$		–0.3		0.7	
High level input voltage, V_{IH}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$		$V_{DDQ}/2 + 0.18$			V
	$\overline{PWRDWN}$		1.7		$V_{DDQ} + 0.3$	
DC input signal voltage (see Note 5)			–0.3		V_{DDQ}	V
Differential input signal voltage, V_{ID} (see Note 6)	DC	CLK, FBIN	0.36		$V_{DDQ} + 0.6$	V
	AC	CLK, FBIN	0.7		$V_{DDQ} + 0.6$	
Output differential cross-voltage, V_{OX} (see Note 7)			$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V
Input differential pair cross-voltage, V_{IX} (see Note 7)			$V_{DDQ}/2 - 0.2$		$V_{DDQ}/2 + 0.2$	V
High-level output current, I_{OH}					–12	mA
Low-level output current, I_{OL}					12	mA
Input slew rate, SR			1		4	V/ns
Operating free-air temperature, T_A			0		85	°C

NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
5. DC input signal voltage specifies the allowable dc execution of differential input.
6. Differential input signal voltage specifies the differential voltage |VTR–VCP| required for switching, where VTR is the true input level and VCP is the complementary input level (see Figure 3).
7. Differential cross-point voltage is expected to track variations of VCC and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	All inputs	V_{DDQ} = 2.3 V, I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage		V_{DDQ} = min to max, I_{OH} = –1 mA	V_{DDQ} – 0.1			V
			V_{DDQ} = 2.3 V, I_{OH} = –12 mA	1.7			
V_{OL}	Low-level output voltage		V_{DDQ} = min to max, I_{OL} = 1 mA			0.1	V
			V_{DDQ} = 2.3 V, I_{OL} = 12 mA			0.6	
I_{OH}	High-level output current		V_{DDQ} = 2.3 V, V_O = 1 V	–18	–32		mA
I_{OL}	Low-level output current		V_{DDQ} = 2.3 V, V_O = 1.2 V	26	35		mA
V_O	Output voltage swing		For load condition see Figure 3	1.1		V_{DDQ} – 0.4	V
I_I	Input current	CLK, FBIN	V_{DDQ} = 2.7 V, V_I = 0 V to 2.7 V			±10	µA
I_{OZ}	High-impedance-state output current		V_{DDQ} = 2.7 V, V_O = V_{DDQ} or GND			±10	µA
I_{DDPD}	Power down current on V_{DDQ} + AV_{DD}		CLK at 0 MHz; Σ of I_{DD} and AI_{DD}			TBD	µA
I_{DD}	Dynamic current on V_{DDQ}		V_{CC} = 2.7 V, f_O = 167 MHz All outputs switching 14 pF in 60 Ω environment, See Figure 3			TBD	mA
$I_{(AVDD)}$	Supply current on AV_{DD}		AV_{CC} = 2.7 V, f_O = 167 MHz		9	12	mA
C_I	Input capacitance		V_{CC} = 2.5 V V_I = V_{CC} or GND		2		pF
C_O	Output capacitance		V_{CC} = 2.5 V V_O = V_{CC} or GND		3		pF

† All typical values are at respective nominal V_{DDQ}.
‡ The value of V_{OC} is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120-Ω resistor, where VTR is the true input signal voltage and VCP is the complementary input signal voltage (see Figure 3).

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
	Clock frequency	60	170	MHz
	Input clock duty cycle	40%	60%	
	Stabilization time† (PLL mode)		0.1	ms
	Stabilization time† (Bypass mode)		30	ms

† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{PLH}§	Low to high level propagation delay time, see Figure 2	Test mode/CLK to any output		3.5		ns
t_{PHL}§	High-to low level propagation delay time, see Figure 2	Test mode/CLK to any output		3.5		ns
t_{en}	Output enable time	$\overline{PWRDWN}$ to Y output		3		ns
t_{dis}	Output disable time	$\overline{PWRDWN}$ to Y output		3		ns
$t_{jit(per)}$	Jitter (period), see Figure 6	66 MHz				ps
		100/133/167 MHz	–75		75	ps
$t_{(jit\_cc)}$	Jitter (cycle-to-cycle), see Figure 3	66 MHz				ps
		100/133/167 MHz	–75		75	
$t_{(jit\_hper)}$	Half-period jitter, see Figure 7	100/133/167 MHz	–100		100	ps
$t_{(sir\_i)}$	Input clock slew rate, see Figure 8		1		4	V/ns
$t_{(sl\_o)}$	Output clock slew rate, see Figures 1 and 8		1		2	V/ns
$t_{(phase)}$	Phase error, see Figure 4		–100		100	ps
$t_{(skew\_o)}$¶	Output skew, see Figure 5				100	ps
$t_{(skew\_p)}$¶	Pulse skew				100	ps
	Duty cycle#	66 MHz to 100 MHz	49.5%		50.5%	
		101 MHz to 167 MHz	49%		51%	
tr, tf	Output rise and fall times (20% – 80%)	Load: 120 Ω/4 pF				ps

‡ All typical values are at respective nominal V_{DDQ}.
§ Refers to transition of noninverting output.
¶ All differential output pins are terminated with 120 Ω / 14 pF
# While the pulse skew is almost constant over frequency, the duty cycle error increases at higher frequencies. This is due to the formula: duty cycle = t_{WH}/t_C, where the cycle time (t_C) decreases as the frequency goes up.

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PARAMETER MEASUREMENT INFORMATION

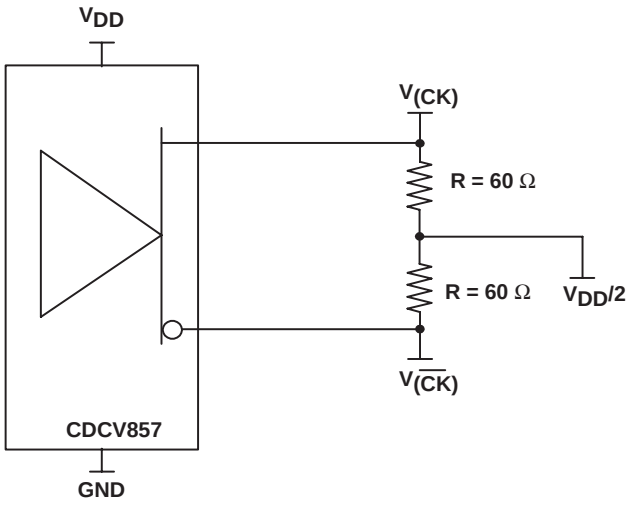
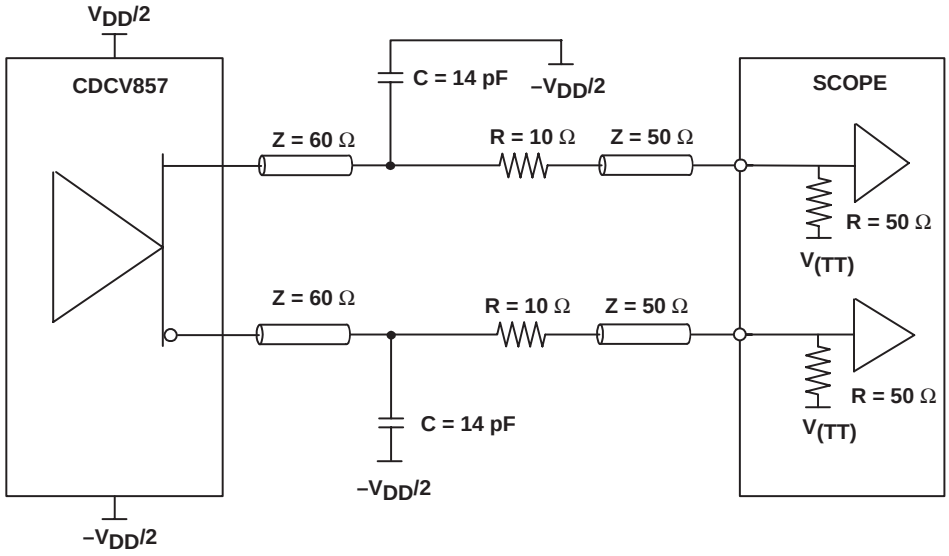
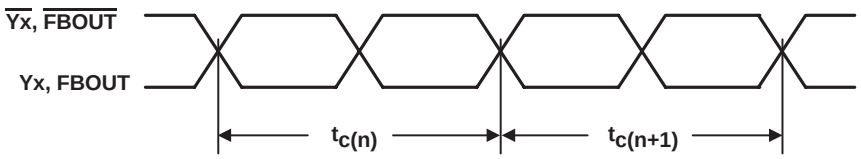


Figure 1. IBIS Model Output Load



NOTE: $V_{(TT)}$= GND

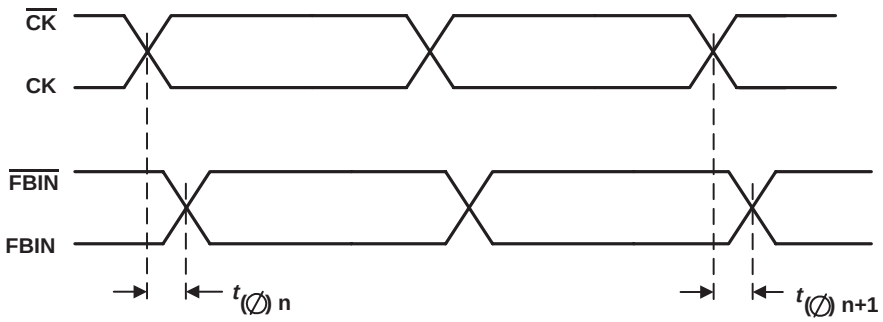
Figure 2. Output Load Test Circuit



$$t_{(jit\_cc)} = t_{c(n)} - t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION



$$t_{(\varnothing)} = \frac{\sum_{1}^{n=N} t_{(\varnothing)\,n}}{N}$$

(N is a large number of samples)

Figure 4. Static Phase Offset

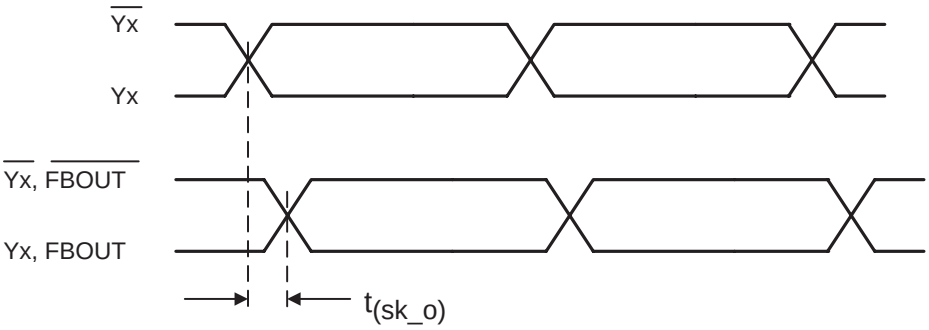
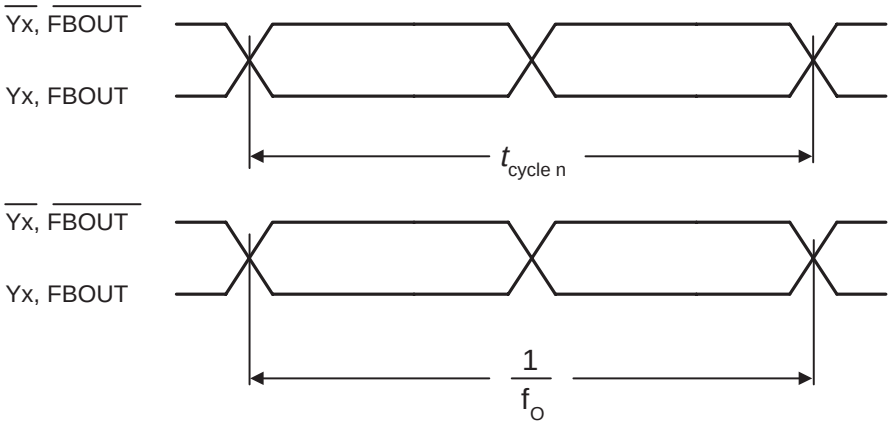


Figure 5. Output Skew



$$t_{(jit\_per)} = t_{c(n)} - \frac{1}{f_O}$$

Figure 6. Period Jitter

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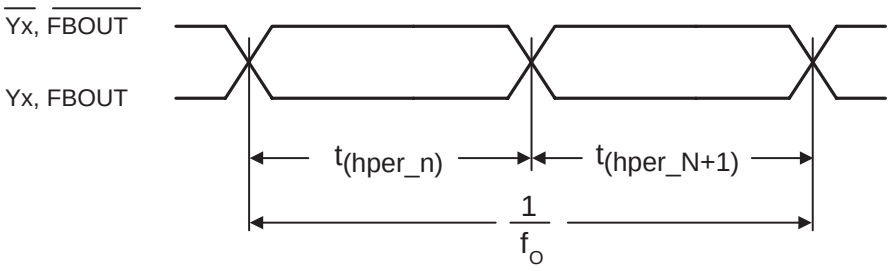
PARAMETER MEASUREMENT INFORMATION



$$t_{(jit\_hper)} = t_{(hper\_n)} - \frac{1}{2xf_O}$$

Figure 7. Half-Period Jitter

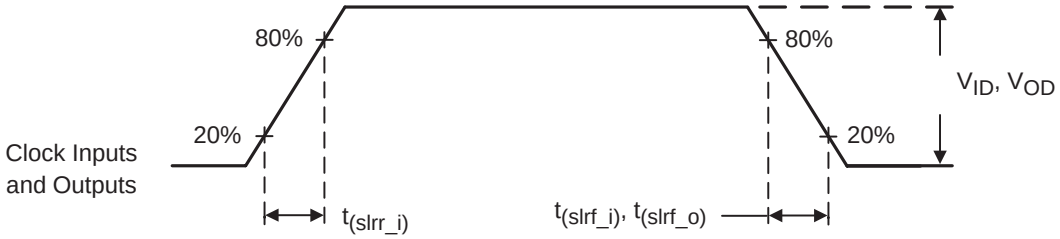


Figure 8. Input and Output Slew Rates

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