

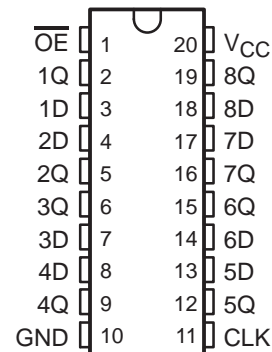
SN74LVC374

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS296B – JANUARY 1993 – REVISED NOVEMBER 1994

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC374 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components. \overline{OE} does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC374 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
\overline{OE}	CLK	D	
L	\uparrow	H	H
L	\uparrow	L	L
L	H or L	X	Q_0
H	X	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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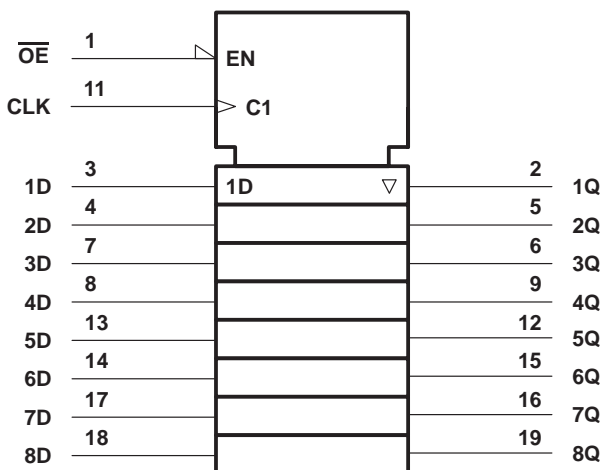
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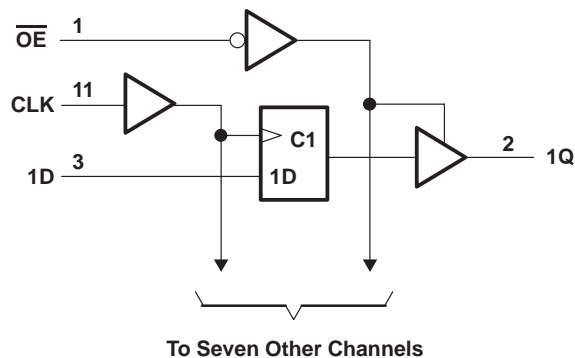
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I	–0.5 V to 4.6 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. This value is limited to 4.6 V maximum.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2		V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.7\text{ V}$		–12	mA
		$V_{CC} = 3\text{ V}$		–24	
I_{OL}	Low-level output current	$V_{CC} = 2.7\text{ V}$		12	mA
		$V_{CC} = 3\text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0	10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC} [†]	T _A = −40°C to 85°C			UNIT
			MIN	TYP	MAX	
V _{OH}	I _{OH} = −100 μA	MIN to MAX	V _{CC} −0.2			V
	I _{OH} = −12 mA	2.7 V	2.2			
		3 V	2.4			
	I _{OH} = −24 mA	3 V	2			
V _{OL}	I _{OL} = 100 μA	MIN to MAX	0.2			V
	I _{OL} = 12 mA	2.7 V	0.4			
	I _{OL} = 24 mA	3 V	0.55			
I _I	V _I = V _{CC} or GND	3.6 V	±5			μA
I _{OZ}	V _O = V _{CC} or GND	3.6 V	±10			μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V	20			μA
ΔI _{CC}	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		500			μA
C _i	V _I = V _{CC} or GND	3.3 V	5.5			pF
C _O	V _O = V _{CC} or GND	3.3 V	5.8			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	100	0	80	MHz
t_w	Pulse duration, CLK high or low	5		5		ns
t_{su}	Setup time, data before CLK \uparrow	2		2		ns
t_h	Hold time, data after CLK \uparrow	2		2		ns



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switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	150		80		MHz
t_{pd}	CLK	Q	1.5	4.9	8.5	1.5	9.5	ns
t_{en}	$\overline{\text{OE}}$	Q	1.5	4.1	8.5	1.5	9.5	ns
t_{dis}	$\overline{\text{OE}}$	Q	1.5	4.2	7.5	1.5	8.5	ns

operating characteristics, $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$

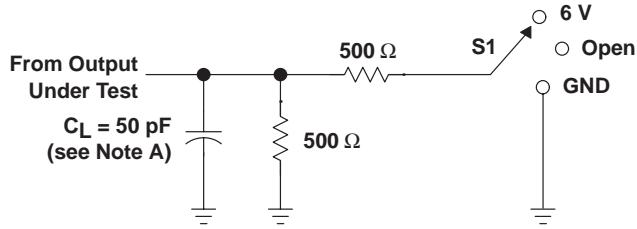
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$	18	pF
		Outputs disabled		9	

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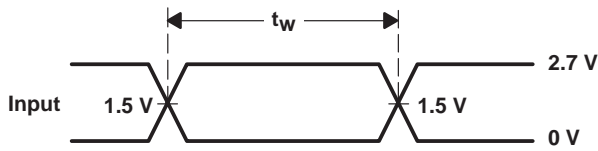
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PARAMETER MEASUREMENT INFORMATION

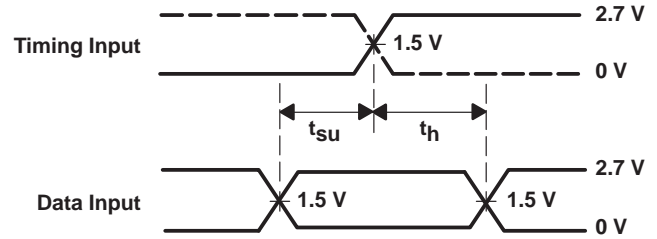


LOAD CIRCUIT FOR OUTPUTS

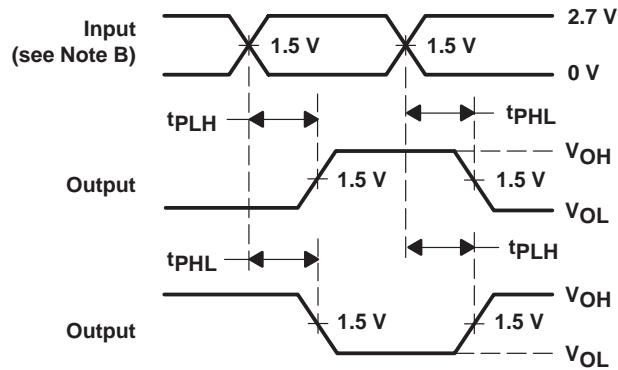
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



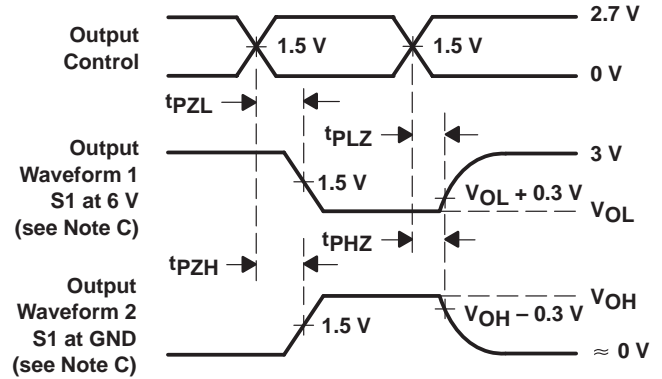
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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