DEVICE
SPECIFICATION

Now available with Loop Timing!

SONET/SDH/ATM OC-3/OC-12 TRANSCEIVER S3028

FEATURES

- Complies with Bellcore and ITU-T specifications
- Jitter generation better than ITU-T requirements
- On-chip high-frequency PLL for clock generation
- Supports 155.52 Mbps (OC-3) and 622.08 Mbps (OC-12)
- Selectable reference frequencies of 19.44, 38.88, 51.84, or 77.76 MHz
- Interface to both PECL and TTL logic
- 4-bit or 8-bit OC-3 TTL datapath
- 8-bit OC-12 TTL datapath
- Compact 64 PQFP package
- Diagnostic loopback mode
- Line loopback mode
- Lock detect
- LOS input
- Low jitter PECL interface
- 0.9W typical power dissipation
- Loop Timing (S3028B only)
- Forward Clocking (S3028B only)
- "Squelched Clock" operation (S3028B only)
- 5 V Power supply

APPLICATIONS

- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

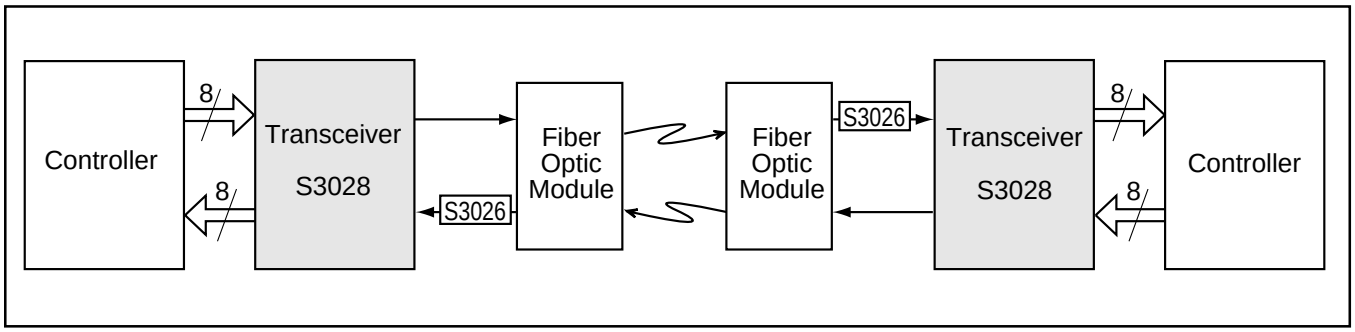
The S3028 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-12 (622.08 Mbit/s) and OC-3 (155.52 Mbit/s) interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications and can be used in conjunction with AMCC's S3026 Clock Recovery Unit (CRU). Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3028 transceiver chip allowing the use of a slower external transmit clock reference. The S3028 also performs SONET/SDH frame detection. The chip can be used with a 19.44, 38.88, 51.84 or 77.76 MHz reference clock, in support of existing system clocking schemes.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3028 is packaged in a 64 PQFP, offering designers a small package outline.

Since the S3028 jitter generation is better than the ITU-T requirements over all reference frequencies, the designer can meet the overall system requirement including the optical interface devices (refer to Table 9 for jitter generation specifications).

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3028 chip supports OC-3 and OC-12 rates (155.52 and 622.08 Mbit/s).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-12 consists of 36 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 36 overhead and 1044 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 2. SONET Structure

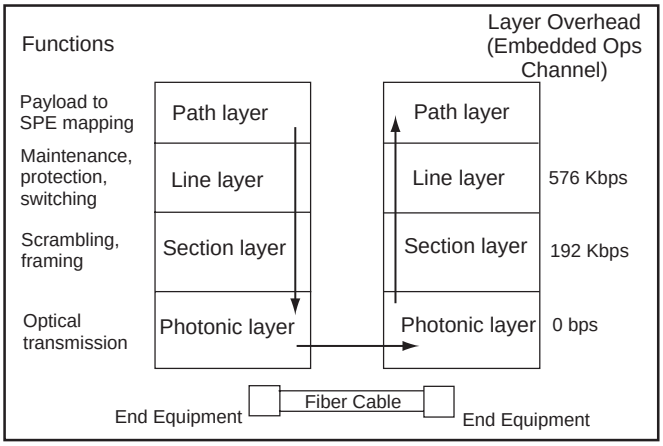


Figure 3. STS–12/OC–12 Frame Format

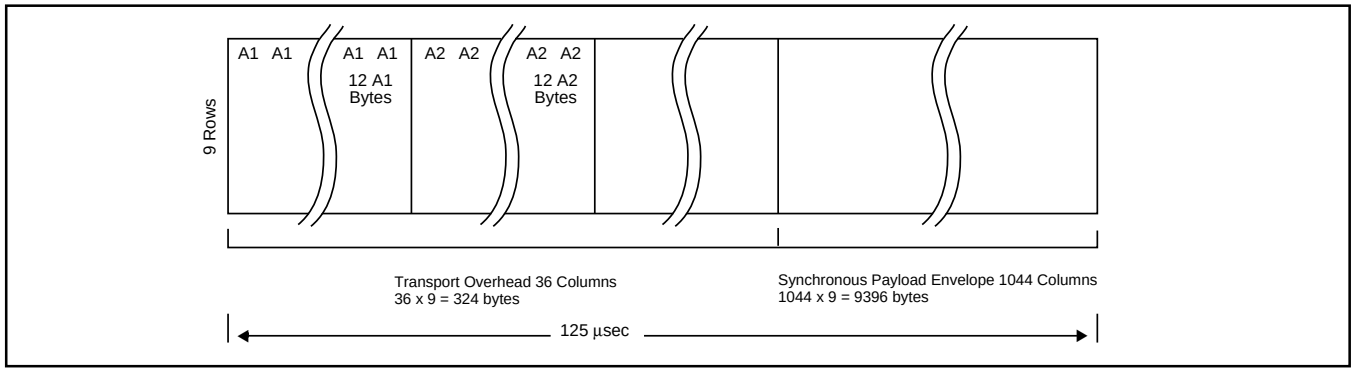
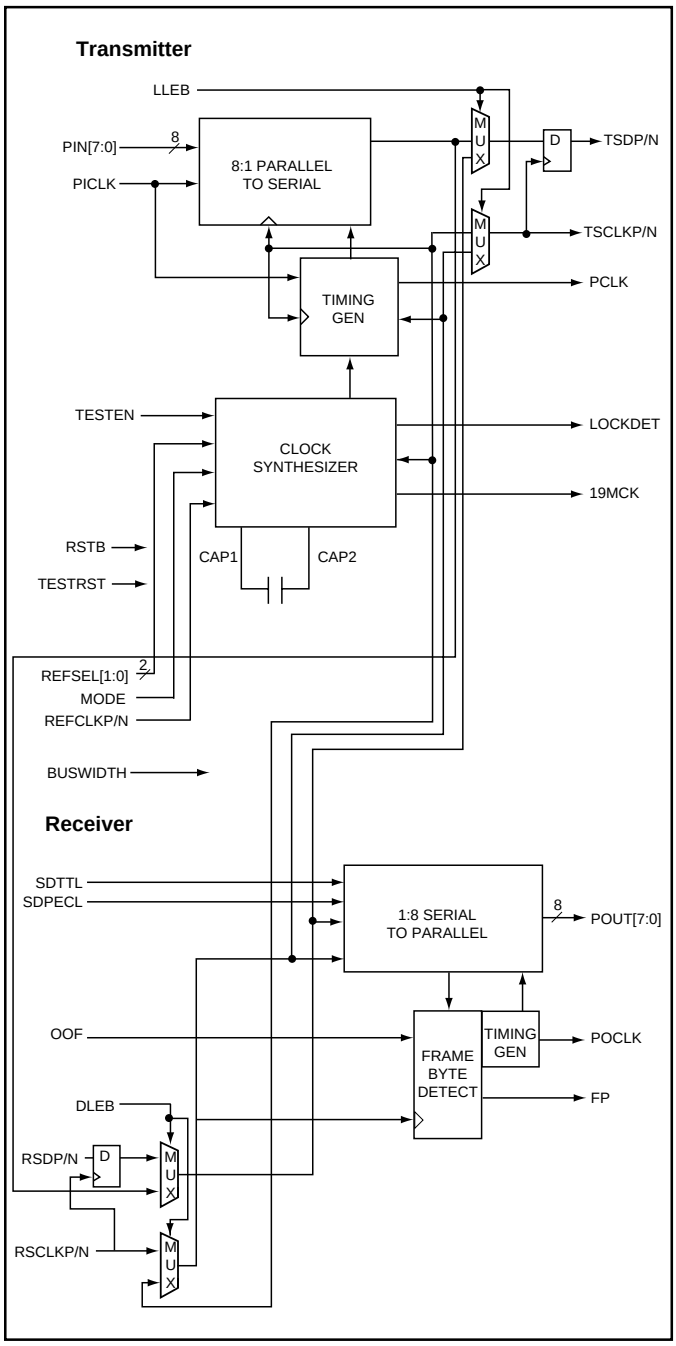


Figure 4. S3028 Transceiver Functional Block Diagram



S3028 OVERVIEW

The S3028 transceiver implements SONET/SDH serialization/deserialization, transmission, and frame detection/recovery functions. The block diagram in Figure 4 shows basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream, framing, and clock distribution throughout the front end.

The S3028 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 4 or 8-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Serial input
2. Frame detection
3. Serial-to-parallel conversion
4. 4 or 8-bit parallel output

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figures 7 through 10.

Suggested Interface Devices

AMCC	S3026	622/155 Mbit/s	Clock Recovery Device
AMCC	S3027	622/155 Mbit/s	Clock Recovery Device
AMCC	CONGO (S1201)		POS/ATM SONET Mapper
AMCC	NILE (S1202)		ATM SONET Mapper

TRANSCEIVER FUNCTIONAL DESCRIPTION

TRANSMITTER OPERATION

The S3028 transceiver chip performs the serializing stage in the processing of a transmit SONET STS-3 or STS-12 bit serial data stream. It converts the 8-bit parallel 19.44, 38.88 or 77.76 Mbyte/sec data stream into bit serial format at 155.52 or 622.08 Mbit/sec. Diagnostic loopback is provided (transmitter to receiver). Line loopback is also provided (receiver-to-transmitter).

A high-frequency bit clock can be generated from a 19.44, 38.88, 51.84 or 77.76 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Clock Synthesizer

The clock synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock phase synchronized with the input Reference Clock (REFCLK). There are three selectable output clock frequencies that are synthesizable from any of four selectable reference frequencies for SONET/SDH operation.

The MODE inputs select the output serial clock frequency to be 622.08 MHz for STS-12, or 155.52 MHz for STS-3. Their frequencies are selected as shown in Table 2.

Table 2. Clock Frequency Options

MODE	Output Clock Frequency	Operating Mode
1	622.08 MHz	STS-12
0	155.52 MHz	STS-3

The REFSEL[1:0] inputs in combination with the MODE input select the ratio between the output clock frequency and the reference input frequency, as shown in Table 3. This ratio is adjusted for each of the four operating modes so that the reference frequency selected by the REFSEL[1:0] is the same for all modes.

The REFCLK input must be generated from a differential PECL crystal oscillator which has a frequency accuracy that meets the value specified in Table 9 in order for the TSCLK frequency to have the same accuracy required for operation in a SONET system.

Table 3. Reference Frequency Options

REFSEL[1:0]	Reference Clock Frequency	Operating Mode
00	19.44 MHz	STS-12, STS-3
01	38.88 MHz	STS-12, STS-3
10	51.84 MHz	STS-12, STS-3
11	77.76 MHz	STS-12

Table 4. Reference Jitter Limits

Frequency Band	Maximum Reference Clock Jitter	Operating Mode
12 kHz to 5 MHz	14 ps rms	STS-12
12 kHz to 1 MHz	56 ps rms	STS-3

In order to meet the 0.01 UI SONET jitter generation specifications, the maximum reference clock jitter must be guaranteed over the 12 kHz to 1 MHz bandwidth for the STS-3 operating mode. For details of reference clock jitter requirements, see Table 4.

The on–chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLK input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generator

The timing generator function, seen in Figure 4, provides two separate functions. It provides a byte rate version of the TSCLK, and a mechanism for aligning the phase between the incoming byte clock and the clock which loads the parallel-to-serial shift register.

The PCLK output is a byte rate version of TSCLK. For STS-12, the PCLK frequency is 77.76 MHz, and for STS-3, its frequency is 19.44 or 38.88 MHz. PCLK is intended for use as an 8-bit parallel clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3028 device.

In the parallel-to-serial conversion process, the incoming data is passed from the PICLK 8-bit parallel clock timing domain to the internally generated serial clock timing domain, which is phase aligned to TSCLK.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the Reference Clock REFCLK. The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the internal clock with that of the reference clock (REFCLK). The modulus of the counter is a function of the reference clock frequency and the operating frequency.

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 4 is comprised of two 8-bit wide registers. The first register latches the data from the PIN[7:0] bus on the rising edge of PICLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

An internally generated byte clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data is shifted out of the second register at the TSCLK rate.

RECEIVER OPERATION

The S3028 transceiver chip provides the first stage of the digital processing of a receive SONET STS-3 or STS-12 bit-serial stream. It converts the bit-serial 155.52 or 622.08 Mbit/sec data stream into a 19.44, 38.88 or 77.76 Mbyte/sec parallel data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). An additional loopback mode is provided for line loopback (receiver to transmitter).

Frame and Byte Boundary Detection

The frame and byte boundary detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing pattern detection is enabled and disabled by the Out Of Frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled for the duration that OOF is set High. It is disabled when a framing pattern is detected after OOF is set Low. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (RSD or looped transmitter data). The timing generator block takes the located byte boundary and uses it to block the incoming data stream into bytes for output on the parallel output data bus (POUT[7:0]). When framing pattern detection is enabled, the frame boundary is reported on the Frame Pulse (FP) output when any 48-bit pattern matching the framing pattern is detected on the incoming data stream. When framing pattern detection is disabled, the byte boundary is frozen to the location found when detection was previously enabled. Only framing patterns aligned to the fixed byte boundary are indicated on the FP output.

The probability that random data in an STS-3 or STS-12 stream will generate the 48-bit framing pattern is extremely small. It is highly improbable that a mimic pattern would occur within one frame of data. Therefore, the time to match the first frame pattern and to verify it with down-stream circuitry, at the next occurrence of the pattern, is expected to be less than the required 250 µs, even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set low to disable the frame search process from trying to synchronize to a mimic frame pattern.

Serial to Parallel Converter

The serial to parallel converter consists of three 8-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is an 8-bit internal holding register, which transfers data from the serial to parallel register on byte boundaries as determined by the frame and byte boundary detection block. On the falling edge of the free running POCLK, the data in the holding register is transferred to an output holding register which drives POUT[7:0].

The delay through the serial to parallel converter can vary from 1.5 to 2.5 byte periods (12 to 20 serial bit periods) measured from the first bit of an incoming byte to the beginning of the parallel output of that byte. The variation in the delay is dependent on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of POCLK, which is independent of the byte boundaries. The advantage of this serial to parallel converter is that POCLK is neither truncated nor extended during reframe sequences.

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the serial-to-parallel block in place of the normal data stream (RSD).

Line Loopback

The line loopback circuitry consists of alternate clock and data output drivers. For the S3028, it selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable (LLEB) input is inactive, it selects data and clock from the parallel to serial converter block. When LLEB is active, it forces the output data multiplexer to select data and clock from the RSD and RSCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. Diagnostic loopback and line loopback can be active at the same time.

Loop Timing

In loop timing mode, the clock synthesizer PLL of the S3028 is bypassed, and the timing of the entire transmitter section is controlled by the Receive Serial Clock, RSCLKP/N. This mode is entered by setting the TESTEN input to a TTL high level.

The internal PLL continues to operate in this mode, and continues as the source for the 19MCK. If this signal is being used (e.g. as the reference for an external clock recovery device such as the AMCC S3026), the REFCLKP/N and REFSEL[1:0] inputs must be properly driven in either 19.44 MHz or 51.84 MHz mode. The 19MCK output should not be used in loop timing mode if 77.76 or 38.88 MHz reference operation is selected. The MODE input has no effect on the transmitter operation if loop timing is selected.

Forward Clocking

For both 77.76 MHz and 38.88 MHz reference operation, the S3028 operates in the forward clocking mode. The PLL locks the PCLK output of the transmitter section to the REFCLK with a fixed and repeatable phase relation. This allows the transmitter data source to also be the timing source for the serial clock synthesis.

For operation at 19.44 MHz and 51.84 MHz references, separate timing paths are use for PLL control and PCLK generation, and forward clocking is not recommended.

"Squelched Clock" Operation

Some integrated optical receiver/clock recovery modules force their recovered serial receive clock output to the logic zero state if the optical signal is removed or reduced below a fixed threshold. This condition is accompanied by the expected deassertion of the signal detect output.

The S3028B has been designed for operation with clock recovery devices that provide continuous serial clock for seamless down stream clocking in the event of optical signal loss. For operation with an optical transceiver that provides the “squelched clock” behavior as described above, the S3028B can be operated in the “squelched clock mode” by setting the BUSWIDTH input low, (4 bit mode at 155.52 Mbit/s rate) while the MODE input is set high (622.08 Mbit/s rate). "Squelched Clock" mode is available in 622.08 Mbit/s mode only.

The Receive Serial Clock, RSCLKP/N, is used for all receiver timing when the SDPECL/SDTTL inputs are in the active state. When the SDPECL/SDTTL inputs are placed in the inactive state, (usually by the deassertion of LOCKDET or signal detect from the optical transceiver/clock recovery unit) the transmitter serial clock will be used to maintain timing in the receiver section. This will allow the POCLK to continue to run and the parallel outputs to flush out the last received characters and assume the all zero state imposed at the serial data input.

In this mode there will be a random 1.6 nsec shortening or lengthening of the POCLK cycle, resulting in an apparent phase shift in the POCLK at the deassertion of the signal detect condition. Another similar phase shift will occur when the signal detect condition is reasserted.

In the normal operating mode with both MODE and BUSWIDTH inputs high, there will be no phase discontinuities at the POCLK output during signal loss or reacquisition (assuming operation with continuous clocking from the CRU device such as the AMCC S3026 or S3027)

Table 5. S3028 Transceiver Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PIN7 PIN6 PIN5 PIN4 PIN3 PIN2 PIN1 PIN0	TTL	I	60 59 58 57 56 55 54 53	Parallel Data Input, a 77.76, 51.84, 38.88 or 19.44 Mbyte/s word, aligned to the PICLK, Paralle Input Clock. PIN7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). PIN[7:0] is sampled on the rising edge of PICLK. If a 4-bit bus width is selected, PIN7 is the most significant bit, and bit 4 is the least significant bit.
PICLK	TTL	I	61	Parallel Input Clock, a 77.76, 51.84, 38.88 or 19.44 MHz, nominally 50% duty cycle input clock, to which PIN[7:0] is aligned. PICLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PIN[7:0]. After a master reset, two rising edges of PICLK are required to fully initialize the internal datapath.
CAP1 CAP2	Analog	I	10 11	The loop filter capacitor is connected to these pins. The capacitor value should be 0.01µF ±10% tolerance, X7'R dielectric. 50 volt is recommended (16 volt is acceptable).
TSDP TSDN	Diff. PECL	O	17 18	Transmit Serial Data. Serial data stream signals, normally connected to an optical transmitter module.
TSCLKP TSCLKN	Diff. PECL	O	21 20	Transmit Serial Clock that can be used to retime the TSD signal. This clock will be 622.08 MHz or 155.52 MHz, depending on the operating mode.
PCLK	TTL	O	62	A reference clock generated by dividing the internal bit clock by eight (or by four when BUSWIDTH is low). It is normally used to coordinate 8-bit wide transfers between upstream logic and the S3028 device.
LOCKDET	TTL	O	63	Lock Detect signal. Active High. When active, this output indicates that the transmit PLL is locked onto the reference clock input.

Table 5. S3028 Transceiver Pin Assignment and Descriptions (continued)

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Diff. PECL	I	24 25	Receive Serial Data stream signals normally connected to an optical receiver module. These inputs are clocked by the RSCLK inputs.
RSCLKP RSCLKN	Diff. PECL	I	27 28	Receive Serial Clock. Recovered clock signal that is synchronous with the RSD inputs. This clock is used by the receive section as the master clock to perform framing and deserialization functions.
OOF	TTL	I	33	Out Of Frame indicator used to enable framing pattern detection logic in the S3028. This logic is enabled by a rising edge on OOF, and remains enabled until frame boundary is detected or when OOF is set low, whichever is longer. OOF is an asynchronous signal with a minimum pulse width of one POCLK period. (See Figures 12 and 13.)
SDPECL	PECL	I	23	PECL Signal Detect. PECL with internal 1kΩ pull-down. Active High when SDTTL is held at a logic 0. Active Low when SDTTL is held at a logic 1. A single-ended 10K PECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDPECL is inactive, the data on the Serial Data in (RSDP/N) pins will be internally forced to a constant zero. When SDPECL is active, data on the RSDP/N pins will be processed normally. When SDTTL is to be connected to the optical receiver module instead of SDPECL, then SDPECL should be tied High to implement an active low signal detect, or left unconnected to implement an active high signal detect.
SDTTL	TTL	I	22	TTL Signal Detect. Active High when SDPECL is unconnected (logic 0). Active Low when SDPECL is held at a logic 1. A single-ended TTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDTTL is inactive, the data on the RSDP/N pins will be internally forced to a constant zero. When SDTTL is active, data on the RSDP/N pins will be processed normally.
POUT7 POUT6 POUT5 POUT4 POUT3 POUT2 POUT1 POUT0	TTL	O	45 44 43 41 40 39 37 36	Parallel Output Data bus, a 77.76, 51.84, 38.88 or 19.44 Mbyte/s word, aligned to the POCLK Parallel Output Clock. POUT7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). POUT[7:0] is updated on the falling edge of POCLK. If a 4-bit bus width is selected, POUT7 is the most significant bit, and bit 4 is the least significant bit.
19MCK	TTL	O	64	19 MHz clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function (such as the S3026).

Table 5. S3028 Transceiver Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
FP	TTL	O	35	Frame Pulse. Indicates frame boundaries in the incoming data stream (RSD). If framing pattern detection is enabled, as controlled by the OOF input, FP pulses high for one POCLK cycle when a 48-bit sequence matching the framing is detected on the RSD inputs. When framing pattern detection is disabled, FP pulses high when the incoming data stream, after byte alignment, matches the framing pattern. FP is updated on the falling edge of POCLK.
POCLK	TTL	O	47	A 77.76, 51.84, 38.88, or 19.44 MHz nominally 50% duty cycle, byte rate output clock that is aligned to POUT[7:0] byte serial output data. POUT[7:0] and FP are updated on the falling edge of POCLK.

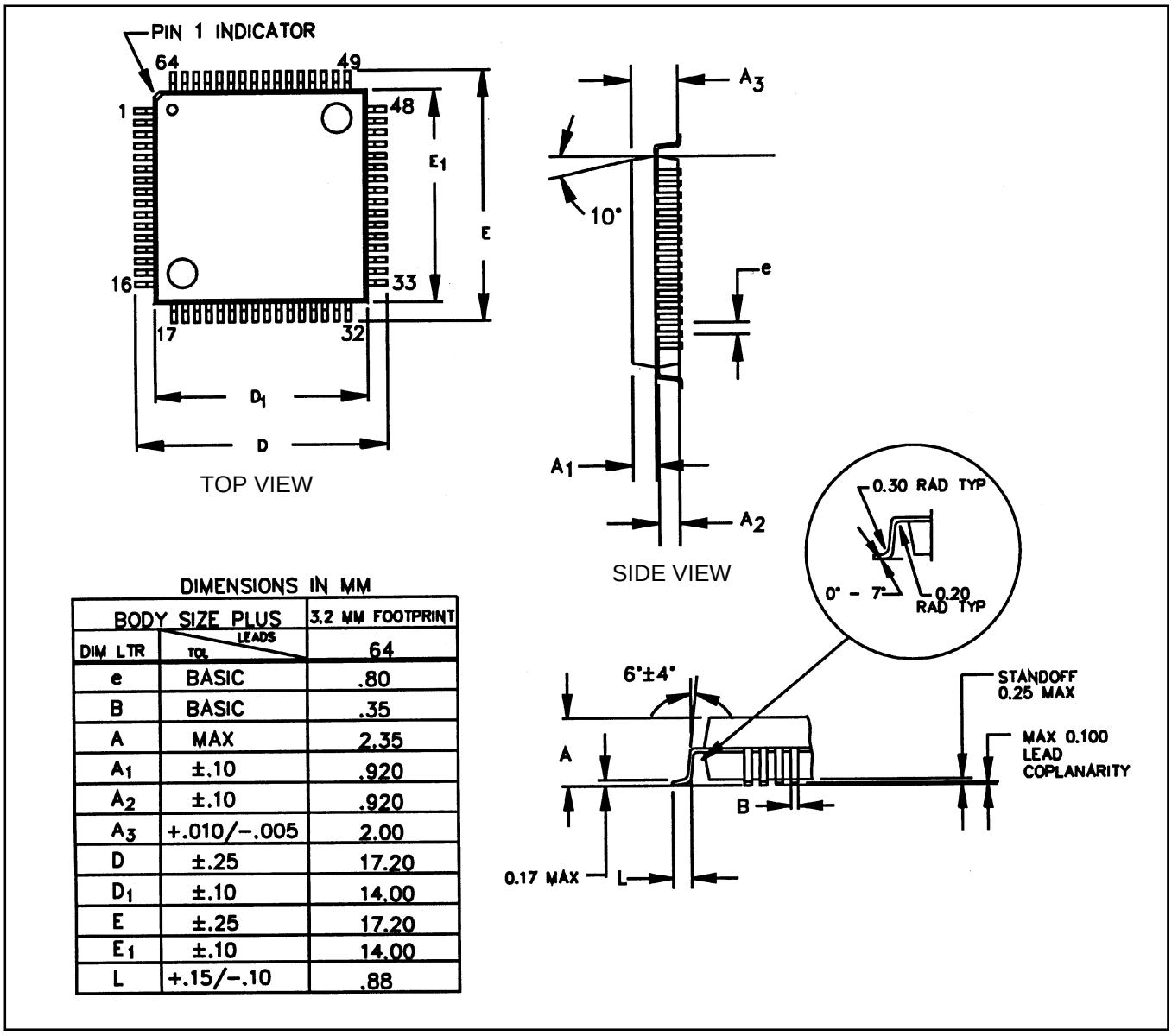
Table 6. S3028 Common Control Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TESTEN	TTL	I	13	Test Enable. Test clock/loop timing enable signal. Active High. Set high to provide access to the PLL during production tests. Also used to enable loop timing mode when High (S3028B only).
BUSWIDTH	TTL	I	30	Bus Width selection. Used to select 4-bit or 8-bit operation of the transmit and receive parallel interfaces. Low selects a 4-bit bus width. High selects an 8-bit bus width. Must be high for 622.08 Mbit/s normal operation (S3028). Low in 622.08 Mbit/s mode enables squelched clock operation (S3028B only).
REFCLKP REFCLKN	Diff. PECL	I	15 14	Reference Clock input. Used as the reference for the internal bit clock frequency synthesizer.
DLEB	TTL	I	32	Diagnostic Loopback Enable. Active Low. Selects diagnostic loopback. When DLEB is high, the S3028 device uses the primary data (RSD) and clock (RSCLK) inputs. When low, the S3028 device uses the diagnostic loopback clock and data from the transmitter.
RSTB	TTL	I	48	Master Reset. Reset input for the device, active Low. During reset, PCLK does not toggle.
LLEB	TTL	I	31	Line Loopback Enable. Active Low. Selects line loopback. When LLEB is active, the S3028 will route the data from the RSD/RSCLK inputs to the TSD/TSCLK outputs.
REFSEL1 REFSEL0	TTL	I	4 3	Reference Select inputs. Used to select the reference clock frequency. See Table 3.
MODE	TTL	I	49	Mode select, used to select the serial bit rate. Low selects 155.52 Mbit/s. High selects 622.08 Mbit/s. For 155.52 Mbit/s mode, the parallel interface can operate with 4 bits.
TESTRST	TTL	I	50	Test Reset input. Active High. Used to reset portions of the PLL during production testing. Held Low for normal operation.

Table 7. S3028 Power Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
AGND	0V	–	5, 8	Analog 0V
AVCC	+5V	–	6, 7	Analog +5V via individual Ferrite bead (BLM32A06) and individual decoupling.
CGND	0V	–	9, 12	Ground ring to guard CAP1 and CAP2 pins connect to ground plane at a single point.
TXOUTGND	0V	–	19	Digital 0V
TXOUTVCC	+5V	–	16	Digital +5V, Individually decoupled.
RXCOREVCC	+5V	–	26, 52	Digital +5V, individually decoupled.
RXCOREGND	0V	–	29, 51	Digital 0V
TTLVCC	+5V	–	38, 46	Digital +5V, Individually decoupled.
TTLGND	0V	–	34, 42	Digital 0V
TXCOREGND	0V	–	2	Digital 0V
TXCOREVCC	+5V	–	1	Digital +5V, individually decoupled.

Figure 5. 64 PQFP Package



DIMENSIONS IN MM

BODY SIZE PLUS		3.2 MM FOOTPRINT
DIM LTR	TOL / LEADS	64
e	BASIC	.80
B	BASIC	.35
A	MAX	2.35
A_1	±.10	.920
A_2	±.10	.920
A_3	+.010/−.005	2.00
D	±.25	17.20
D_1	±.10	14.00
E	±.25	17.20
E_1	±.10	14.00
L	+.15/−.10	.88

Table 8. Thermal Management

Max Power	Θja
1.37 W	52.0 ˚ C/W

Figure 6. S3028 64 PQFP Pinout

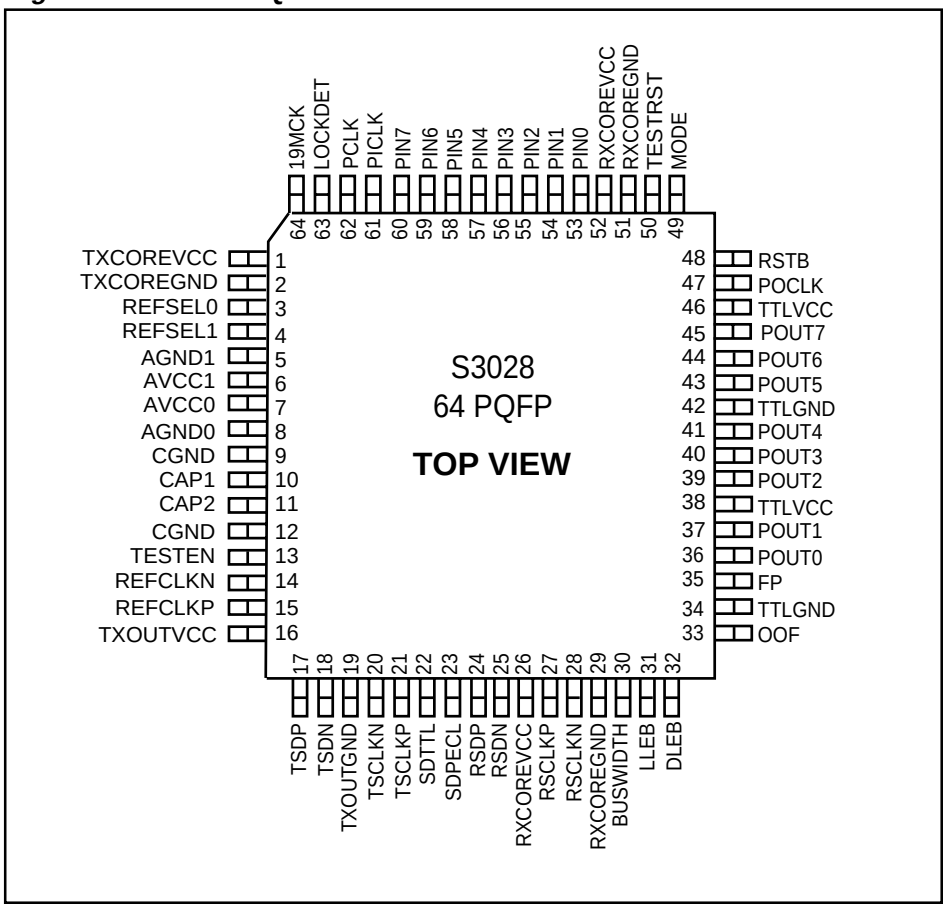


Table 9. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08 ±12%		MHz	
Data Output Jitter* **STS-12** –19.44 MHz Ref. Clk. –38.88 MHz Ref. Clk. –51.84 MHz Ref. Clk. –77.76 MHz Ref. Clk. **STS-3** –19.44 MHz Ref. Clk. –38.88 MHz Ref. Clk. –51.84 MHz Ref. Clk.			0.007 0.006 0.005 0.004 0.002 0.001 0.001	UI (rms)	rms jitter, in lock
Reference Clock Frequency Tolerance*	-20		+20	ppm	Required to meet SONET output frequency specification
Reference Clock Input Duty Cycle	30		70	% of UI	
Reference Clock Rise & Fall Times			2.0	ns	10% to 90% of amplitude
ECL Output Rise & Fall Times			450	ps	10% to 90%, 50Ω load, 5 pF cap

* Noise on REFCLKP/N should be less than 14 ps rms in a jitter frequency band from 12 KHz to 5 MHz for STS-12.

Table 10. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with respect to GND	-0.5		+7.0	V
Voltage on Any TTL Input Pin	-0.5		+5.5	V
Voltage on Any PECL Input Pin	0		V_{CC}	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA
High Speed PECL Output Source Current			50	mA

ESD Ratings

The S3028 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1000 V, except Pin 6, Pin 10, Pin 11, Pin 16, and Pin 21.

Table 11. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Conditions
Ambient Temperature Under Bias	-40		85	˚C	See Note 1.
Junction Temperature Under Bias	-40		+130	˚C	
Voltage on V_{CC} with respect to GND	4.75		5.25	V	
Voltage on Any TTL Input Pin	0		V_{CC}	V	
Voltage on Any PECL Input Pin	V_{CC} -2		V_{CC}	V	
I_{CC} Supply Current		180	260	mA	Outputs open, V_{CC} = V_{CC} max
P_D Power Dissipation		0.900	1.37	W	Outputs open, V_{CC} = V_{CC} max
Capacitive Load on Any TTL Pin			15	pF	

1. Applications above 70˚C ambient require one or more power/GND planes in the circuit board.

Table 12. TTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.7			V	V_{CC} = min, I_{OH} = -1mA
V_{OL}	Output Low Voltage (TTL)			.5	V	V_{CC} = min, I_{OL} = 4mA[1]
V_{IH}	Input High Voltage (TTL)	2.0		5.5	V	$I_H \leq$ 1mA at V_{IH} = 5.5V
V_{IL}	Input Low Voltage (TTL)	0		0.8	V	
I_{IH}	Input High Current (TTL)			50	µA	V_{IN} = 2.4V
I_{IL}	Input Low Current (TTL)	-500		-50	µA	V_{IN} = 0.5V
I_I	Input High Current at Max V_{CC}			1.0	mA	V_{CC} = max, V_{IN} = 5.5V
I_{OS}	Output Short Circuit Current	-100.0		-25.0	mA	V_{CC} = max, V_{OUT} = 0.5V
V_{IK}	Input Clamp Diode Voltage	-1.2			V	V_{CC} = min, V_{IN} = -18mA

1. 19MCK output: I_{OL} = 2mA

Table 13. PECL Input/Output DC Characteristics

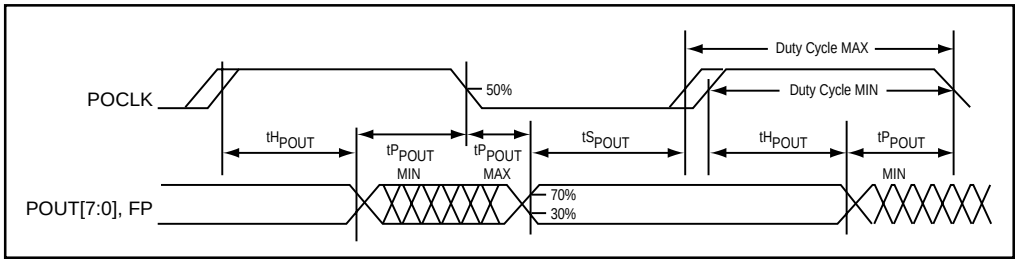
Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	PECL Input Low Voltage	V_{CC} -2.000 V_{CC} -2.000 V_{CC} -2.000		V_{CC} -1.504 V_{CC} -1.475 V_{CC} -1.441	V	-40 ˚ C 25 ˚ C 85 ˚ C
V_{IH}	PECL Input High Voltage	V_{CC} -1.225 V_{CC} -1.105 V_{CC} -1.023		V_{CC} -0.778 V_{CC} -0.680 V_{CC} -0.573	V	-40 ˚ C 25 ˚ C 85 ˚ C
V_{OL}	PECL Output Low Voltage for Differential PECL Outputs	V_{CC} -2.500 V_{CC} -2.500 V_{CC} -2.500		V_{CC} -1.647 V_{CC} -1.620 V_{CC} -1.573	V	-40 ˚ C 25 ˚ C 85 ˚ C
V_{OH}	PECL Output High Voltage for Differential PECL Outputs	V_{CC} -1.500 V_{CC} -1.422 V_{CC} -1.342		V_{CC} -0.828 V_{CC} -0.730 V_{CC} -0.623	V	-40 ˚ C 25 ˚ C 85 ˚ C
ΔV_{DIFF}	Min. Differential Input Voltage Swing for Differential PECL Inputs	100		1300	mV	
ΔV_{OUT}	Serial Output Voltage Swing for Differential PECL Outputs	600		1600	mV	50Ω to V_{CC} -2.0V

Table 14. AC Receiver Timing Characteristics

Symbol	Description	Min	Max	Units
	POCLK Duty Cycle	45	55	%
tP_{POUT}	POCLK Low to POUT[7:0] valid prop. delay at STS-3, 8-bit POCLK Low to POUT[7:0] valid prop. delay at STS-3, 4-bit POCLK Low to POUT[7:0] valid prop. delay at STS-12	-8 -8 -3	0 0 1	ns ns ns
tS_{POUT}	POUT[7:0] and FP Setup Time w.r.t. POCLK[1]	4		ns
tH_{POUT}	POUT[7:0] and FP Hold Time w.r.t. POCLK[1]	3		ns
tS_{RSD}	RSDP/N Setup Time w.r.t. RSCLKP/N	400		ps
tH_{RSD}	RSDP/N Hold Time w.r.t. RSCLKP/N	400		ps

1. Set-up and hold times are specified for an interface which directly connects the S3028 receiver parallel outputs to the data and clock inputs on an external register.

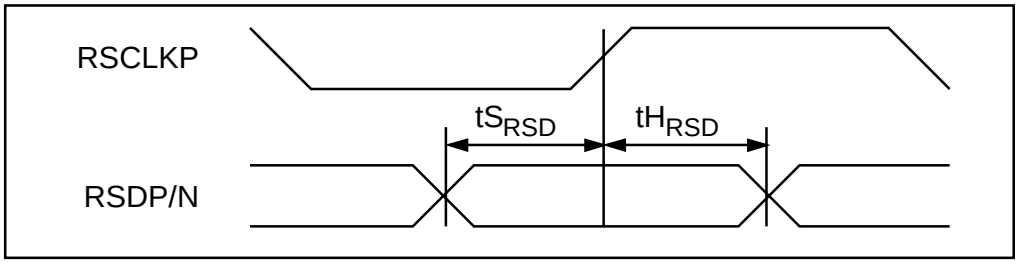
Figure 7. Receiver Output Timing



Notes on TTL Output Timing:

1. Output propagation delay time of TTL outputs is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.
2. Maximum output propagation delays and duty cycles of TTL outputs are measured with a 15 pF load.
3. When a set-up time is specified on TTL signals between an output and a clock, the set-up time is the time in nano seconds from the 50% point of the output to the 50% point of the clock.
4. When a hold time is specified on TTL signals between an output and a clock, the hold time is the time in nano seconds from the 50% point of the clock to the 50% point of the output.

Figure 8. Receiver Input Timing



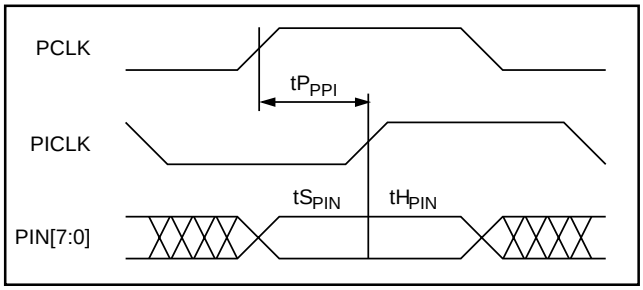
Notes on High-Speed PECL Input Timing

1.Timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

Table 15. AC Transmitter Timing Characteristics

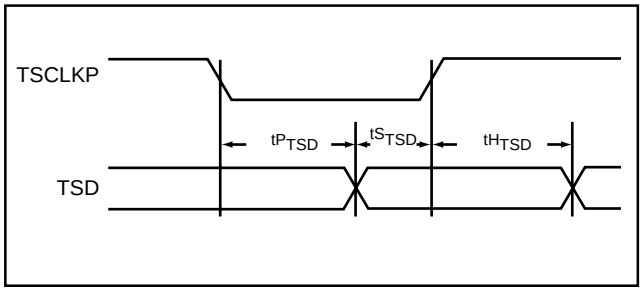
Symbol	Description	Min	Max	Units
	TSCLK Frequency (nom. 155.52 or 622.08 MHz)		640	MHz
	TSCLK Duty Cycle	40	60	%
	PICLK Duty Cycle	33	67	%
tP_{PPI}	PCLK to PICLK Propagation Delay		5.0	ns
tS_{PIN}	PIN[7.0] Set-up Time w.r.t. PICLK	1.5		ns
tH_{PIN}	PIN[7.0] Hold Time w.r.t. PICLK	1.0		ns
tP_{TSD}	TSCLK Low to TSD Valid Propagation Delay		440	ps
tS_{TSD}	TSD Set-up Time w.r.t. TSCLK	300		ps
tH_{TSD}	TSD Hold Time w.r.t. TSCLK	300		ps

Figure 9. Transmitter Input Timing



1. When a set-up time is specified on TTL signals between an input and a clock, the set-up time is the time in nano seconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in nano seconds from the 50% point of the clock to the 50% point of the input.

Figure 10. Transmitter Output Timing



Notes on High-Speed PECL Output Timing

1. Timing is measured from the cross-over point of the reference signal to the cross-over point of the output.

RECEIVER FRAMING

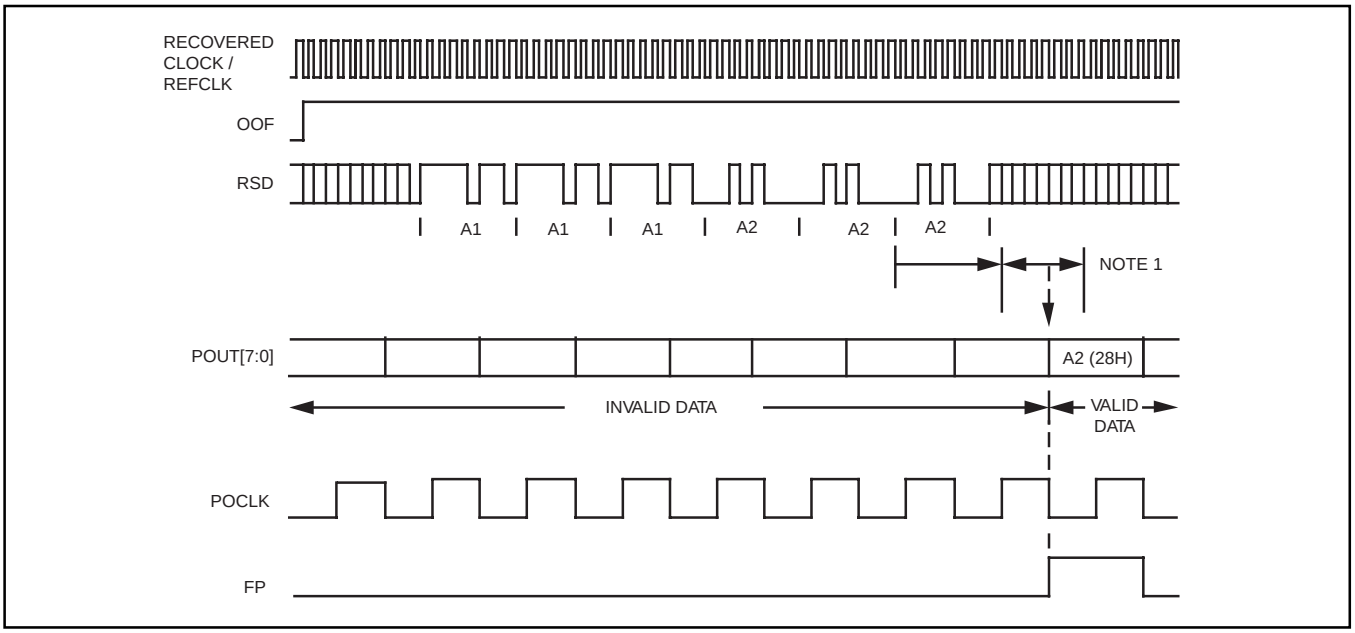
Figure 11 shows a typical reframe sequence in which a byte realignment is made. The frame and byte boundary detection is enabled by the rising edge of OOF and remains enabled while OOF is High. Both boundaries are recognized upon receipt of the third A2 byte which is the first data byte to be reported with the correct byte alignment on the outgoing data bus (POUT[7:0]). Concurrently, the Frame Pulse (FP) is set High for one POCLK cycle.

When interfacing with a section terminating device, the OOF input remains high for one full frame after the first frame pulse while the section terminating device verifies internally that the frame and byte alignment are correct, as shown in Figure 12. Since at least one framing pattern has been detected since the rising edge of OOF, boundary detection is disabled when OOF is set Low.

The frame and byte boundary detection block is activated by the rising edge of OOF, and stays active until the first FP or until OOF goes Low, whichever occurs last. Figure 12 shows a typical OOF timing pattern which occurs when the S3028 is connected to a down stream section terminating device. OOF remains high for one full frame after the first FP. The frame and byte boundary detection block is active until OOF goes Low.

Figure 13 shows the frame and byte boundary detection activation by a rising edge of OOF, and deactivated by the first FP.

Figure 11. Frame and Byte Detection



NOTE 1: Range of input to output delay can be 1.5 to 2.5 POCLK cycles.

Figure 12. OOF Operation Timing with PM5312 STTX or PM5355 SUNI-622

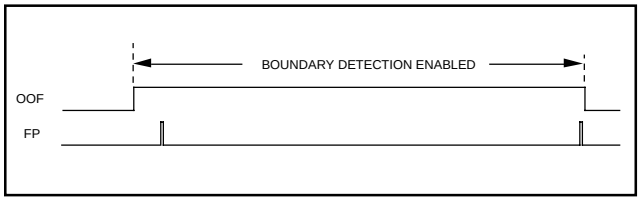
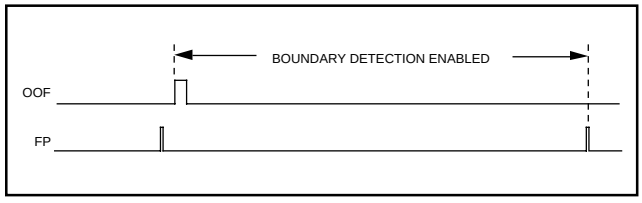


Figure 13. Alternate OOF Timing



S3028 WITH DATA CLOCK SYNCHRONOUS TO REFERENCE CLOCK

INTRODUCTION

In some applications it is necessary to “forward clock” the data in a SONET/SDH system. In this application the reference clock from which the high speed serial clock is synthesized and the parallel data clock both originate from the same (usually TTL/CMOS) clock source. This application note explains how the AMCC S3028 can be configured to operate in this mode.

Clock Control Logic Description

The timing control logic in the S3028 automatically generates an internal load signal which has a fixed relationship to the reference clock. The logic takes into account the variation of the reference clock to the internal load signal over temperature and voltage.

The connections required to implement the design are shown in Figure 14, and the timing specifications are shown in Figure 15. The setup and hold times for the reference clock to the data must be met by the controller ASIC. It is recommended to latch the data on the falling edge of the reference clock in order to meet the required specifications.

Possible Problems

In order to meet the jitter generation specifications required by SONET, the jitter of the reference clock must be minimized. It may be difficult to meet the SONET jitter generation specifications using a reference clock input with a TTL reference source.

Figure 14. S3028 with Data Clocked by Reference Clock

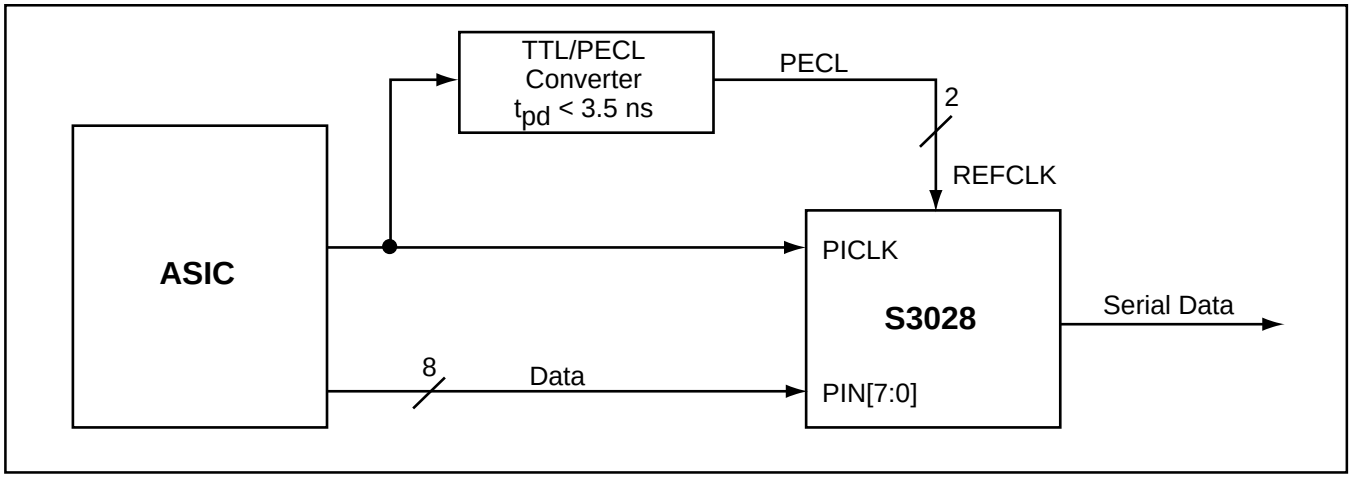
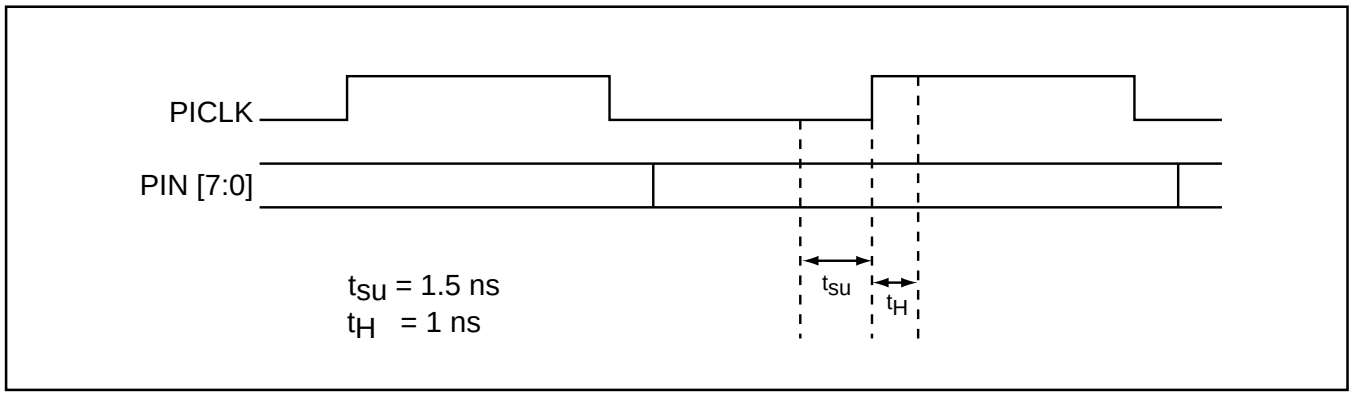
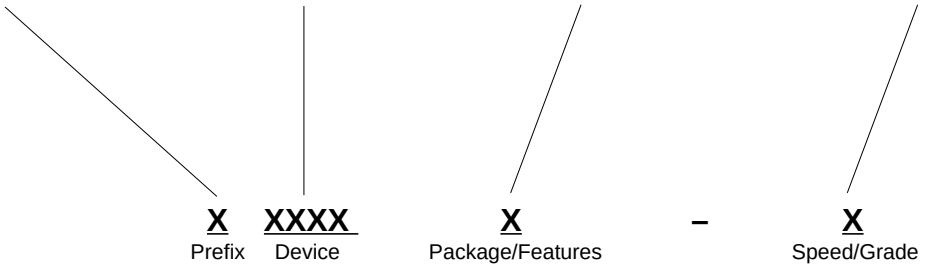


Figure 15. Data Timing with Respect to Reference Clock



Ordering Information

PREFIX	DEVICE	PACKAGE/FEATURES	SPEED GRADE
S – Integrated Circuit	3028	B – 64 PQFP, Loop Timing, Forward Clocking, "Squelched Clock" Operation	Blank – 155/622 Mbps 1 – 155 Mbps only



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