Features

- **Dual Mode Low Drop Out Voltage Regulator**
- **1.8V Fixed Output Voltage**
- **3V to 5.5V Supply Operation**
- **80 mA Maximum Load Current in Full Power Mode**
- **Maximum Current Consumption 36 µA in Full Power Mode and 14 µA in Low Power Mode**
- **Power-down Mode Consumption Less Than 1 µA**
- **More Than 70dB (Typical) PSRR at 1 KHz**
- **80 μV_{RMS} Output Noise**
- **0.35 µm CMOS Technology**
- **Typical Application: Baseband Memory Section Supply in Mobile Terminals**

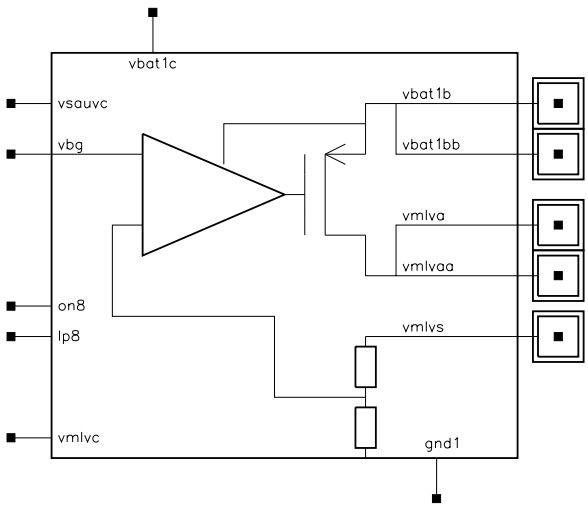
Description

RE029 is a dual mode Low Drop Out (LDO) voltage regulator macrocell with a fixed 1.8V output voltage, rated for loads up to 80 mA in full power mode and 5 mA in low power mode. (Both modes can be selected by the LP8 signal.) It is designed to be integrated with other analog cells, digital logic, microcontrollers, DSP cores and memory blocks into system-on-chip products.

The circuit consists of a PMOS pass device, an error amplifier and a feedback resistive network, sized to achieve the required closed loop gain. These blocks make up the regulating loop. An over-current and short circuit protection circuit has been included to limit the output current delivered by the regulator, thus avoiding destruction in case of a short circuit.

An external reference voltage V_{BG} (bandgap voltage) is necessary for correct functionality. The target reference voltage is 1.231V delivered, for example, by BG019. Double pads on the supply voltage V_{BAT1B}/V_{BAT1BB} and output voltage V_{MLVA}/V_{MLVAA} are used to reduce the total output resistance. Current reference is generated inside the cell through a circuit supplied by a 2.5V ± 0.1V of regulated input voltage on V_{SAUVC}. Remote sense terminal V_{MLVS} provides regulation of the load by connecting it to the output terminal near a critical point to improve performance of the regulator (e.g., connecting it to the package pin by double-bonding, thus avoiding the bonding resistance influence). A ceramic capacitor of 2.2 µF connected from V_{MLVA}/V_{MLVAA} to ground is needed as external compensation.

Figure 1. Symbol [1]



Note: 1. Pin names are written as they appear on the user screen when the symbol is opened in the design tool environment.

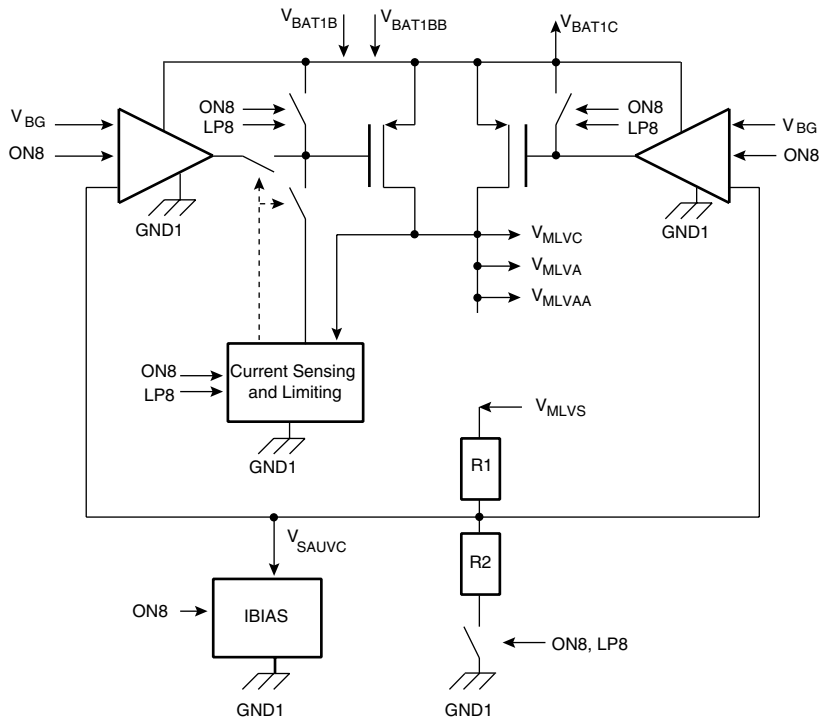
Embedded ASIC Macrocell: Power Management for Mobile Terminals (PM)

RE029 1.8V 80 mA Dual Mode LDO Regulator

Rev. 2705A–PMGMT–03/02

Functional Diagram

Figure 2. Functional Diagram



Pin Description

Pin Name	I/O	Type	Function	Value
V_{BAT1B}	Power Supply	External Pad	Power Supply	3V to 5.5V
V_{BAT1BB}	Power Supply	External Pad	Power Supply	3V to 5.5V
V_{MLVA}	Analog Output	External Pad	Output Voltage	1.7V to 1.9V
V_{MLVAA}	Analog Output	External Pad	Output Voltage	1.7V to 1.9V
V_{MLVS}	Analog Input	External Pad	Sense Voltage	1.7V to 1.9V
V_{MLVC}	Analog Output	Internal Pin	Output Voltage	1.7V to 1.9V
V_{BAT1C}	Auxiliary Power Supply	Internal Pin	Power Supply	3V to 5.5V
GND1	Analog Ground	Internal Pin	Ground	0
V_{SAUVC}	Positive Power Supply	Internal Pin	Power Supply	2.5V ± 0.1V
V_{BG}	Analog Input	Internal Pin	Voltage Reference	1.231V
ON8	Digital Input	Internal Pin	Enable Command	0V or V_{BAT1B}/V_{BAT1BB}
LP8	Digital Input	Internal Pin	Low Power Mode Command	0V or V_{BAT1B}/V_{BAT1BB}

Absolute Maximum Ratings*

Analog Signals	-0.3V to 6.5V
Digital Signals	-0.3V to 5.5V
Output Current	Internally limited
Junction Temperature	-20°C to 150°C

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications(1)

T_J = -20°C to 125°C, V_{BAT1B}/V_{BAT1BB} = 3V to 5.5V unless otherwise specified, output capacitance = 2.2 µF.

Table 1. Electrical Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{BAT1B}/V_{BAT1BB}	Operating Supply Voltage			3		5.5	V
V_{SAUVC}	Auxiliary Operating Supply Voltage			2.4	2.5	2.6	V
T_J	Temperature Range			-20		125	°C
Full Power Mode							
V_{MLVA}/V_{MLVAA}	Output Voltage			1.72		1.87	V
I_{MLVA}/I_{MLVAA}	Output Current					80	mA
I_{QQ}	Quiescent Current			25	30	36	µA
ΔV_{DC}	Line Regulation	V_{BAT1B}/V_{BAT1BB}= 3.4V to 3.V; I_{MLVA}/I_{MLVAA} = 80 mA			0.5	1	mV
ΔV_{TRAN}	Transient Line Regulation	V_{BAT1B}/V_{BAT1BB} = 3.4V to 3V; I_{MLVA}/I_{MLVAA} = 80 mA rise time = fall time = 5 µs			2	2.7	mV
ΔV_{DC}	Load Regulation	10% - 90% of max I_{MLVA}/I_{MLVAA};			2	4.2	mV
ΔV_{TRAN}	Transient Load Regulation	10% - 90% of max I_{MLVA}/I_{MLVAA}; rise time = fall time = 5 µs			5	23	mV
PSRR(2)	Power Supply Rejection Ratio at Full Load	V_{BAT1B}/V_{BAT1BB} = 3V	@100 Hz	-80		-85	dB
			@1 kHz	-79		-80	dB
			@20 kHz	-51		-60	dB
			@100 kHz	-29		-39	dB
		V_{BAT1B}/V_{BAT1BB} = 4.25V	@100 Hz	-68		-73	dB
			@1 kHz	-68		-73	dB
			@20 kHz	-58		-62	dB
			@100 kHz	-32		-39	dB
		V_{BAT1B}/V_{BAT1BB} = 5.5V	@100 Hz	-62		-68	dB
			@1 kHz	-62		-68	dB
			@20 kHz	-53		-59	dB
			@100 kHz	-32		-39	dB

Table 1. Electrical Characteristics (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_N	Output Noise[3]	Bandwidth = 10 Hz to 100 kHz			46	80	μV_{RMS}
T_R	Rise Time	Full Load 10% - 90% of V_{MLVA}/V_{MLVAA}				130	µs
I_{SD}	Shut Down Current					1	µA
I_{CC}	Short-circuit Current Threshold					130	mA
Low Power Mode							
V_{MLVA}/V_{MLVAA}	Output Voltage			1.7		1.9	V
I_{MLVA}/I_{MLVAA}	Output Current					5	mA
I_{QQ}	Quiescent Current			9.75	11.5	13.75	µA
ΔV_{DC}	Line Regulation	V_{BAT1B}/V_{BAT1BB}= 3.4V to 3.V; I_{MLVA}/I_{MLVAA} = 5 mA			0.5	1	mV
ΔV_{TRAN}	Transient Line Regulation	V_{BAT1B}/V_{BAT1BB} = 3.4V to 3V; I_{MLVA}/I_{MLVAA} = 5 mA rise time = fall time = 5 µs			1.2	1.7	mV
ΔV_{DC}	Load Regulation	10% - 90% of max I_{MLVA}/I_{MLVAA}			4.7	7.8	mV
ΔV_{TRAN}	Transient Load Regulation	10% - 90% of max I_{MLVA}/I_{MLVAA}; rise time = fall time = 5 µs			2	4.5	mV
PSRR[2]	Power Supply Rejection Ratio at Full Load	V_{BAT1B}/V_{BAT1BB} = 3V	@100 Hz	-70		-74	dB
			@1 kHz	-70		-74	dB
			@20 kHz	-58		-69	dB
			@100 kHz	-30		-36	dB
		V_{BAT1B}/V_{BAT1BB} = 4.25V	@100 Hz	-52		-72	dB
			@1 kHz	-52		-72	dB
			@20 kHz	-49		-59	dB
			@100 kHz	-30		-41	dB
		V_{BAT1B}/V_{BAT1BB} = 5.5V	@100 Hz	-43		-50	dB
			@1 kHz	-43		-50	dB
			@20 kHz	-43		-49	dB
			@100 kHz	-35		-42	dB
V_N	Output Noise[3]	Bandwidth = 10 Hz to 100 kHz			90	170	μV_{RMS}
T_R	Rise Time	Full Load 10% - 90% of V_{MLVA}/V_{MLVAA}				170	µs
I_{SD}	Shut Down Current					1	µA

Notes: 1. Obtained by considering the parasitics of a TFBGA100 Package.
2. This parameter shows the immunization of the circuit taking into account a voltage ripple on battery voltage for different frequencies shown.
3. Obtained by using BG019 as reference voltage generator.

Control Modes

All digital signals are referred to the supply voltage $V_{BAT1B,}$ V_{BAT1BB}.

Table 2. Truth Table

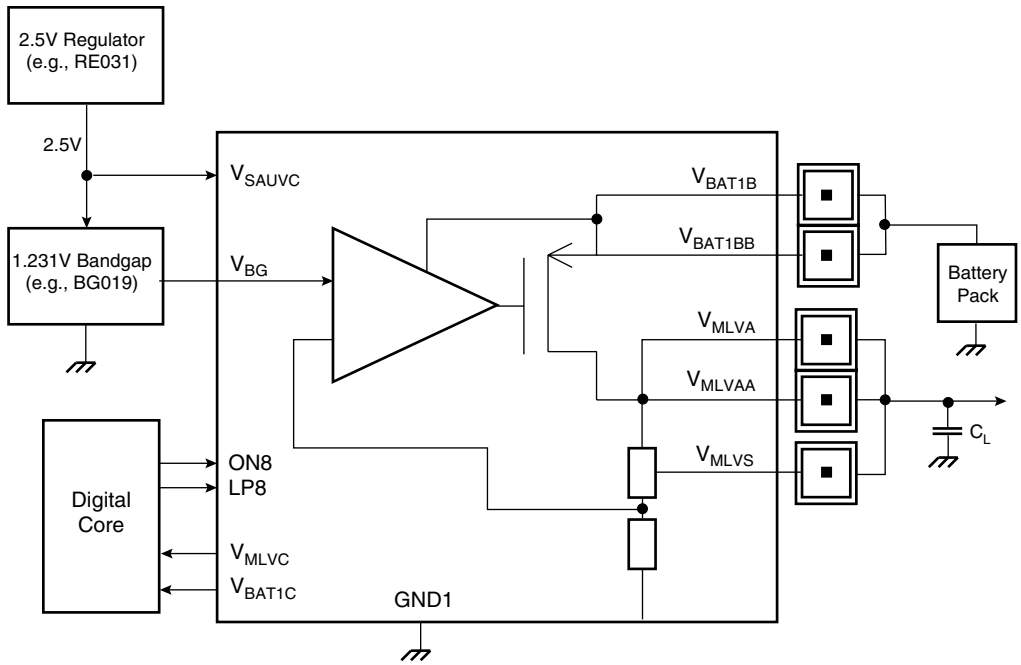
ON8	LP8	V_{MLVA}/V_{MLVAA}
0	X	Power down (High-Z)
1	0	Power on, Full Power Mode V_{MLVA}/V_{MLVAA} = 1.8V
1	1	Power on, Low Power Mode V_{MLVA}/V_{MLVAA} = 1.8V

Application Example

A ceramic capacitor (C_L) of 2.2 µF with ESR between 20 mΩ and 250 mΩ connected from V_{MLVA}/V_{MLVAA} to ground is needed for external compensation.

Description	Min	Typ	Max	Units
Capacitor (C_L)	1.8	2.2	2.6	µF

Figure 3. Application Example



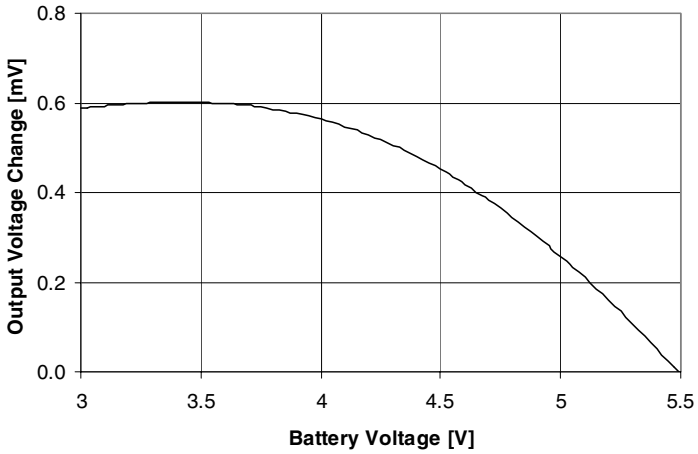
Typical Performance Characteristics (Conditions specified on page 10)

Note.

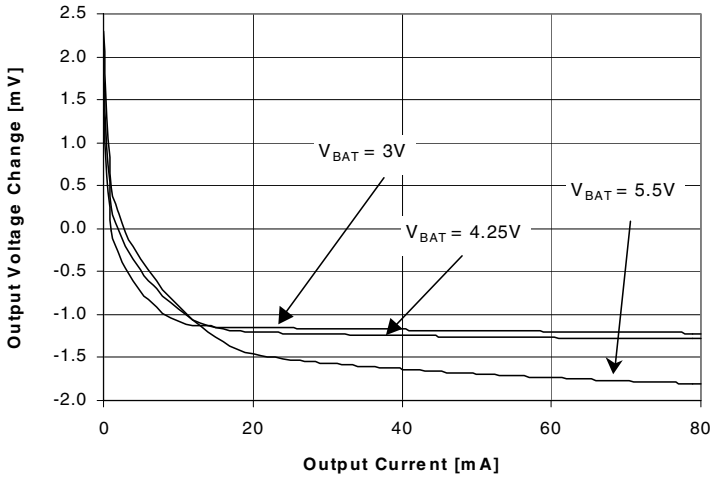
In these graphs:

- Output Voltage (V_{MLV}) refers to V_{MLVA}/V_{MLVAA}
- Battery Voltage (V_{BAT}) refers to V_{BAT1B}/V_{BAT1BB}
- Output Current (I_{MLV}) refers to I_{MLVA}/I_{MLVAA}

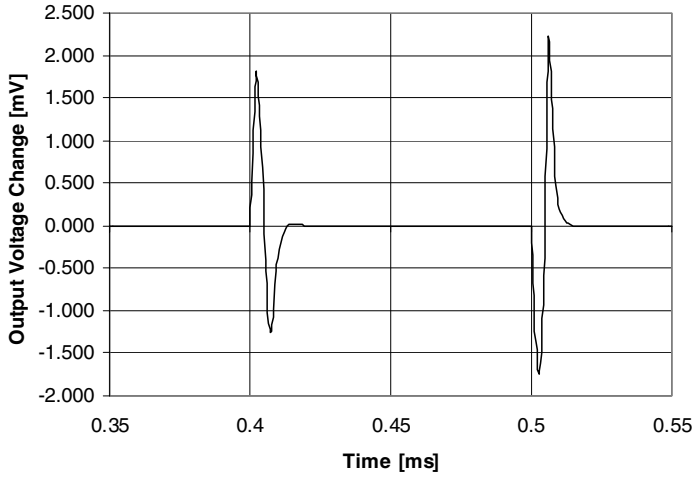
Static Line Regulation at Full Load in Full Power Mode



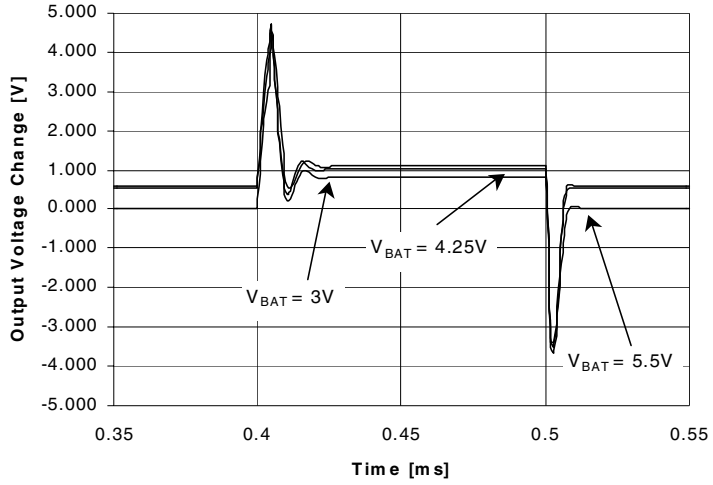
Static Load Regulation in Full Power Mode



Transient Line Regulation at Full Load in Full Power Mode

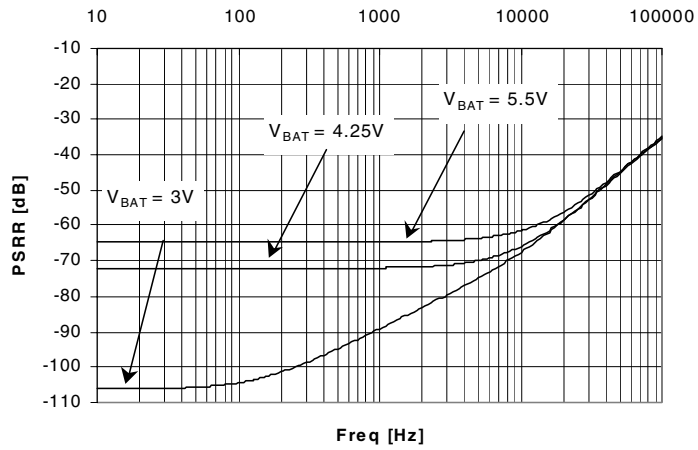


Transient Load Regulation in Full Power Mode

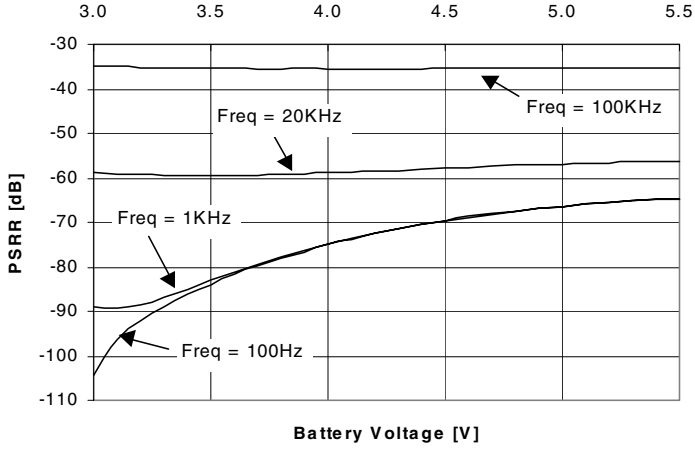


Typical Performance Characteristics (Conditions specified on page 10)

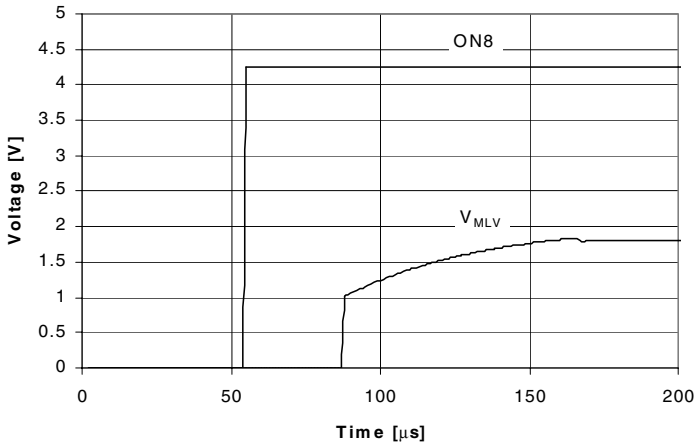
Power Supply Rejection Ratio at Full Load in Full Power Mode



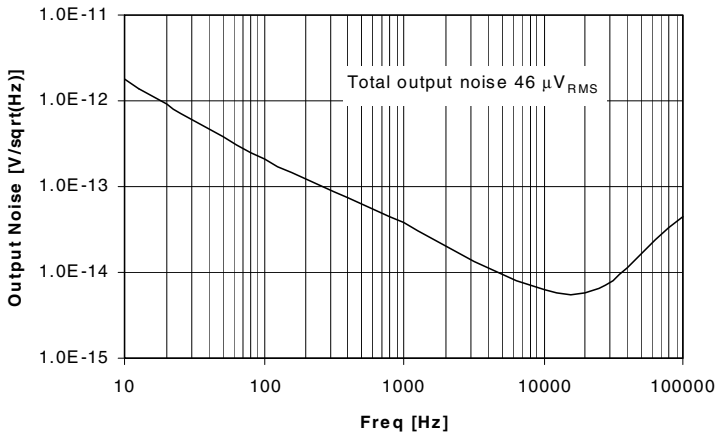
Power Supply Rejection Ratio at Full Load Versus Battery Voltage in Full Power Mode



LDO Startup at Full Load for V_{BAT} = 4.25V in Full Power Mode

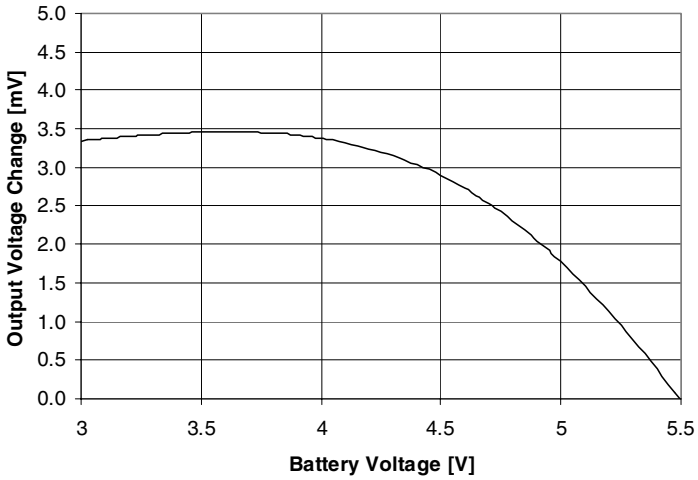


Output Noise Spectrum at Full Load and V_{BAT} = 4.25V in Full Power Mode

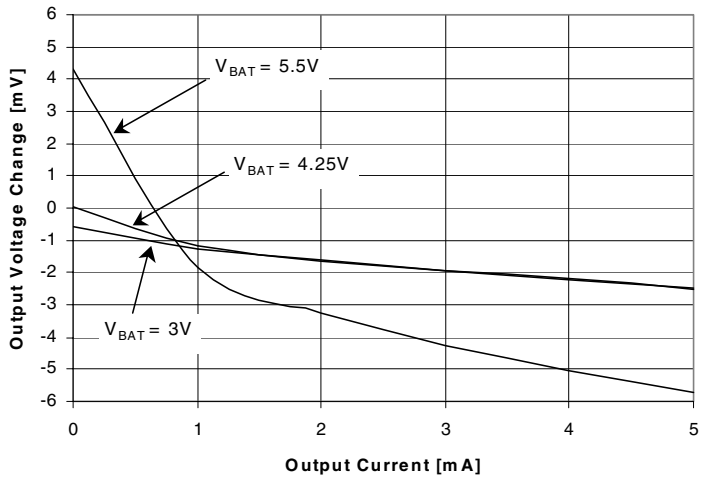


Typical Performance Characteristics (Conditions specified on page 10)

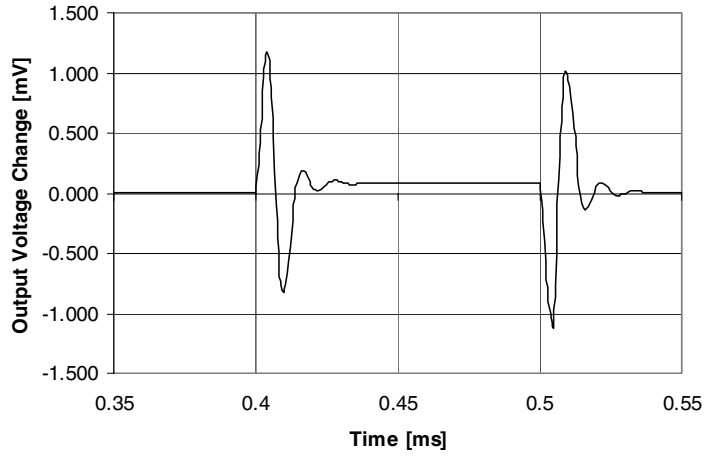
Static Line Regulation at Full Load in Low Power Mode



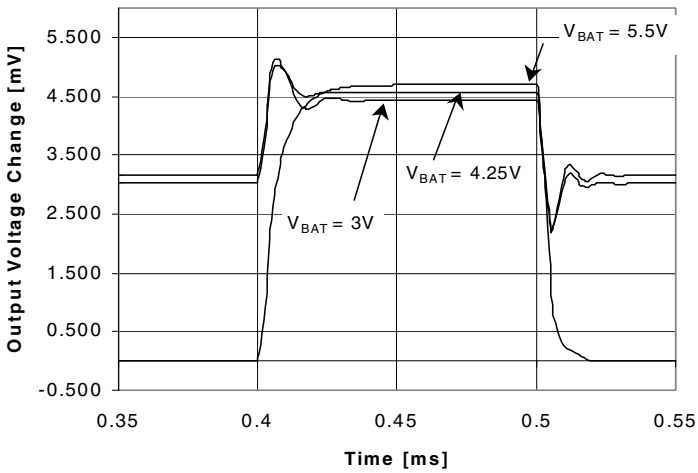
Static Load Regulation in Low Power Mode



Transient Line Regulation at Full Load in Low Power Mode

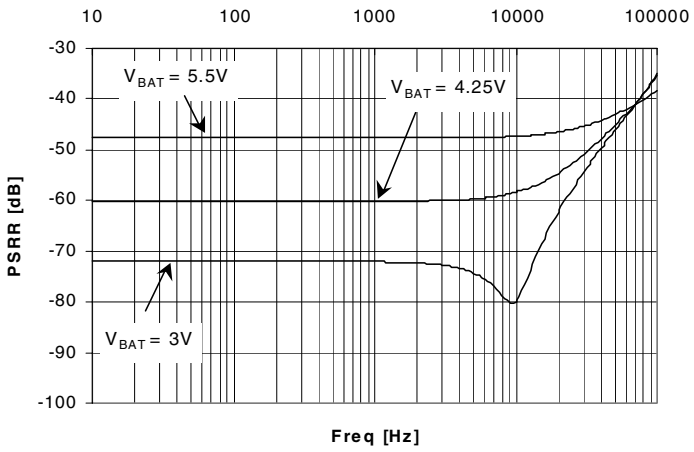


Transient Load Regulation in Low Power Mode

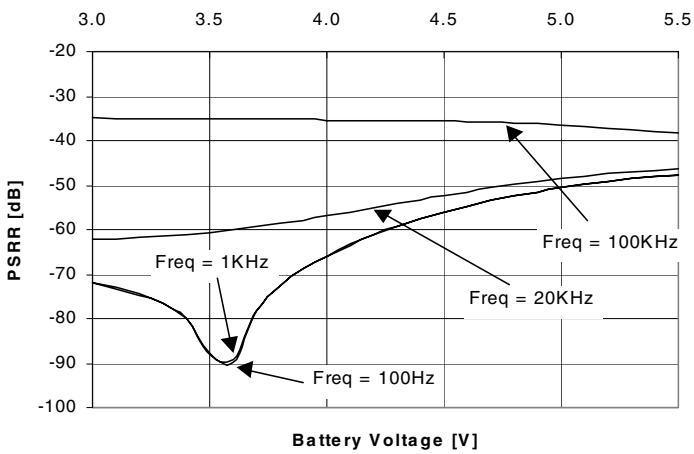


Typical Performance Characteristics (Conditions specified on page 10)

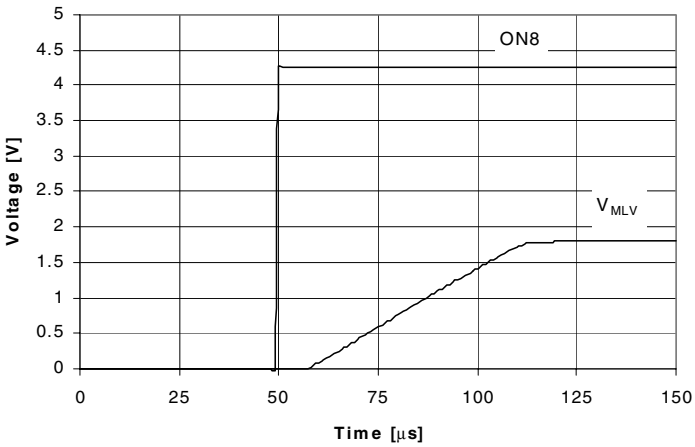
Power Supply Rejection Ratio at Full Load in Low Power Mode



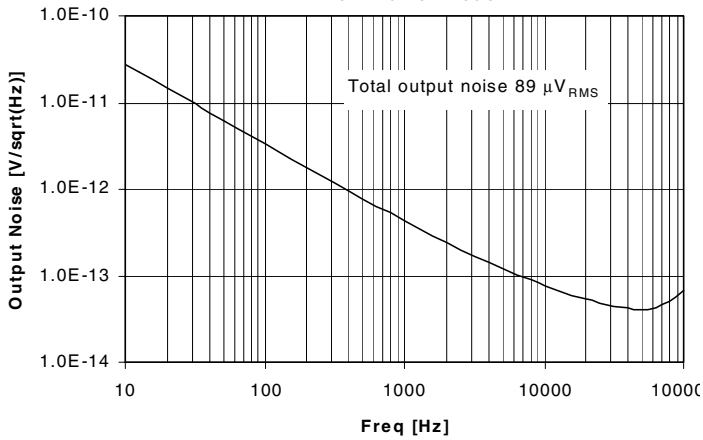
Power Supply Rejection Ratio at Full Load Versus Battery Voltage in Low Power Mode



LDO Startup at Full Load for V_{BAT} = 4.25V in Low Power Mode



Output Noise Spectrum at Full Load and V_{BAT} = 4.25V in Low Power Mode

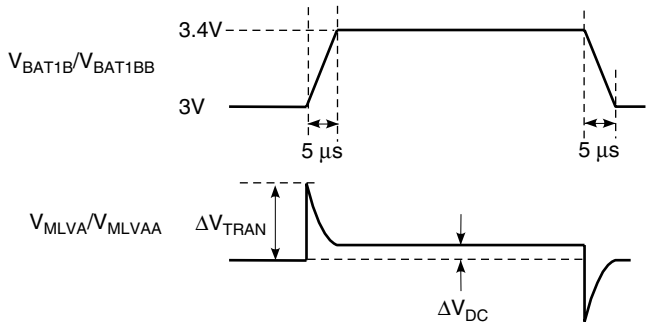


Terminology

Line Regulation

Measures the maximum transient and DC variations of the output voltage of the RE029 when the supply changes between two specified values with fixed load current; minimum rise time and fall time is 5 µs.

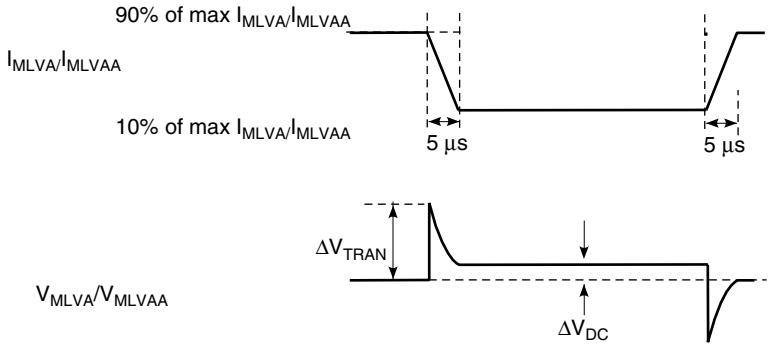
Figure 4. Line Regulation



Load Regulation

Measures the maximum transient and DC variations of the output voltage of the RE029 when the load current changes between two specified values with fixed power supply; minimum rise time and fall time is 5 µs.

Figure 5. Load Regulation



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