



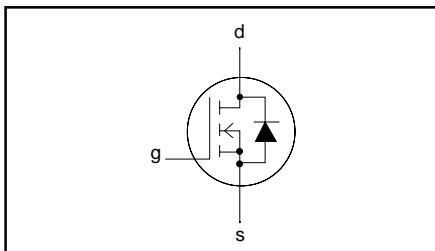
N-channel logic level TrenchMOS™ transistor

PSMN003-25W

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

| |
|---|
| $V_{DSS} = 25\text{ V}$ |
| $I_D = 100\text{ A}$ |
| $R_{DS(ON)} \leq 3.2\text{ m}\Omega (V_{GS} = 10\text{ V})$ |
| $R_{DS(ON)} \leq 3.5\text{ m}\Omega (V_{GS} = 5\text{ V})$ |

GENERAL DESCRIPTION

SiliconMAX products use the latest Philips Trench technology to achieve the lowest possible on-state resistance in each package at each voltage rating.

Applications:-

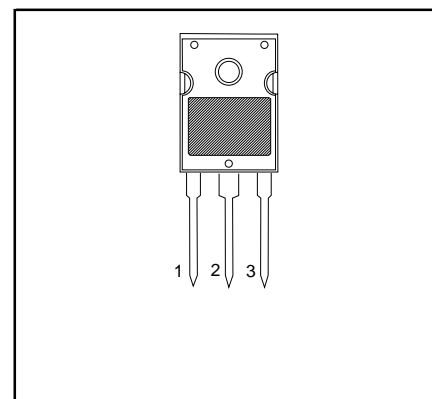
- d.c. to d.c. converters
- switched mode power supplies

The PSMN003-25W is supplied in the SOT429 (TO247) conventional leaded package.

PINNING

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | gate |
| 2 | drain |
| 3 | source |
| tab | drain |

SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------------|--|--|------|------------------|------------------|
| V_{DSS} | Drain-source voltage | $T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$ | - | 25 | V |
| V_{DGR} | Drain-gate voltage | $T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 25 | V |
| V_{GS} | Continuous gate-source voltage | | - | ± 15 | V |
| V_{GSM} | Peak pulsed gate-source voltage | $T_j \leq 150\text{ }^\circ\text{C}$ | - | ± 20 | V |
| I_D | Continuous drain current | $T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 5\text{ V}$ | - | 100 ¹ | A |
| | | $T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 5\text{ V}$ | - | 100 ¹ | A |
| I_{DM} | Pulsed drain current | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 300 | A |
| P_D | Total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 300 | W |
| T_j, T_{stg} | Operating junction and storage temperature | | -55 | 175 | $^\circ\text{C}$ |

1 Maximum continuous current limited by package.

SiliconMAX

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|----------|----------------------------------|--|------|------|------|
| E_{AS} | Non-repetitive avalanche energy | Unclamped inductive load, $I_{AS} = 100$ A; $t_p = 100$ μ s; T_j prior to avalanche = 25°C; $V_{DD} \leq 15$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 5$ V; refer to fig:15 | - | 162 | mJ |
| I_{AS} | Non-repetitive avalanche current | | - | 100 | A |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------------|--|-------------|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | | - | - | 0.5 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | in free air | - | 45 | - | K/W |

ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---------------|----------------------------------|--|------------------|--------------------------|--------------------------|--|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$ | 25 23 | - - | - - | V V |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$ | 1 0.5 | 1.5 - | 2 - | V V |
| $R_{DS(ON)}$ | Drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 25$ A $V_{GS} = 5$ V; $I_D = 25$ A $V_{GS} = 4.5$ V; $I_D = 25$ A $V_{GS} = 5$ V; $I_D = 25$ A; $T_j = 175^\circ\text{C}$ | - - - - | 2.8 3.1 3.3 4.8 | 3.2 3.5 4.0 6.5 | m Ω m Ω m Ω m Ω |
| I_{GSS} | Gate-source leakage current | $V_{GS} = \pm 5$ V; $V_{DS} = 0$ V; | - | 0.02 | 100 | nA |
| I_{DSS} | Zero gate voltage drain current | $V_{DS} = 25$ V; $V_{GS} = 0$ V; $T_j = 175^\circ\text{C}$ | - | 0.05 | 10 500 | μ A μ A |
| $Q_{g(tot)}$ | Total gate charge | $I_D = 100$ A; $V_{DD} = 15$ V; $V_{GS} = 5$ V | - | 219 | - | nC |
| Q_{gs} | Gate-source charge | | - | 30 | - | nC |
| Q_{gd} | Gate-drain (Miller) charge | | - | 113 | - | nC |
| $t_{d\ on}$ | Turn-on delay time | $V_{DD} = 15$ V; $R_D = 0.6$ Ω ; | - | 28 | - | ns |
| t_r | Turn-on rise time | $V_{GS} = 10$ V; $R_G = 5.6$ Ω | - | 133 | - | ns |
| $t_{d\ off}$ | Turn-off delay time | Resistive load | - | 716 | - | ns |
| t_f | Turn-off fall time | | - | 424 | - | ns |
| L_d | Internal drain inductance | Measured tab to centre of die | - | 3.5 | - | nH |
| L_d | Internal drain inductance | Measured from drain lead to centre of die | - | 4.5 | - | nH |
| L_s | Internal source inductance | Measured from source lead to source bond pad | - | 7.5 | - | nH |
| C_{iss} | Input capacitance | $V_{GS} = 0$ V; $V_{DS} = 20$ V; $f = 1$ MHz | - | 12.6 | - | nF |
| C_{oss} | Output capacitance | | - | 3500 | - | pF |
| C_{rss} | Feedback capacitance | | - | 2400 | - | pF |



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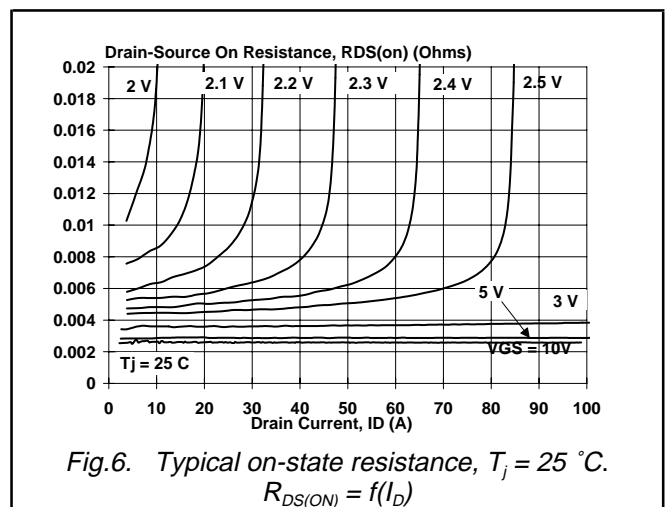
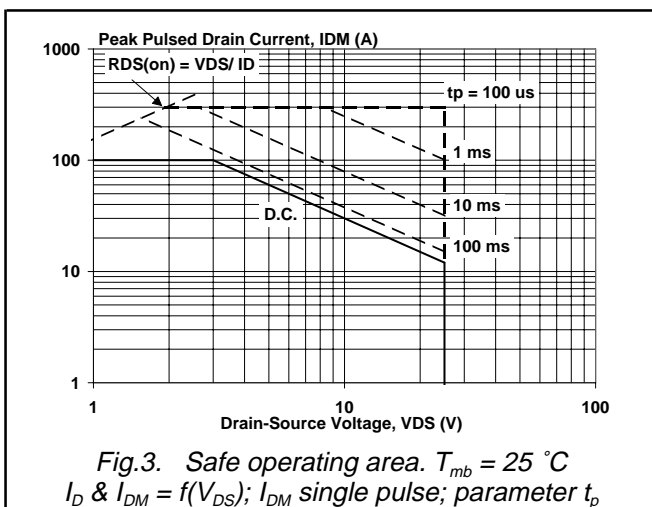
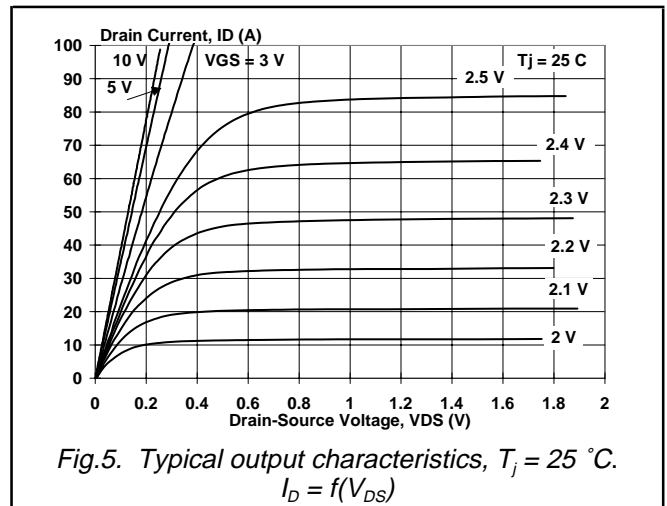
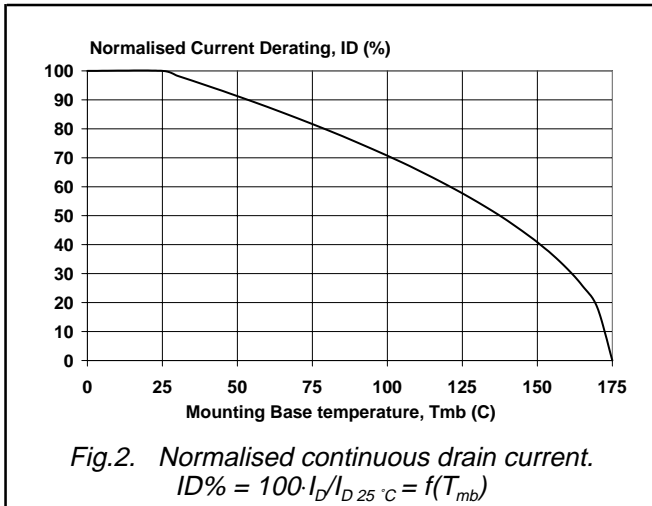
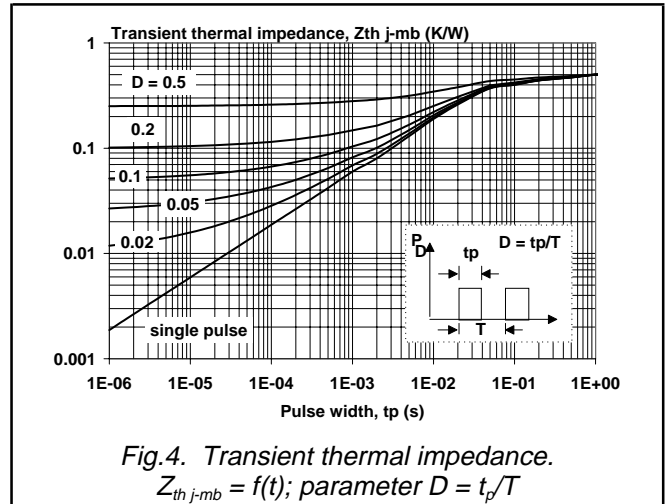
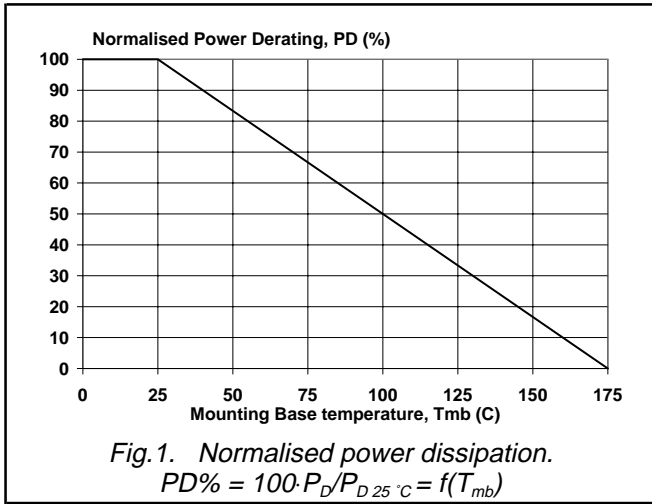
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------|--|---|------|------|------|---------------|
| I_S | Continuous source current (body diode) | | - | - | 100 | A |
| I_{SM} | Pulsed source current (body diode) | | - | - | 300 | A |
| V_{SD} | Diode forward voltage | $I_F = 25\text{ A}; V_{GS} = 0\text{ V}$ | - | 0.85 | 1.2 | V |
| | | $I_F = 75\text{ A}; V_{GS} = 0\text{ V}$ | - | 1.0 | - | |
| t_{rr} | Reverse recovery time | $I_F = 20\text{ A}; -dI_F/dt = 100\text{ A}/\mu\text{s};$ | - | 250 | - | ns |
| Q_{rr} | Reverse recovery charge | $V_{GS} = 0\text{ V}; V_R = 20\text{ V}$ | - | 1.5 | - | μC |



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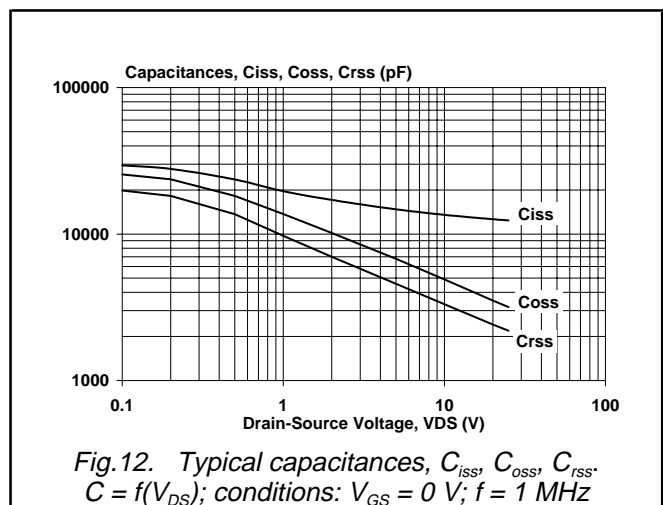
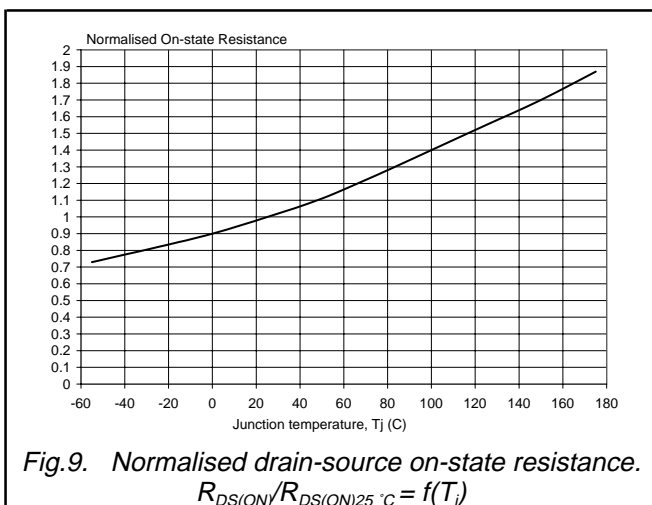
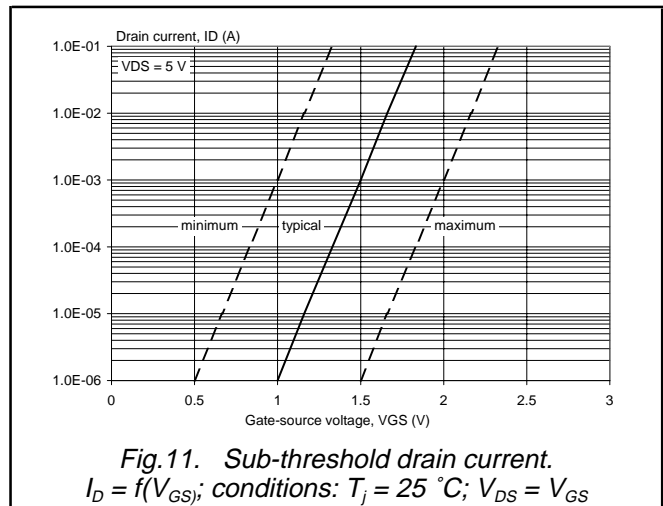
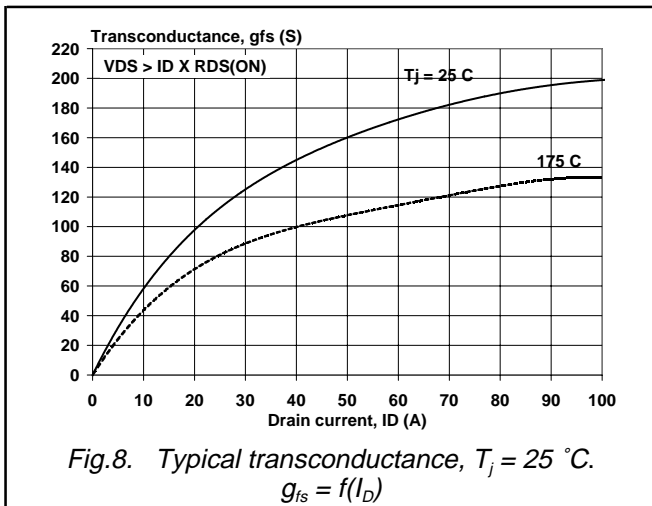
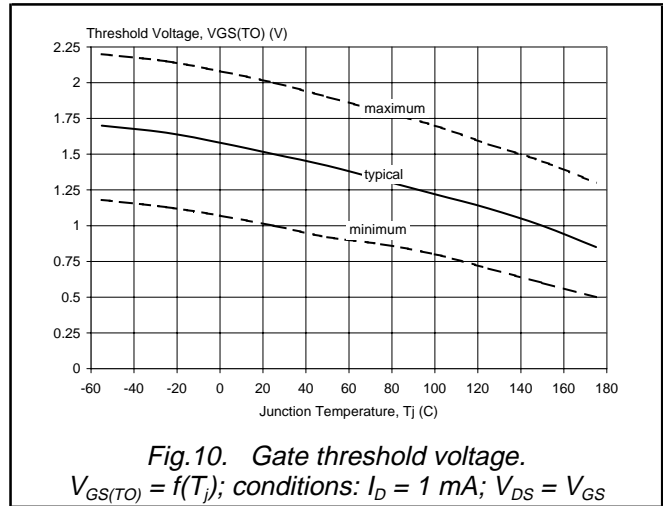
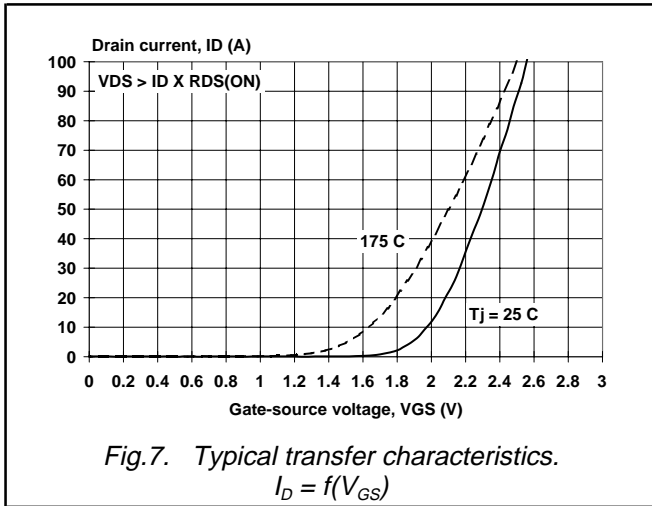
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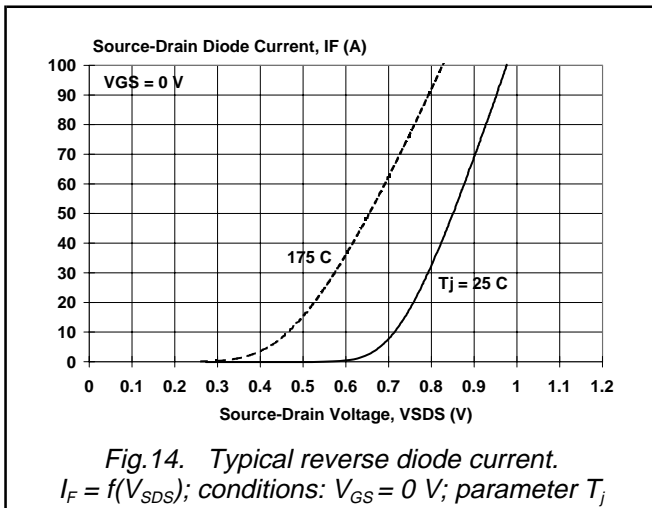
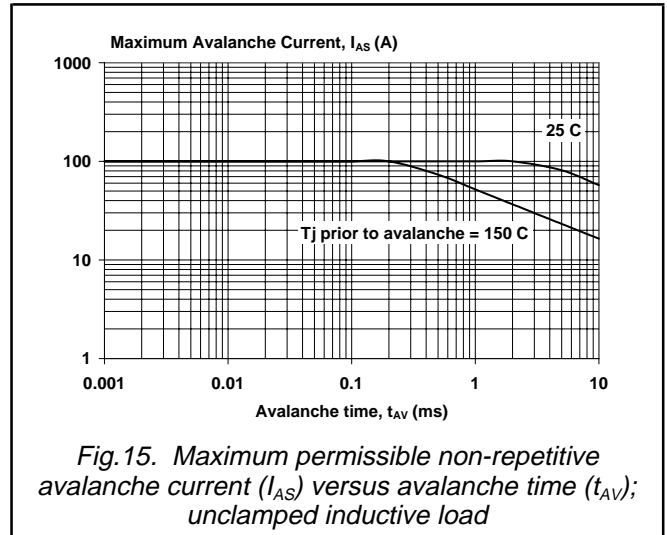
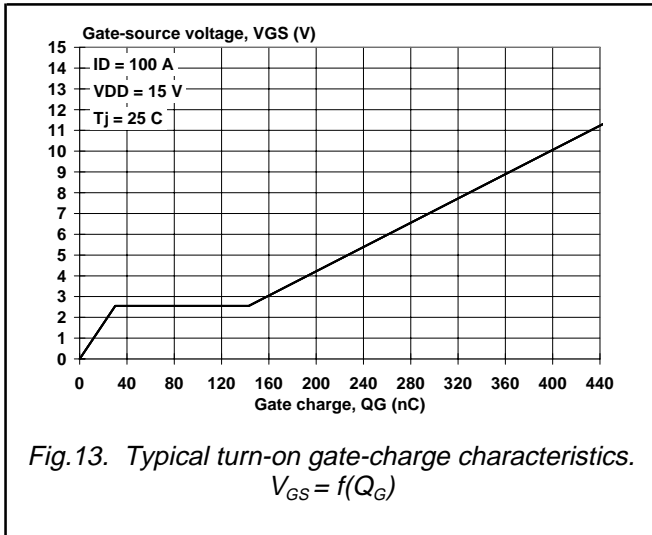
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MECHANICAL DATA

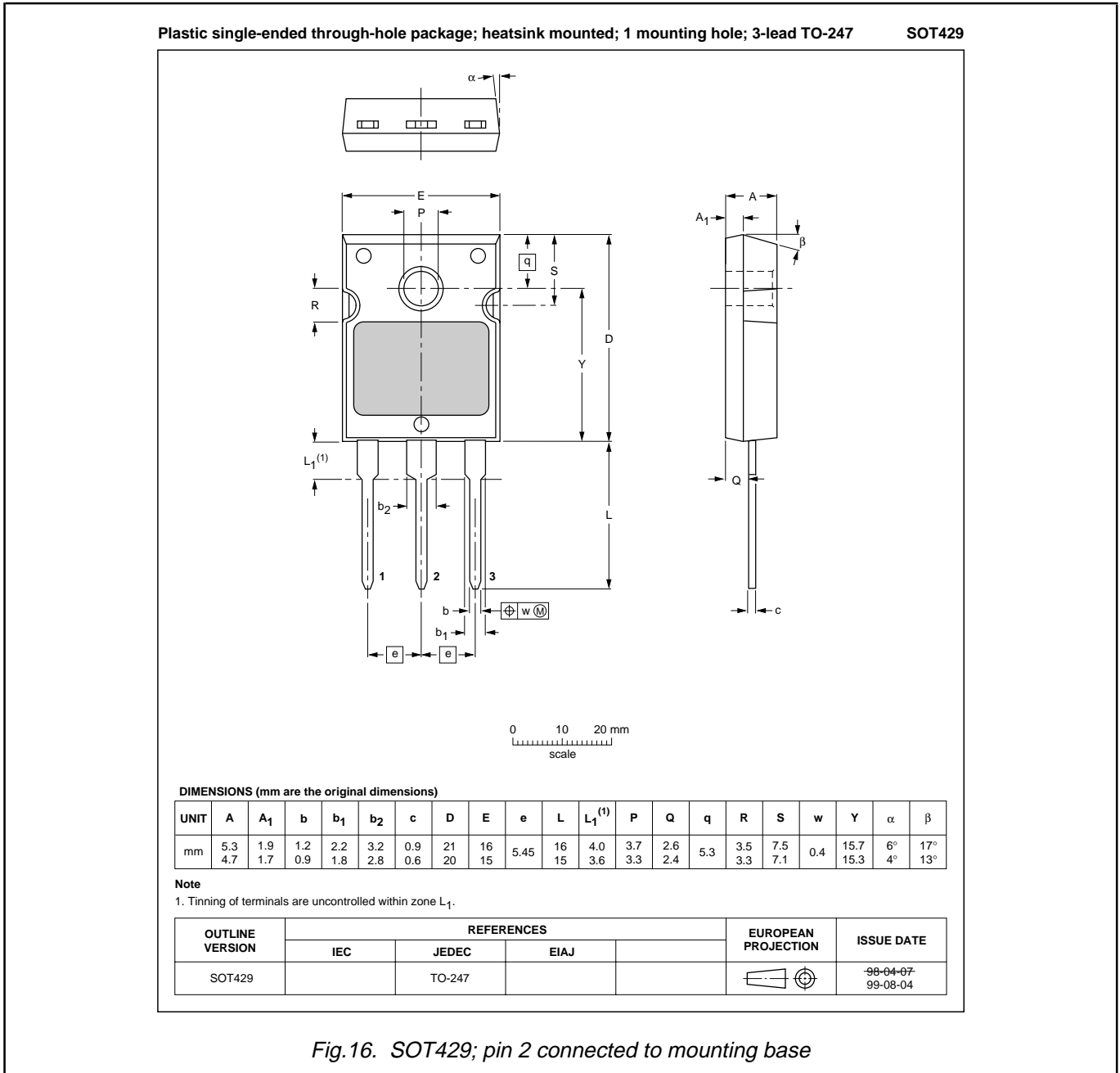


Fig.16. SOT429; pin 2 connected to mounting base

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT429 envelope.
3. Epoxy meets UL94 V0 at 1/8".



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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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